Order this document by MC4741C/D

MOTOROLA

MC4741C

Differential Input Operational Amplifier

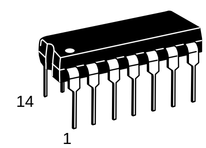
The MC4741C is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741C can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

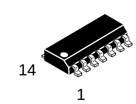
- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER
(QUAD MC1741)

SEMICONDUCTOR TECHNICAL DATA

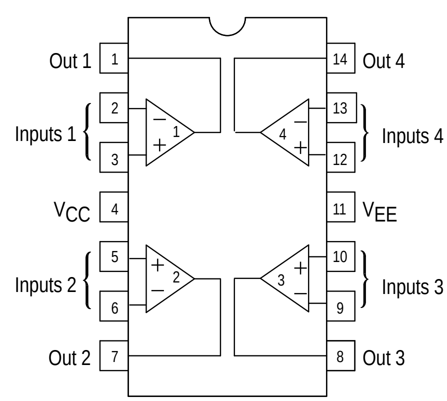


P SUFFIX
PLASTIC PACKAGE
CASE 646



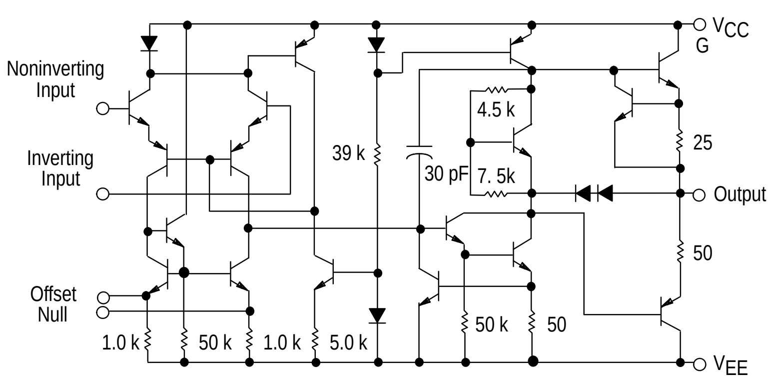
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram
(1/4 of Circuit Shown)



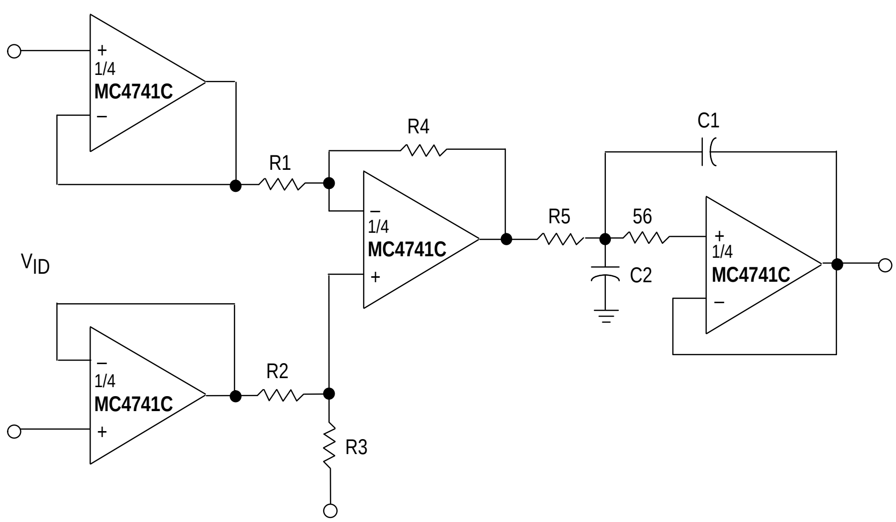
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC4741CD	T_A = 0° to +70°C	SO–14
MC4741CP		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±36	V
Input Common Mode Voltage	V_{ICM}	±18	V
Output Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

High Impedance Instrumentation Buffer/Filter



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_v	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection (R_S ≤ 10 k)	CMR	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	µV/V
Output Voltage Swing (R_L ≥ 10 k) (R_L ≥ 2 k)	V_O	 ±12 ±10	 ±14 ±13	 – –	V
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	105	210	mW
Transient Response (Unity Gain – Non–Inverting) (V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Rise Time (V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Overshoot (V_I = 10 V, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Slew Rate	 t_{TLH} os SR	 – – –	 0.3 15 0.5	 – – –	 µs % V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = * T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current (T_A = 0° to + 70°C)	I_{IO}	–	–	300	nA
Input Bias Current (T_A = 0° to + 70°C)	I_{IB}	–	–	800	nA
Large Signal Voltage Gain (R_L ≥ 2k, V_{OUT} = ±10 V)	A_V	15	–	–	V/mV
Output Voltage Swing (R_L ≥ 2 k)	V_O	±10	±13	–	V

* T_{high} = 70°C T_{low} = –0°C

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

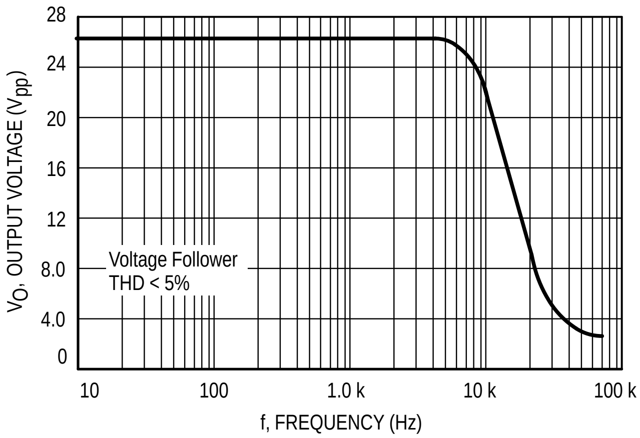


Figure 2. Open Loop Frequency Response

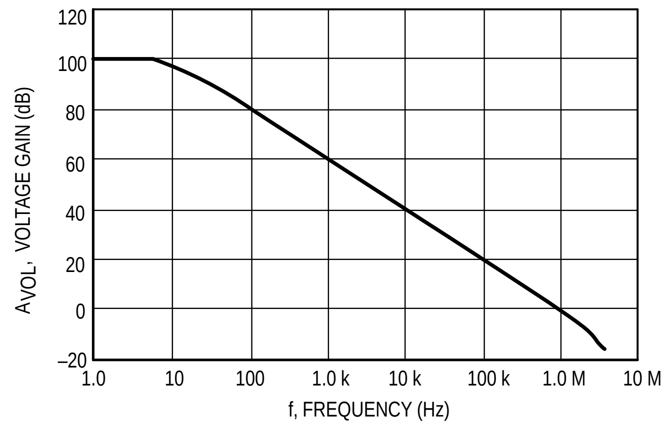


Figure 3. Positive Output Voltage Swing versus Load Resistance

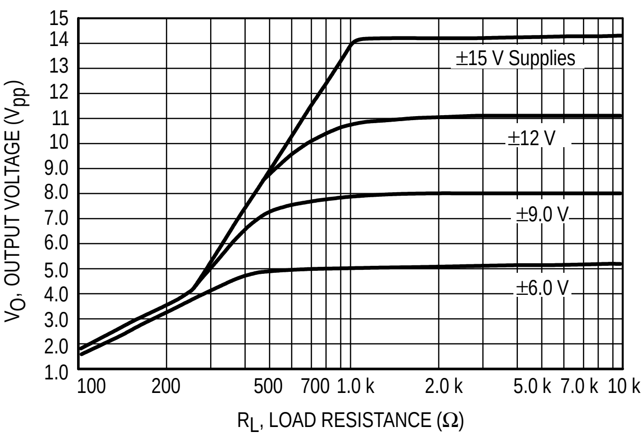


Figure 4. Negative Output Voltage Swing versus Load Resistance

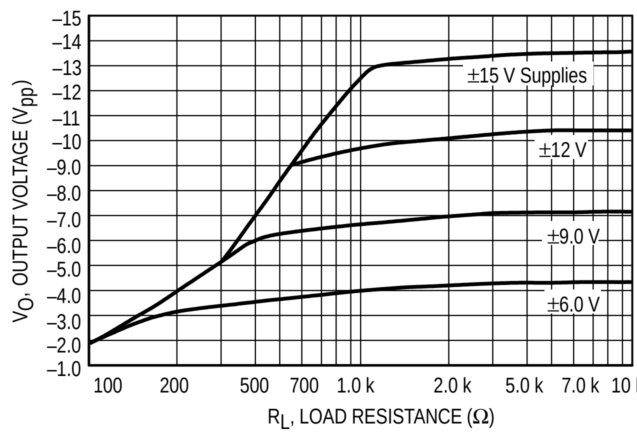


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

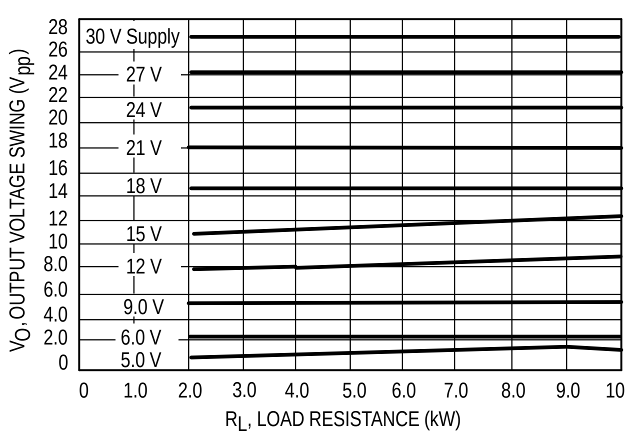


Figure 6. Noninverting Pulse Response

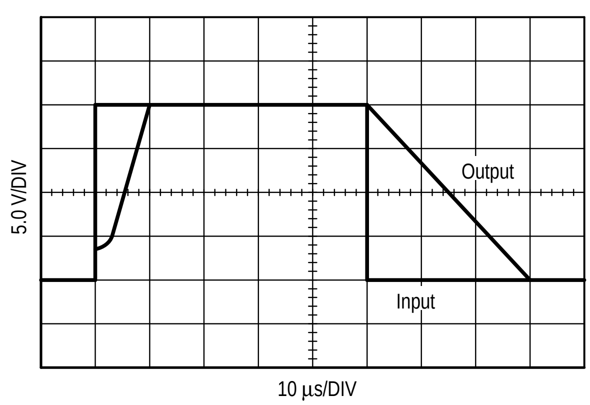


Figure 7. Bi–Quad Filter

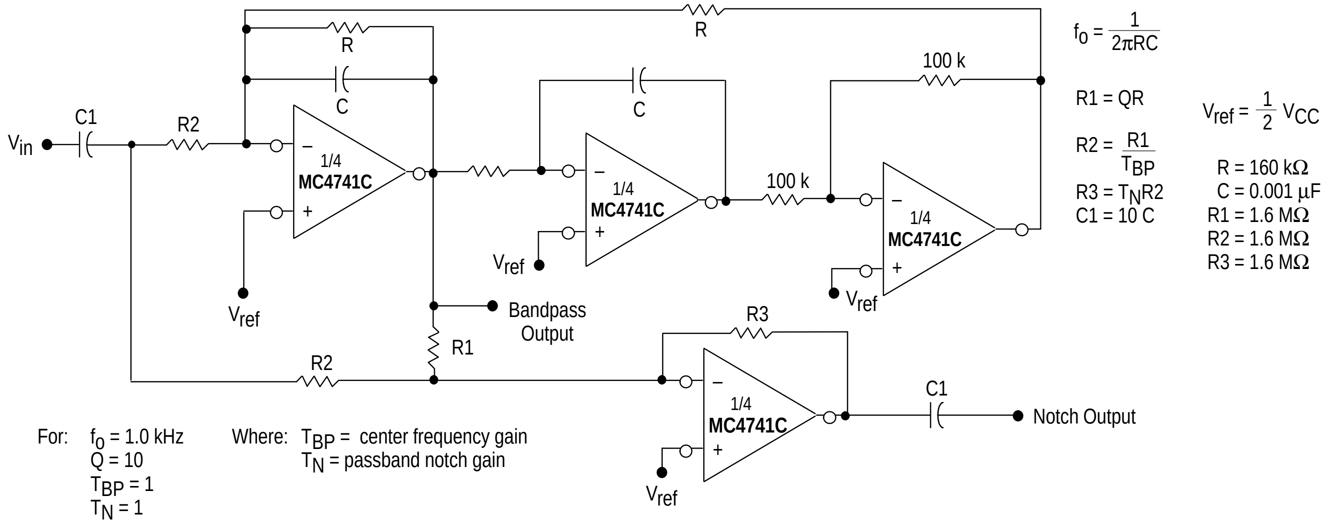


Figure 8. Open Loop Voltage Gain versus Supply Voltage

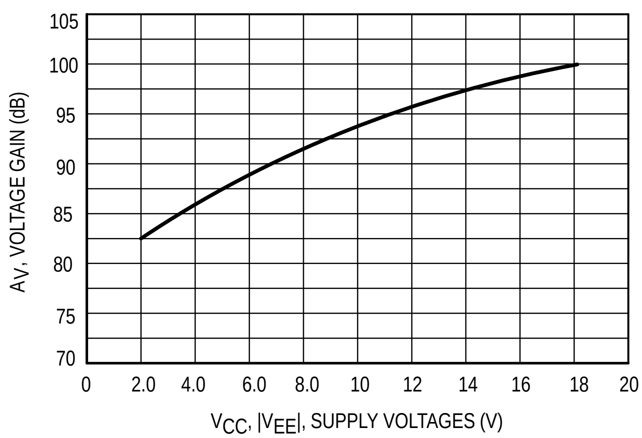


Figure 9. Transient Response Test Circuit

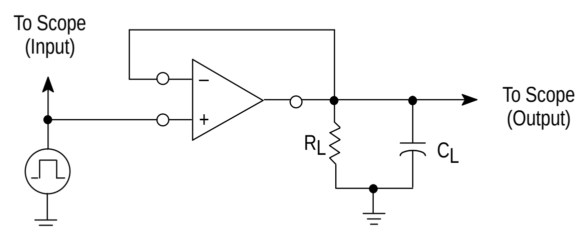
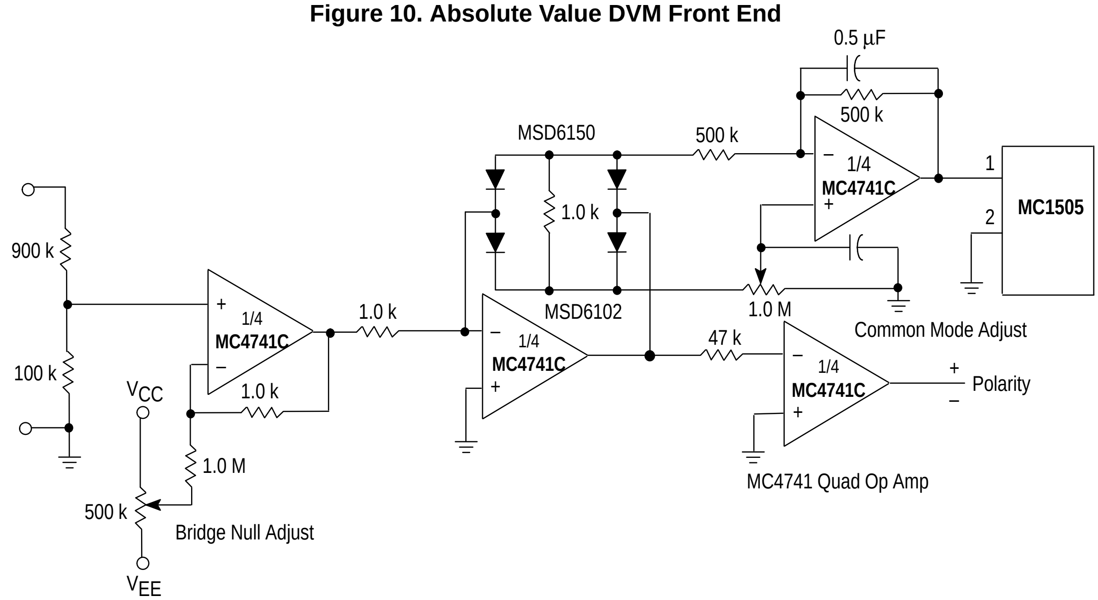
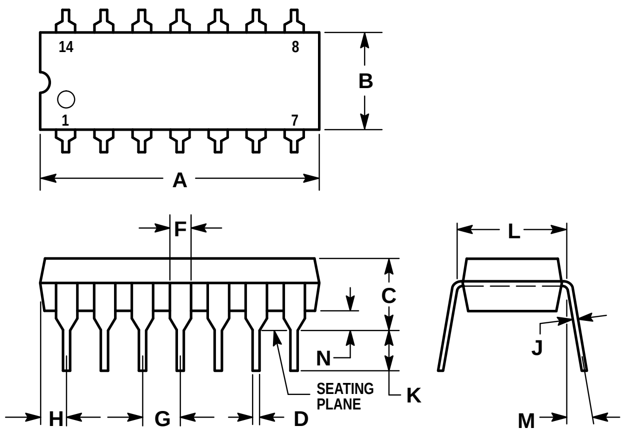


Figure 10. Absolute Value DVM Front End



OUTLINE DIMENSIONS

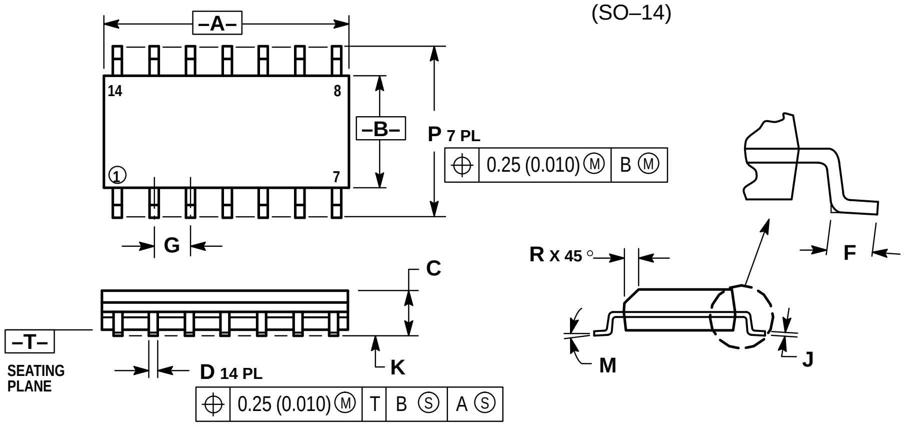
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
ISSUE F
(SO–14)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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