MOTOROLA

MC54/74F181

4-BIT ARITHMETIC LOGIC UNIT

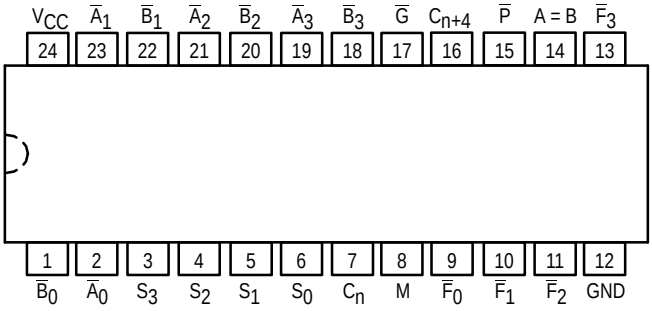
The MC54/74F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

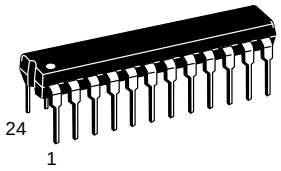
- Provides 16 Arithmetic Operations, ie, Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables, ie, Exclusive-OR, Compare, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Full Lookahead for High-Speed Arithmetic Operation on Long Words

4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL

CONNECTION DIAGRAM





N SUFFIX
PLASTIC
CASE 724-03

ORDERING INFORMATION

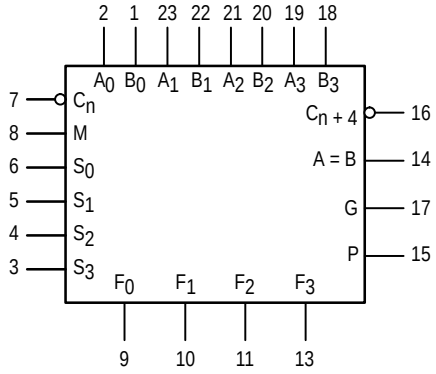
MC54/74FXXXN Plastic

GUARANTEED OPERATING RANGES

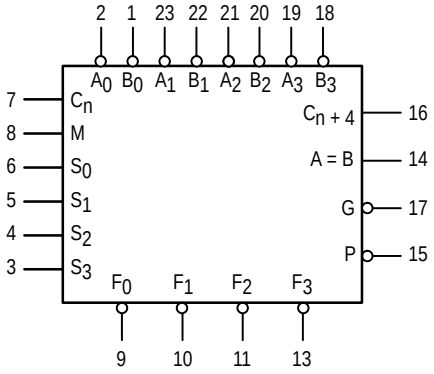
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–1.0	mA
V_{OH}	Output Voltage — High A = B output	54, 74			5.5	V
I_{OL}	Output Current — Low	54, 74			20	mA

LOGIC SYMBOLS

ACTIVE-HIGH OPERANDS

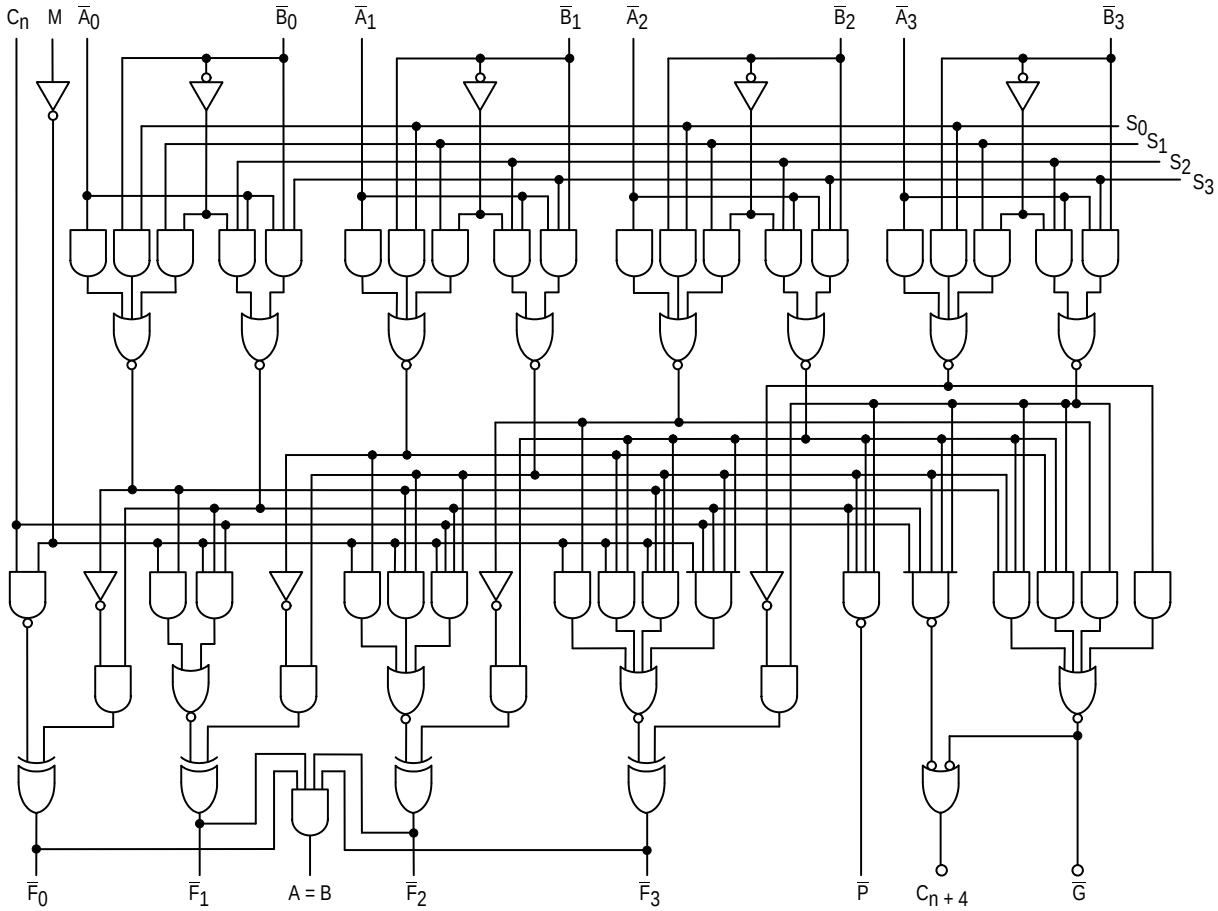


ACTIVE-LOW OPERANDS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
I_{OH}	Output Current — HIGH				250	µA	V_{OH} = 5.5 V	V_{CC} = MIN, A = B
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	M Input			–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
		A and B Inputs			–1.8	mA		
		S_{0-3} Inputs			–2.4	mA		
		C_n Input			–3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			43	65	mA	V_{CC} = MAX	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four F181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

AC CHARACTERISTICS

Symbol	Parameter Path	Mode	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	54/74F Max	54F T_A = −55 to +125°C, V_{CC} = 5.0 V ±10%, C_L = 50 pF Min	54F Max	74F T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%, C_L = 50 pF Min	74F Max	Unit
t_{PLH} t_{PHL}	C_n to C_{n+4}		3.0 3.0	8.5 8.0	3.0 3.0	10.5 10	3.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	A or B to C_{n+4}	Sum	5.0 5.0	13 12	5.0 5.0	15 14	5.0 5.0	14 13	ns
t_{PLH} t_{PHL}	A or B to C_{n+4}	Dif	5.0 5.0	14 13	5.0 5.0	16 15	5.0 5.0	15 14	ns
t_{PLH} t_{PHL}	C_n to F	Any	3.0 3.0	8.5 8.5	3.0 3.0	10.5 10.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Sum	3.0 3.0	7.5 7.5	3.0 3.0	9.5 9.5	3.0 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	A or B to G	Dif	3.0 3.0	8.5 9.5	3.0 3.0	10.5 11.5	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	A or B to P	Sum	3.0 3.0	7.0 7.5	3.0 3.0	9.0 9.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	A or B to P	Dif	4.0 3.5	7.5 8.5	4.0 3.5	9.5 10.5	4.0 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	A_i or B_i to F_i	Sum	3.0 3.0	9.0 10	3.0 3.0	11 11	3.0 3.0	10 10	ns
t_{PLH} t_{PHL}	A_i or B_i to F_i	Dif	3.0 3.0	11 11	3.0 3.0	13 13	3.0 3.0	12 12	ns
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0 4.0	10.5 10	4.0 4.0	12.5 12	4.0 4.0	11.5 11	ns
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	4.5 4.5	12 12	4.5 4.5	14 14	4.5 4.5	13 13	ns
t_{PLH} t_{PHL}	A or B to F	Logic	4.0 4.0	9.0 10	4.0 4.0	11 12	4.0 4.0	10 11	ns
t_{PLH} t_{PHL}	A or B to A = B	Dif	11 7.0	27 12.5	11 7.0	31 14.5	11 7.0	29 13.5	ns

FUNCTION TABLE

Mode Select Inputs				Active-LOW Operands & F_n Outputs		Active-HIGH Operands & F_n Outputs	
				Logic	**Arithmetic****	**Logic**	**Arithmetic****
S_3	S_2	S_1	S_0	**(M = H)**	**(M = L) (C_n = L)**	**(M = H)**	**(M = L) (C_n = H)**
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + $\overline{B}$
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{A\overline{B}}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	A$\overline{B}$ minus 1
H	L	L	L	$\overline{A}$B	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.

H = HIGH Voltage Level
L = LOW Voltage Level