

Dual 1-of-4 Decoder/ Demultiplexer

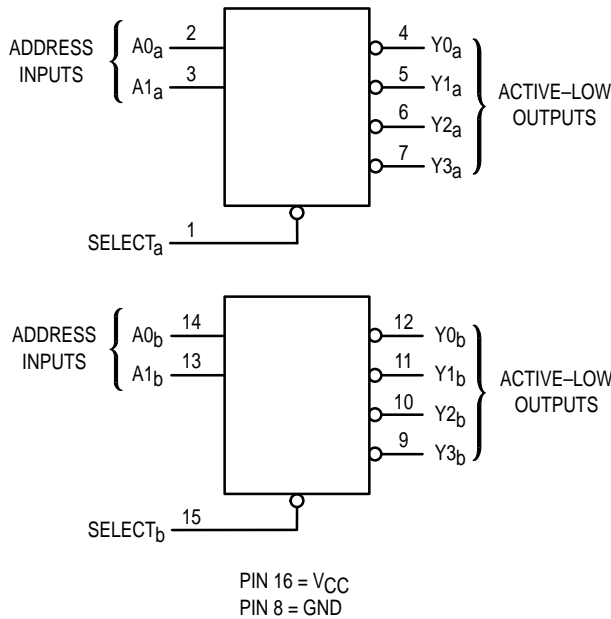
High-Performance Silicon-Gate CMOS

The MC54/74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

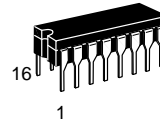
This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

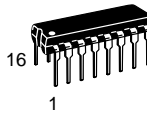
LOGIC DIAGRAM



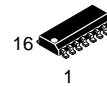
MC54/74HC139A



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC

PIN ASSIGNMENT

SELECT _a	1 •	16	V _{CC}
A0 _a	2	15	SELECT _b
A1 _a	3	14	A0 _b
Y0 _a	4	13	A1 _b
Y1 _a	5	12	Y0 _b
Y2 _a	6	11	Y1 _b
Y3 _a	7	10	Y2 _b
GND	8	9	Y3 _b

FUNCTION TABLE

Inputs		Outputs				
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 † Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
 Ceramic DIP: - 10 mW/°C from 100° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	3.98	3.84	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	0.26	0.33	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 1 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

CPD	Power Dissipation Capacitance (Per Decoder)*	Typical @ 25°C, VCC = 5.0 V	
		55	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

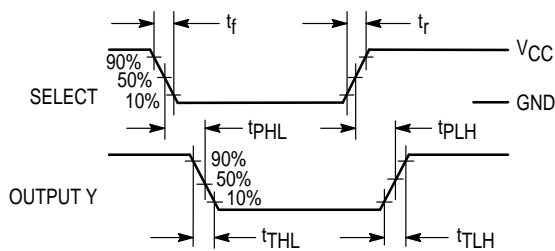


Figure 1.

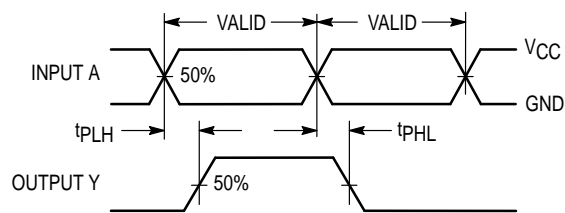
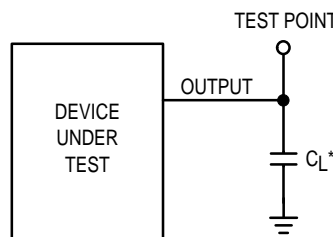


Figure 2.



* Includes all probe and jig capacitance

Figure 3. Test Circuit

PIN DESCRIPTIONS

ADDRESS INPUTS

A0_a, A1_a, A0_b, A1_b (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

CONTROL INPUTS

Select_a, Select_b (Pins 1, 15)

Active-low select inputs. For a low level on this input, the

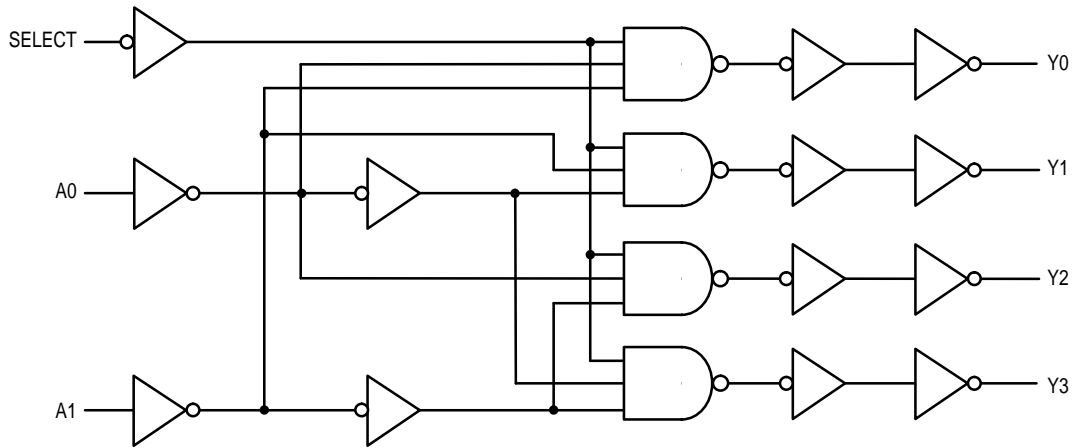
outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.


OUTPUTS

Y0_a – Y3_a, Y0_b – Y3_b (Pins 4 – 7, 12, 11, 10, 9)

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

**EXPANDED LOGIC DIAGRAM
(1/2 OF DEVICE)**



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