

14-Stage Binary Ripple Counter with Oscillator

High-Performance Silicon-Gate CMOS

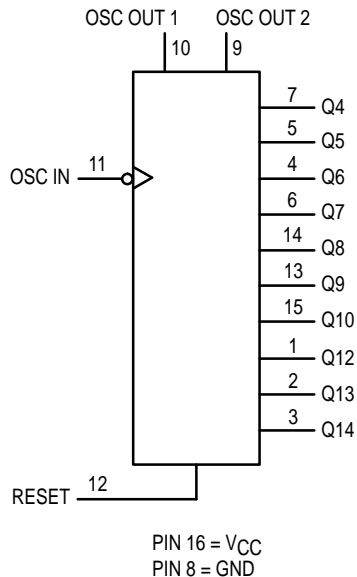
The MC54/74HC4060 is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next, and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during standby operation.

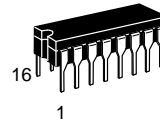
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may need to be gated with Osc Out 2 of the HC4060.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

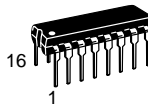
LOGIC DIAGRAM



MC54/74HC4060



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



DT SUFFIX
TSSOP PACKAGE
CASE 948F-01

ORDERING INFORMATION

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXDT	TSSOP

PIN ASSIGNMENT

Q12	1	16	V _{CC}
Q13	2	15	Q10
Q14	3	14	Q8
Q6	4	13	Q9
Q5	5	12	RESET
Q7	6	11	OSC IN
Q4	7	10	OSC OUT 1
GND	8	9	OSC OUT 2

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† TSSOP Package†	750 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or TSSOP Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 † Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
 Ceramic DIP: - 10 mW/°C from 100° to 125°C
 TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.5**	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

** The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14)	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	3.98	3.84	
V _{OL}	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	0.26	0.33	
			6.0	0.26	0.33	0.40	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (Continued)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{OH}	Minimum High-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{CC} or GND I _{out} ≤ 1.0 mA I _{out} ≤ 1.3 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{CC} or GND I _{out} ≤ 1.0 mA I _{out} ≤ 1.3 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	5.0	4.0	3.4	MHz
		4.5	25	20	17	
		6.0	29	24	20	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0	530	665	795	ns
		4.5	106	133	159	
		6.0	91	114	135	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0	1600	2000	2400	ns
		4.5	320	400	480	
		6.0	272	344	408	
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
 - Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- * For T_A = 25°C and C_L = 50 pF, typical propagation delay from Osc In to other Q outputs may be calculated with the following equations:
V_{CC} = 2.0 V: t_p = [205 + 107.5(N - 1)] ns
V_{CC} = 4.5 V: t_p = [41 + 21.5(N - 1)] ns
V_{CC} = 6.0 V: t_p = [35 + 18.3(N - 1)] ns

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		35	pF

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Osc In* (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Osc In (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

* Osc In driven with external clock.

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4–Q10, Q12–Q14 (Pins 7, 5, 4, 6, 14, 13, 15, 1, 2, 3)

Active-high outputs. Each QN output divides the oscillator frequency by 2^N . The user should note that Q1, Q2, Q3, and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 10, 9)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. (See Figures 4 and 5). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

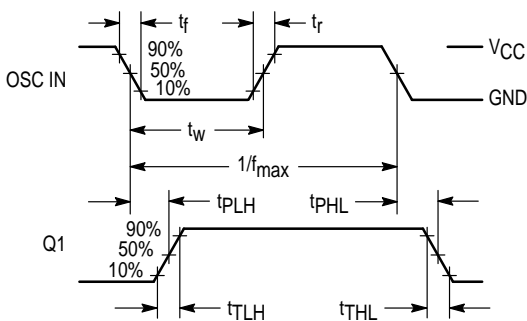


Figure 1.

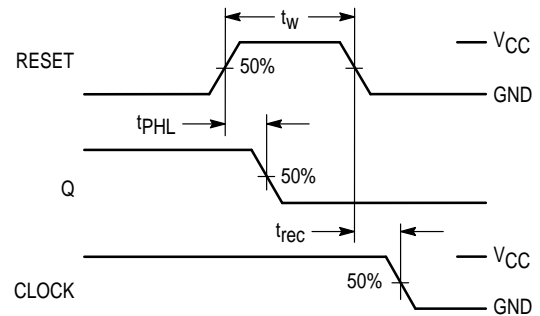


Figure 2.

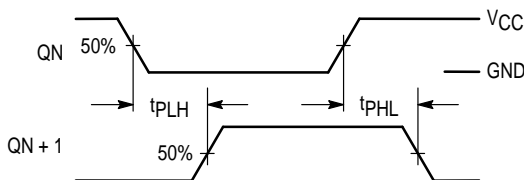
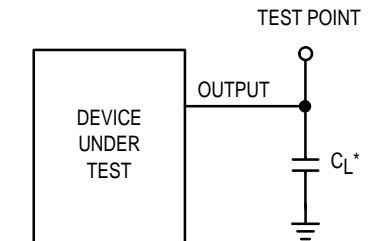


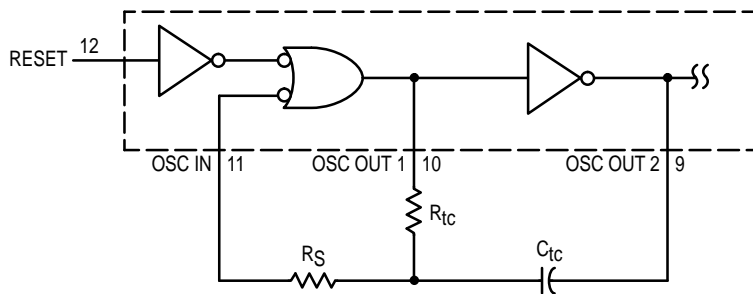
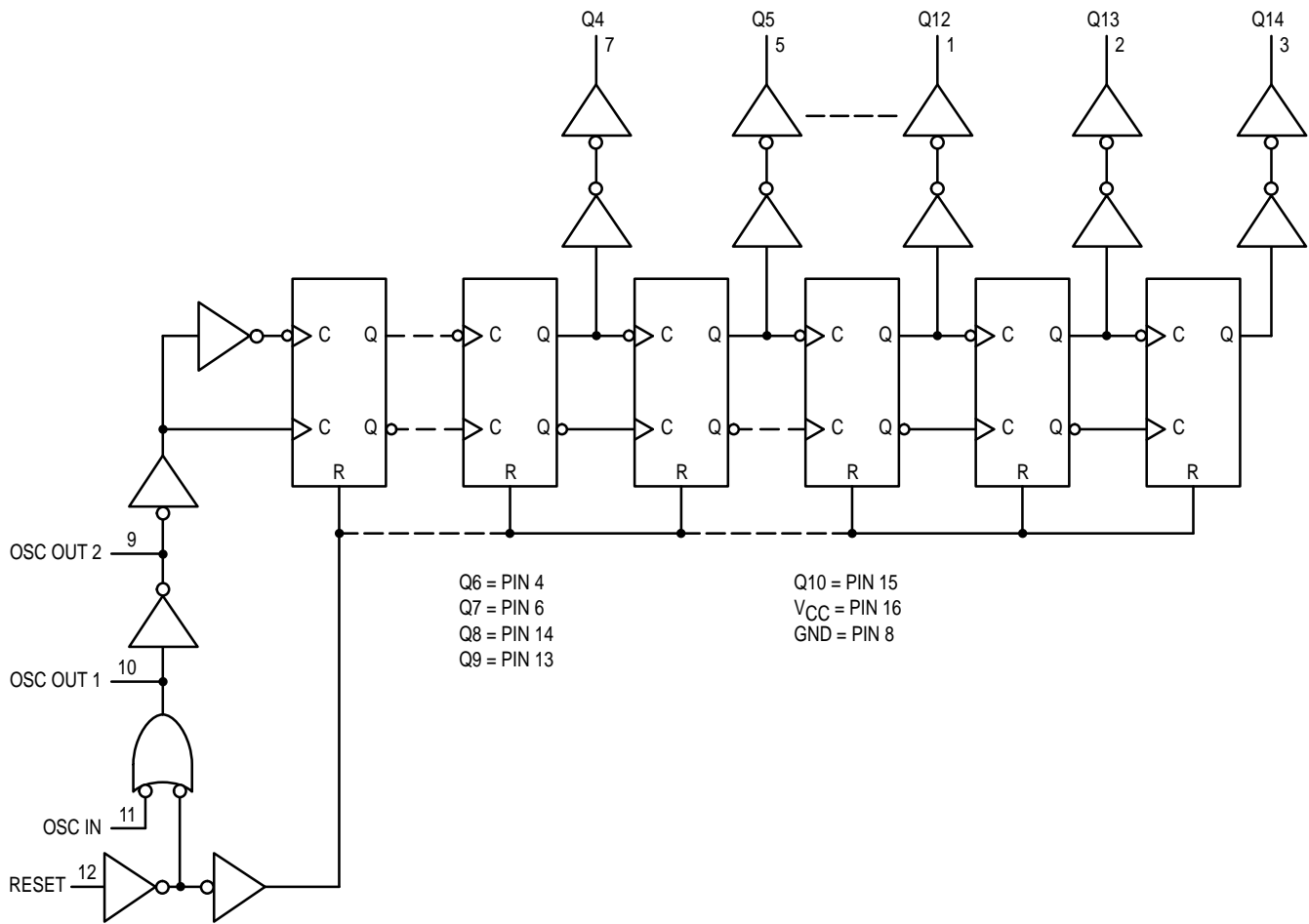
Figure 3.



* Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



For $2.0\text{ V} \leq V_{CC} \leq 6.0\text{ V}$
 $10 R_{tc} > R_S > 2 R_{tc}$
 $400\text{ Hz} \leq f \leq 400\text{ kHz}$

$$f \approx \frac{1}{3 R_{tc} C_{tc}} \quad (\text{f in Hz, } R_{tc} \text{ in ohms, } C_{tc} \text{ in farads})$$

The formula may vary for other frequencies.

Figure 5. Oscillator Circuit Using RC Configuration

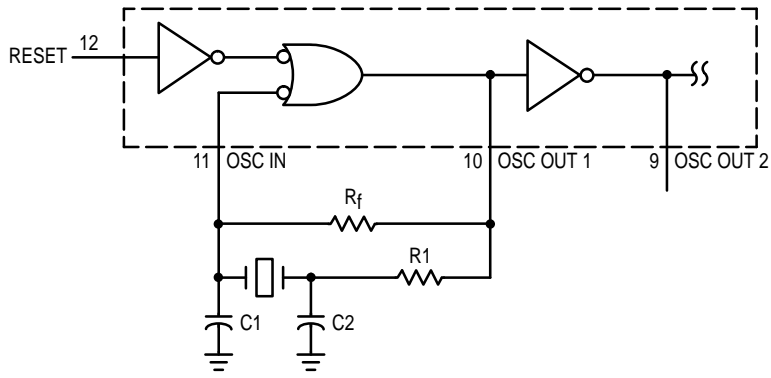


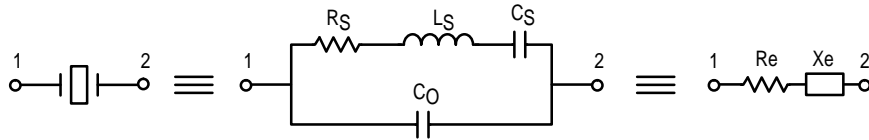
Figure 6. Pierce Crystal Oscillator Circuit

Table 1. Crystal Oscillator Amplifier Specifications

$T_A = 25^\circ\text{C}$ (Input = Pin 11, Output = Pin 10)

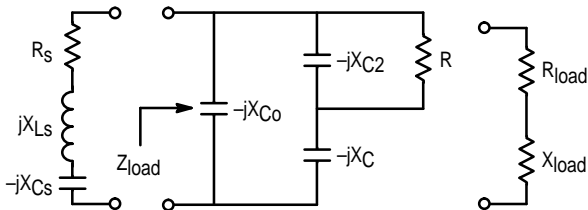
Type	Positive Reactance (Pierce)
Input Resistance, R_{in}	60 M Ω minimum
Output Impedance, Z_{out} (4.5 V supply)	200 Ω (see text)
Input Capacitance, C_{in}	5 pF typical
Output Capacitance, C_{out}	7 pF typical
Series Capacitance, C_a	5 pF typical
Open loop voltage gain with output at full swing, α	3 Vdc supply
	4 Vdc supply
	5 Vdc supply
	6 Vdc supply
	5.0 expected minimum
	4.0 expected minimum
	3.3 expected minimum
	3.1 expected minimum

PIERCE CRYSTAL OSCILLATOR DESIGN



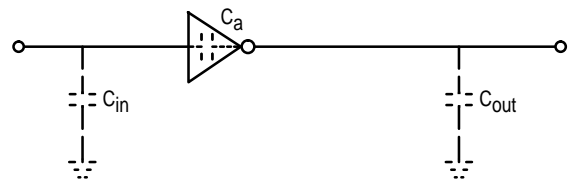
Values are supplied by crystal manufacturer (parallel resonant crystal)

Figure 7. Equivalent Crystal Networks



NOTE: $C = C_1 + C_{in}$ and $R = R_1 + R_{out}$. C_o is considered as part of the load. C_a and R_f typically have minimal effect below 2 MHz.

Figure 8. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 9. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R1. Above 2 MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f , and amplifier phase shift error from 180° .

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_s + jX_{L_s} - jX_{C_s})}{-jX_{C_0} + R_s + jX_{L_s} - jX_{C_s}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β , the attenuation, of the feedback network. For a closed-loop gain of 2, $A_v\beta = 2$, $\beta = 2/A_v$ where A_v is the gain of the HC4060 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load} . For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_0 L_s / Q) - R_s$ where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}(X_e - X_C)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (1)$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{C_{load}} \quad (\text{where the loading capacitor is an external load, not including } C_0) \quad (2)$$

$$R_{load} = \frac{R X_{C_0} X_{C2} [(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X_{C2}^2 (X_C + X_{C_0})^2 + R^2 (X_C + X_{C_0} + X_{C2})^2} \quad (3)$$

Here $R = R_{out} + R_1$. R_{out} is amp output resistance, R_1 is Z. The C corresponding to X_C is given by $C = C_1 + C_{in}$.

Alternately, pick a value for R_1 (i.e., let $R_1 = R_s$). Solve Equations 1 and 2 for C_1 and C_2 . Use Equation 3 and the fact that $Q = 2\pi f_0 L_s / (R_s + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R_1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R_1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R_1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R_1 .

SELECTING R_f

The feedback resistor, R_f , typically ranges up to 20 M Ω . R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as

the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

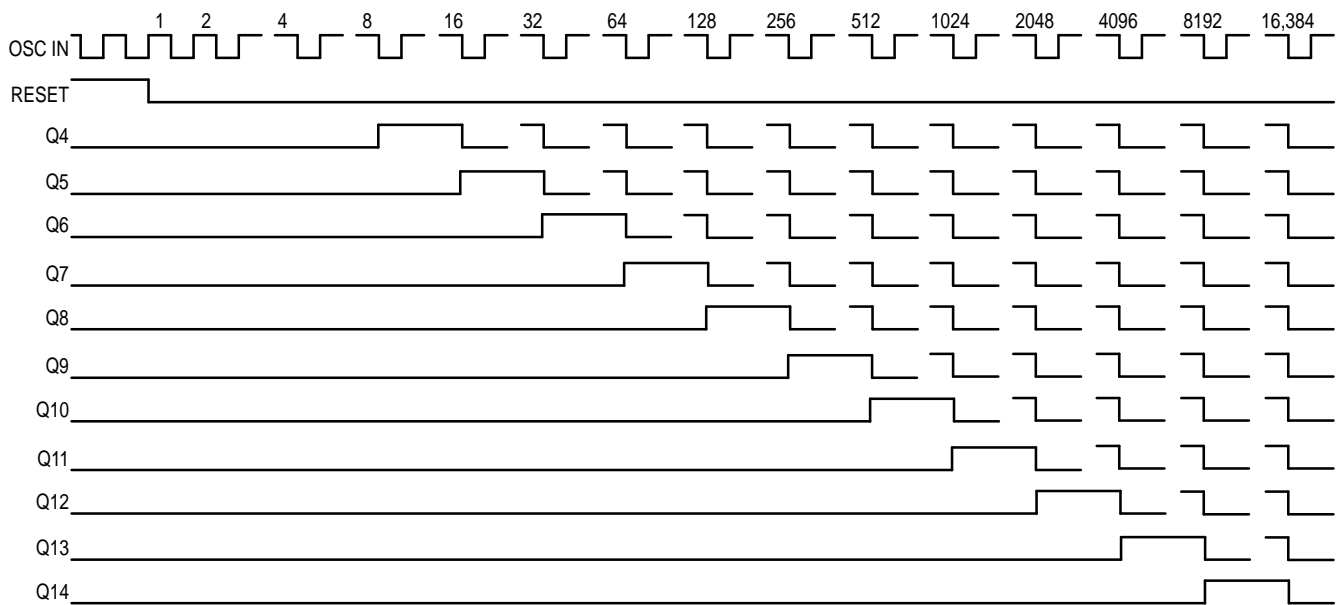
The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

- Technical Note TN-24, Statek Corp.
- Technical Note TN-7, Statek Corp.
- D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.
- D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

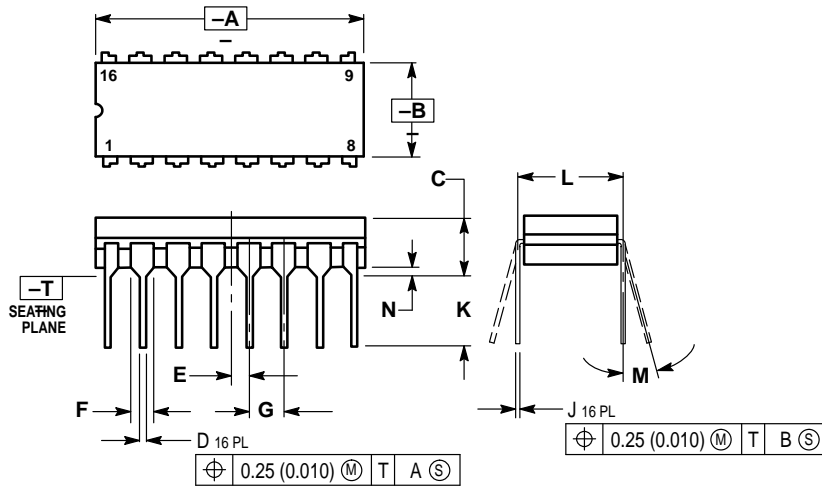
- E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb. 1969.
- D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.
- P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

TIMING DIAGRAM



OUTLINE DIMENSIONS

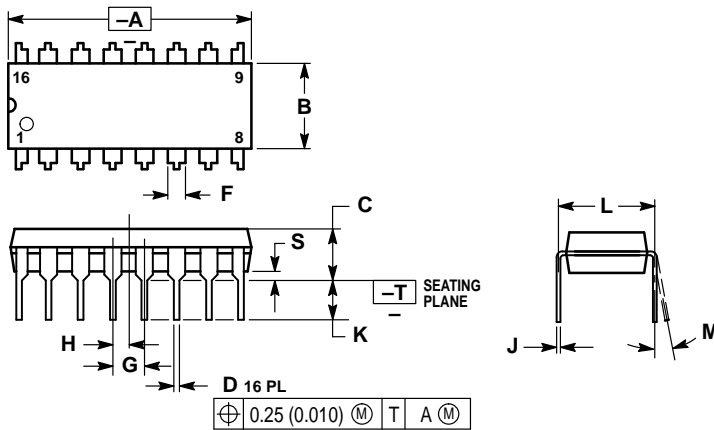
J SUFFIX
CERAMIC PACKAGE
 CASE 620-10
 ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

N SUFFIX
PLASTIC PACKAGE
 CASE 648-08
 ISSUE R

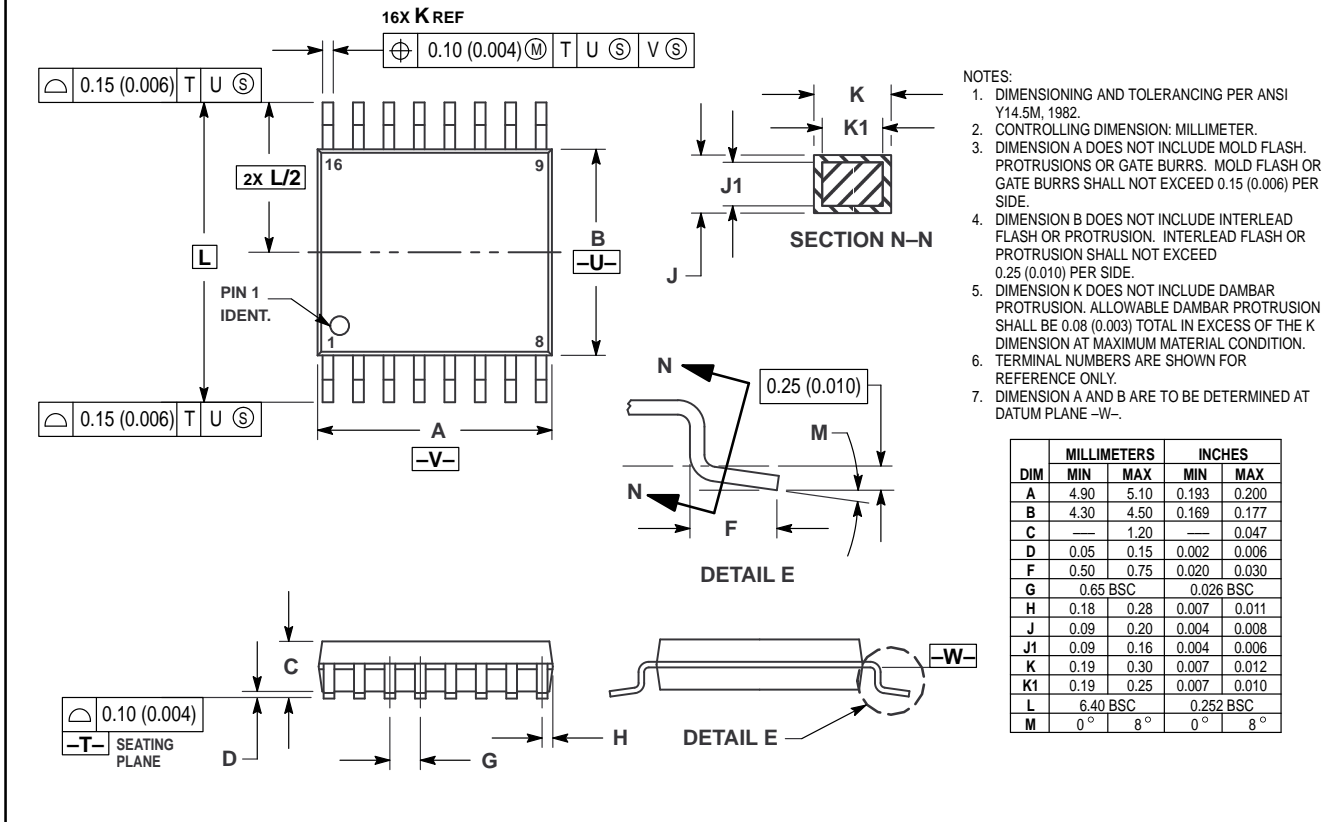


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948F-01
 ISSUE O



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