

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

T-46-09-05

MC54/74HC595A

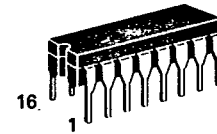
Advance Information
8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs
High-Performance Silicon-Gate CMOS

The MC54/74HC595A is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

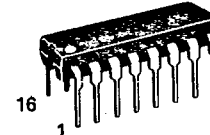
The HC595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595A directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
 - Improved Input Noise and Latchup Immunity



J SUFFIX CERAMIC CASE 620-09



N SUFFIX PLASTIC CASE 648-08

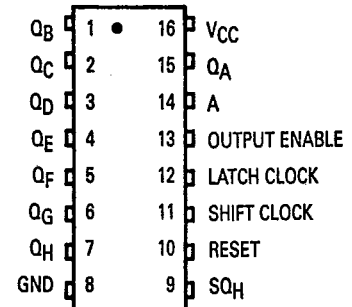


D SUFFIX SOIC CASE 751B-03

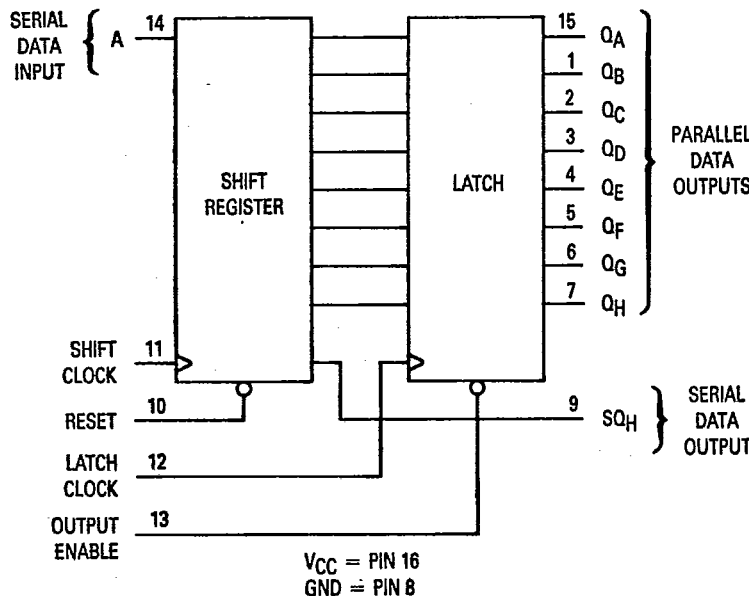
ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.



MOTOROLA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP SOIC Package	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage, Q _A -Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5	3.98	3.84	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage, Q _A -Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5	0.26	0.33	
6.0	0.26	0.33	0.4				

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{OH}	Minimum High-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current, Q _A -Q _H	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t _{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A -Q _H (Figures 3 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A -Q _H (Figures 3 and 7)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _{TLH} , t _{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A -Q _H	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P _D = CPD V _{CC} ² f + I _{CC} V _{CC}	Typical @ 25°C, V _{CC} = 5.0 V			pF
		300			

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t _{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5.0	5.0	5.0	ns
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
t _{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output S _{QH}	Parallel Outputs O _{A-QH}
Reset shift register	L	X	X	L, H,	L	L	U	L	U
Shift data into shift register	H	D		L, H,	L	D → S _{RA} ; S _{RN} → S _{RN} + 1	U	S _{RG} → S _{RH}	U
Shift register remains unchanged	H	X	L, H,	L, H,	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H,		L	U	S _{RN} → L _{RN}	U	S _{RN}
Latch register remains unchanged	X	X	X	L, H,	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high-impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents

D = data (L, H) logic level
U = remains unchanged

X = don't care
Z = high impedance

* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14) — Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11) — Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10) — Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12) — Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13) — Active-low Output Enable. A low on this input allows the data from the latches to be

presented at the outputs. A high on this input forces the outputs (QA-QH) into the high-impedance state. The serial output is not affected by this control unit.

3-state, latch outputs.

SQH (Pin 9) — Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

OUTPUTS

QA-QH (Pins 15, 1, 2, 3, 4, 5, 6, 7) — Noninverted,

SWITCHING WAVEFORMS

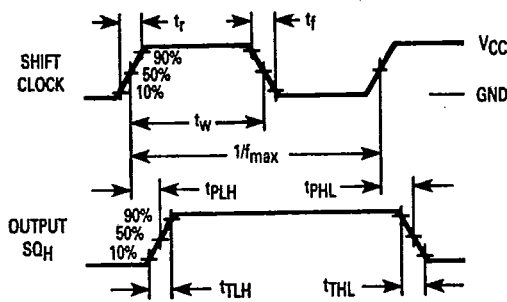


Figure 1

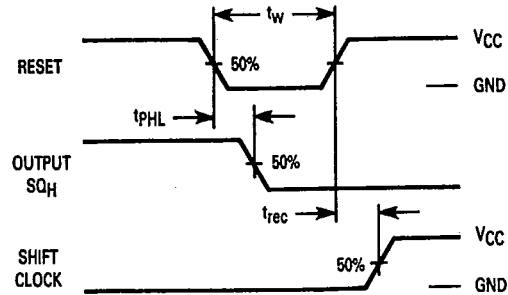


Figure 2

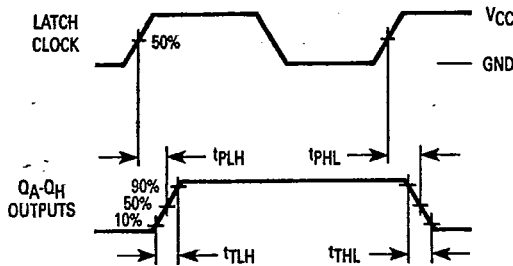


Figure 3

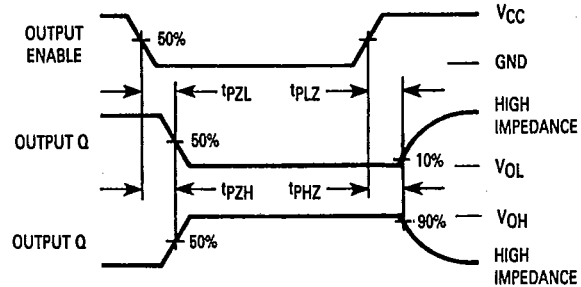


Figure 4

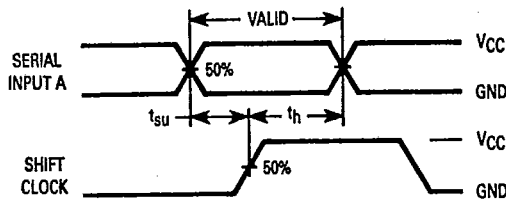


Figure 5

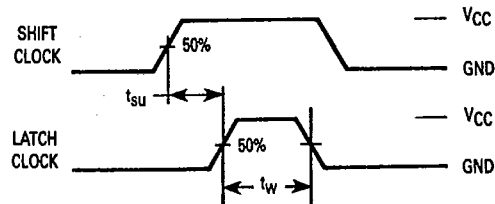
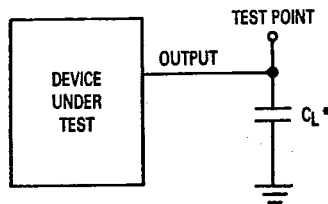
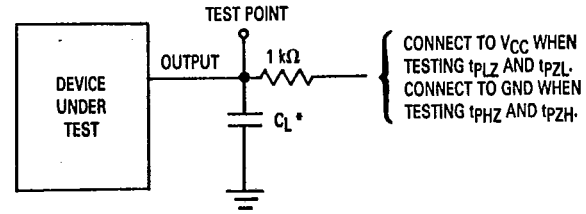


Figure 6



*Includes all probe and jig capacitance.

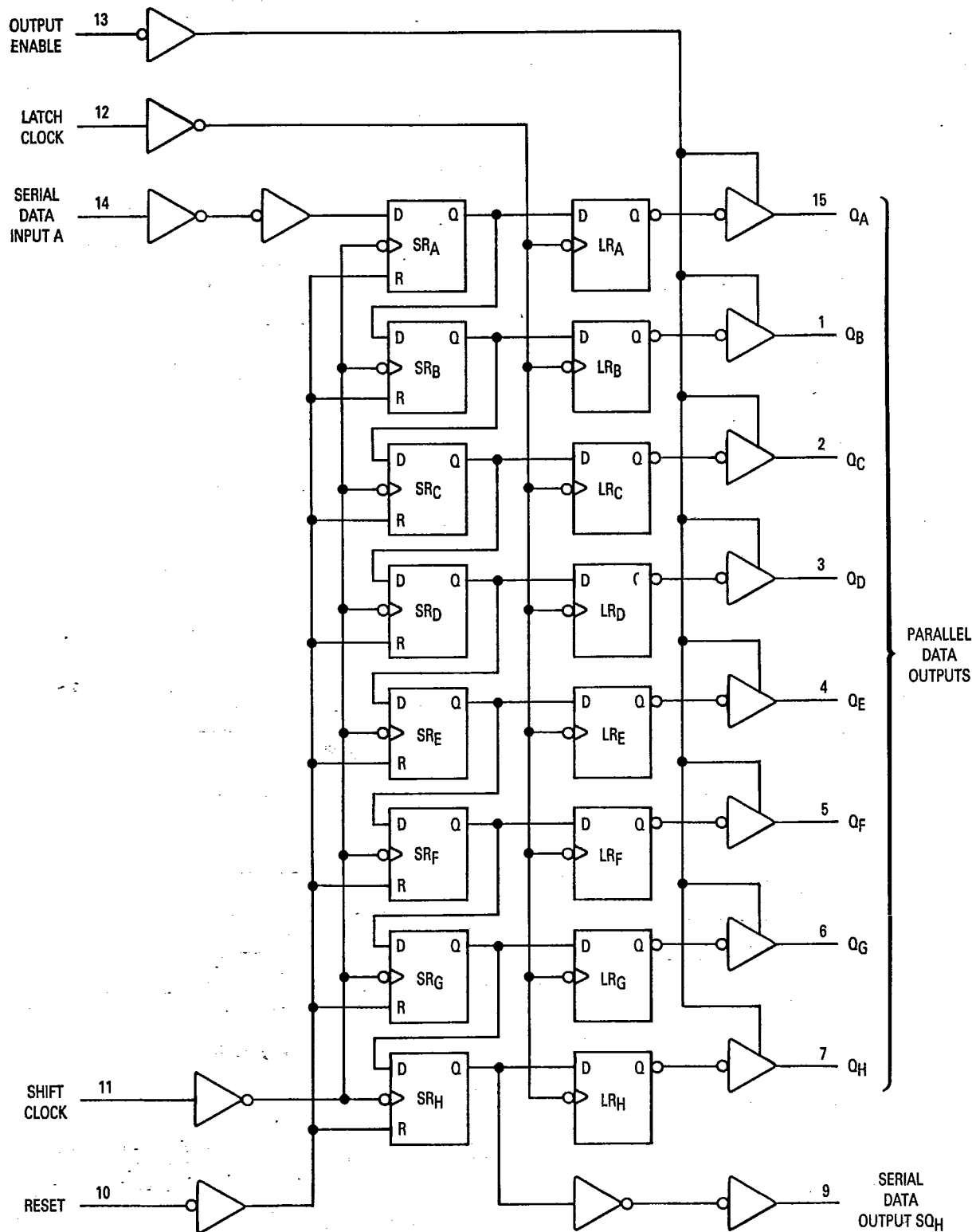
Figure 7. Test Circuit



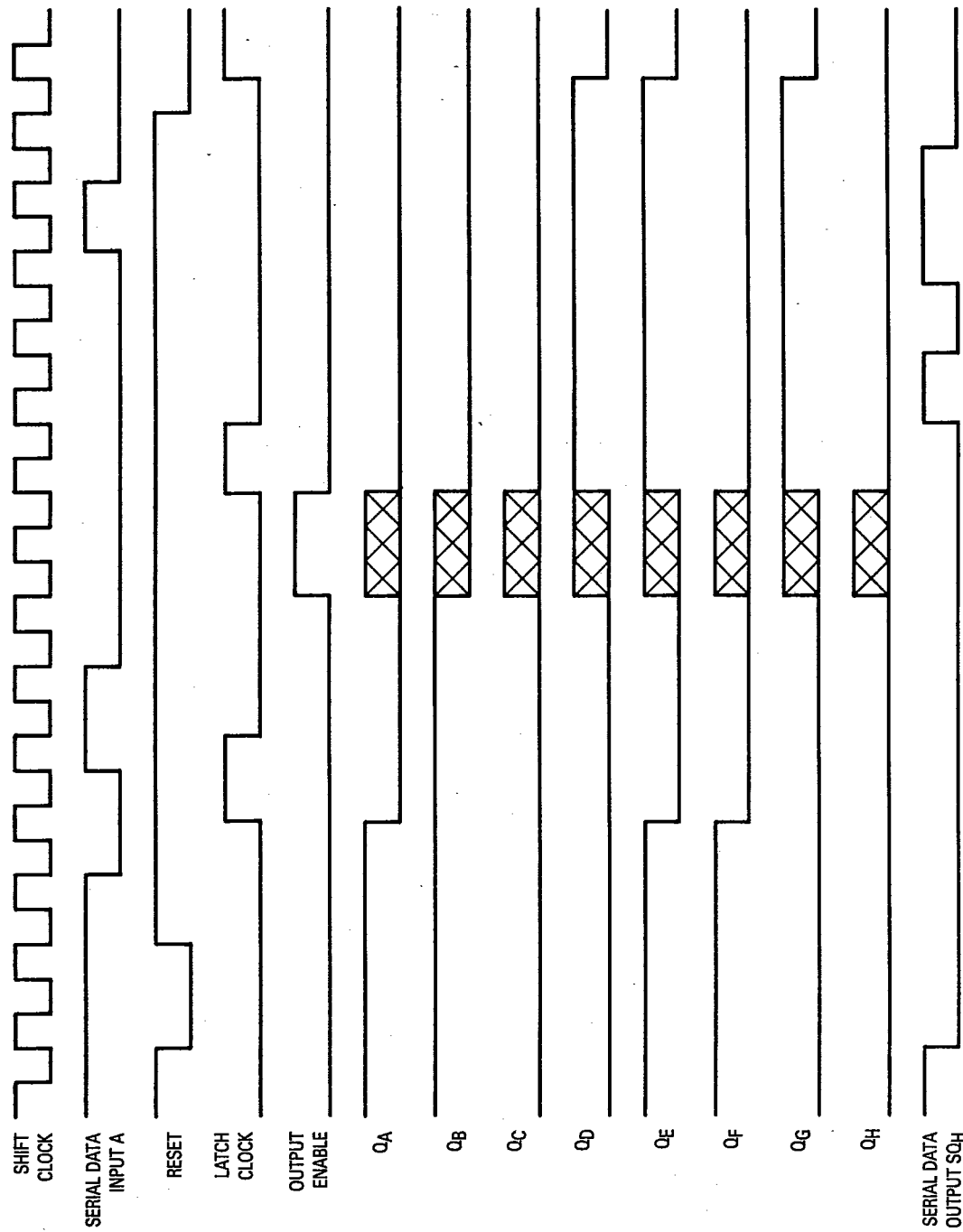
*Includes all probe and jig capacitance.

Figure 8. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



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OUTLINE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

**J SUFFIX
CERAMIC
CASE 620-09**

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**N SUFFIX
PLASTIC
CASE 648-08**

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**D SUFFIX
SOIC
CASE 751B-03**

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MOTOROLA

MC54/74HC595A