MC68340

Technical Summary

Integrated Processor Unit

The MC68340 is a 32-bit integrated processor unit, combining high-performance data manipulation with powerful peripheral subsystems. The MC68340 is a member of the M68300 Family of modular devices featuring fully static, high-speed complementary metal-oxide semiconductor (HCMOS) technology. Based on the powerful MC68000, the CPU32 central processing module provides enhanced system performance and uses the extensive software base of the M68000 Family. Figure 1 shows the major components of the MC68340.

The main features of the MC68340 are as follows:

- Integrated System Functions in a Single Chip
- 32-Bit M68000 Family Central Processor (CPU32)
  - — Upward Object-Code Compatible with the MC68000 and MC68010
  - — New Instructions for Controller Applications
  - — Higher Performance Execution
- Two-Channel DMA Capability for Low-Latency Memory Accesses
- Two Serial I/O Channels
- Two Multiple-Mode 16-Bit Timers
- Four Programmable Chip-Select Signals
- System Failure Protection:
  - — Software Watchdog Timer
  - — Periodic Interrupt Timer
  - — Spurious Interrupt, Double Bus Fault, and Bus Timeout Monitors
  - — Automatic Programmable Bus Termination
- Up to 16 Discrete I/O Pins
- Low-Power Operation
  - — HCMOS Technology Reduces Power in Normal Operation
  - — LPSTOP Mode Provides Static State for Lower Standby Drain

- Frequency: 16.78-MHz Maximum Frequency at 5-V Supply, Software Programmable
- Packages: 144-Pin Ceramic Quad Flat Pack (CQFP)
  145-Pin Plastic Pin Grid Array (PGA)

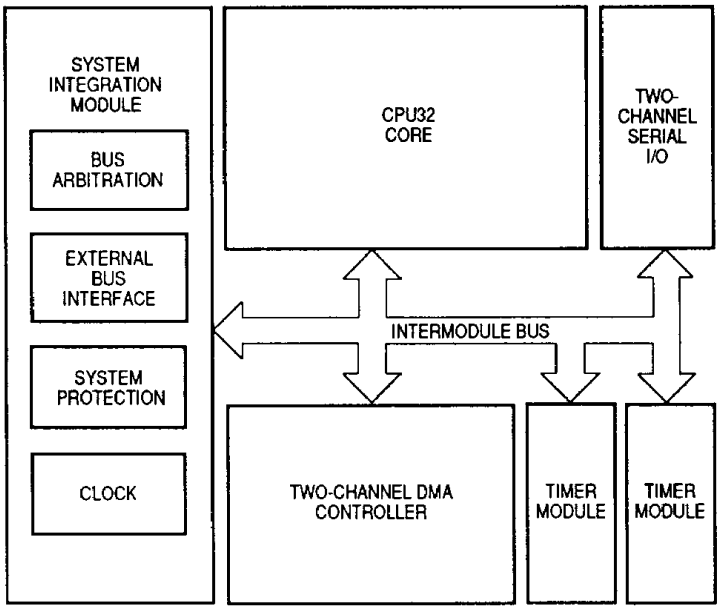


Figure 1. MC68340 Block Diagram

INTRODUCTION

The following paragraphs describe the capabilities of the MC68340 modules. The CPU32 provides the central processing capability; however, it is relieved of much overhead by the intelligent modules included in the MC68340. The system integration module (SIM) provides configuration control at system initialization, handles bus arbitration and the interface to external devices used with the MC68340, provides system protection, and allows software control of the clock speed. Four chip selects in the SIM enhance system integration for easy external memory or peripheral access. The direct memory access (DMA) controller provides two channels of single- or dual-address transfer capability. The serial module provides two channels of high-speed serial communications with synchronous and asynchronous protocols. The two timer modules, which are identical, can be externally cascaded. These modules are connected on-chip via an intermodule bus (IMB).

CPU32

The central processing unit (CPU) of the MC68340 is the CPU32, an upward-compatible M68000 Family member. All MC68010 and most MC68020 enhancements, such as virtual memory support, loop mode operation, instruction pipeline, and 32-bit mathematical operations, are supported. Powerful addressing modes provide compatibility with existing software programs and increase the efficiency of high-level language compilers. New instructions, such as table lookup and interpolate and low-power stop, support the specific requirements of controller applications. Most instructions can execute in one-half the number of clocks required by an MC68000, yielding an overall 1.6 times performance of the same-speed MC68000.

4 PROGRAMMING MODEL

The registers are partitioned into two levels of privilege: user and supervisor. User programs, executing in the user mode shown in Figure 2, can only use the resources of the user model. System software, executing in the supervisor mode shown in Figure 3, has unrestricted access to all processor resources.

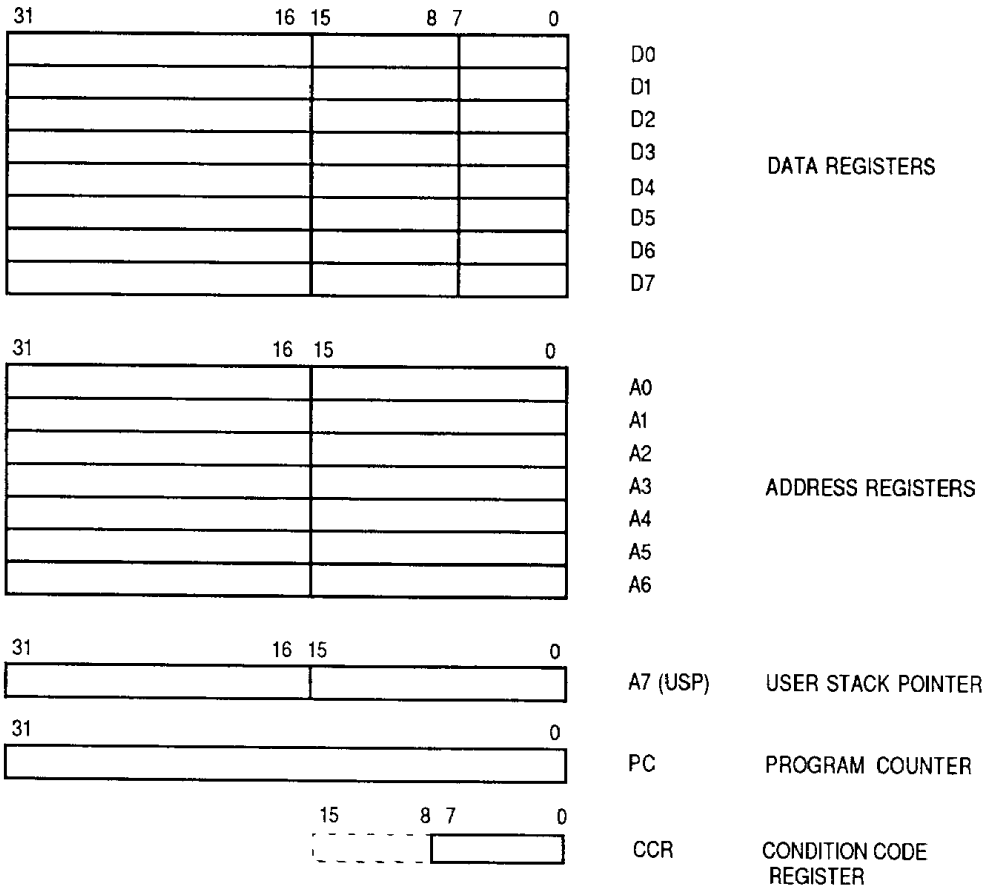


Figure 2. User Programming Model

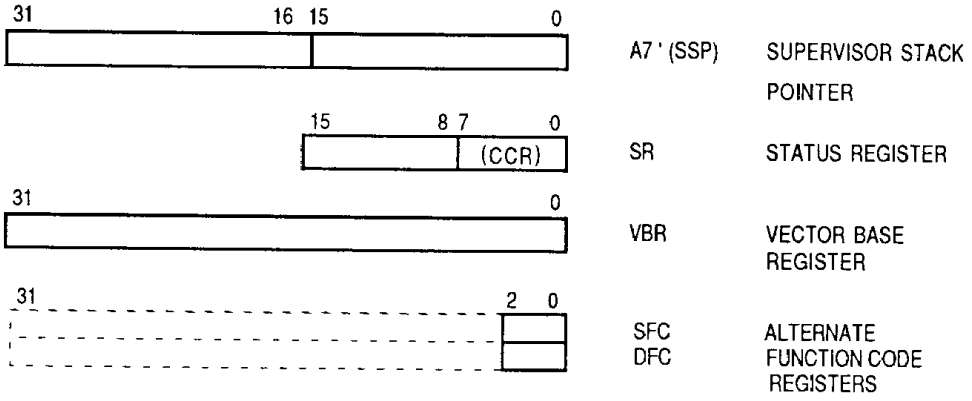


Figure 3. Supervisor Programming Model Supplement

The CPU32 addressing modes are listed in Table 1. The register indirect addressing modes support postincrement, predecrement, offset, and indexing, which are particularly useful for handling data structures common to sophisticated applications and high-level languages. The program counter indirect mode also has indexing and offset capabilities; this addressing mode is typically required to support position-independent software. In addition to these addressing modes, the CPU32 provides index sizing and scaling features that enhance software performance. Data formats are supported orthogonally by all arithmetic operations and by all appropriate addressing modes.

Table 1. Addressing Modes

Addressing Modes	Syntax
Register Direct	Rn
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect with Postincrement	(An)+
Address Register Indirect with Predecrement	-(An)
Address Register Indirect with Displacement	(d_{16},An)
Register Indirect with Index	
Address Register Indirect with Index (8-Bit Displacement)	(d_8,An,Xn)
Address Register Indirect with Index (Base Displacement)	(bd,An,Xn*SCALE)
Memory Indirect	
Memory Indirect Postindexed	([bd,An],Xn,od)
Memory Indirect Preindexed	([bd,An,Xn],od)
Program Counter Indirect with Displacement	(d_{16},PC)
Program Counter Indirect with Index	
PC Indirect with Index (8-Bit Displacement)	(d_8,PC,Xn)
PC Indirect with Index (Base Displacement)	(bd,PC,Xn*SCALE)
Program Counter Memory Indirect	
PC Memory Indirect Postindexed	([bd,PC],Xn,od)
PC Memory Indirect Preindexed	([bd,PC,Xn],od)
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Immediate	#<data>

NOTES:

Dn = Data Register, D0–D7
An = Address Register, A0–A7
d_8, d_{16} = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 (d_8) or 16 (d_{16}) bits; when omitted, assemblers use a value of zero.
Xn = Address or data register used as an index register; form is Xn.SIZE*SCALE, where SIZE is .W or .L (indicates index register size) and SCALE is 1, 2, 4, or 8 (index register is multiplied by SCALE); use of SIZE and/or SCALE is optional.
bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.
od = Outer displacement added as part of effective address calculation after any memory indirection; use is optional with a size of 16 or 32 bits.
PC = Progam Counter
<data> = Immediate value of 8, 16, or 32 bits
() = Effective Address
[] = Used as indirect address or long-word address.

INSTRUCTION SET OVERVIEW

The CPU32 instructions are listed in Table 2. The instruction set has been tailored to support high-level languages and is optimized for those instructions most commonly executed; however, all instructions listed are fully supported. Many instructions operate on bytes, words, and long words, and most instructions can use any of the addressing modes of Table 1.

Table 2. CPU32 Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BGND	Enter Background Mode
BKPT	Breakpoint
BRA	Branch Always
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit
CHK	Check Register against Bounds
CHK2	Check Register against Upper and Lower Bounds
CLR	Clear Operand
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LPSTOP	Low-Power Stop
LSL, LSR	Logical Shift Left and Right
MOVE	Move
MOVE CCR	Move Condition Code Register
MOVE SR	Move to/from Status Register
MOVE USP	Move User Stack Pointer
MOVEA	Move Address
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MOVEQ	Move Quick
MOVES	Move Alternate Address Space
MULS, MULS.L	Signed Multiply
MULU, MULU.L	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
NOT	Ones Complement
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return from Exception
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words

Table 2. CPU32 Instruction Set Summary (Continued)

Mnemonic	Description
TAS	Test Operand and Set
TBLS,TBLSN	Table Lookup and Interpolate (Signed)
TBLU, TBLUN	Table Lookup and Interpolate (Unsigned)
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink

OPERAND TRANSFER MECHANISM

The MC68340 external bus interface overlaps arbitration with data transfers. The bus is optimized to perform high-speed transfers to and from external memory and peripherals. The address bus is 32 bits wide, and the data bus is 16 bits wide.

The MC68340 architecture supports byte, word, and long-word operands, allowing access to 8- and 16-bit data ports through the use of asynchronous cycles controlled by the size outputs (SIZ1 and SIZ0) and data size acknowledge inputs ($\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$). The MC68340 architecture also supports 32-bit external single-address DMA transfers.

Dynamic bus sizing allows the programmer to write code that is not bus-width specific. Long-word accesses to peripherals can be used in code, but the bus transfers only the data width that the peripheral can utilize. A long-word access to an 8-bit peripheral results in four transfers to the peripheral. Dynamic bus sizing allows programmers to write code without knowing the peripheral port size; hardware designers can choose implementations independent of software.

Although the basic bus access time is three clock cycles, additional wait states can be inserted to provide for longer bus accesses. Also, the chip-select circuit fast-termination enable can provide a two-cycle external bus transfer for an external device that has a fast access time. Since the chip-select circuits are controlled by the system clock, the bus cycle termination is inherently synchronized with the system clock.

EXCEPTION PROCESSING

The CPU32 provides the same extensions to the exception stacking process as the MC68020. If the M-bit in the status register is set, the master stack pointer

is used for all task-related exceptions. When a nontask-related exception occurs (i.e., an interrupt), the M-bit is cleared, and the interrupt stack pointer is used. This feature allows a task's stack area to be carried within a single processor control block, and new tasks can be initiated by simply reloading the master stack pointer and setting the M-bit.

The externally generated exceptions are interrupts, bus errors, and reset conditions. The interrupts are requests for processor action from external devices, the bus error signals control bus access to allow recovery from error, and reset signals are used for processor initialization. The internally generated exceptions come from instructions, address errors, tracing, or breakpoints. The TRAP, TRAPcc, TRAPV, CHK, CHK2, RTE, and DIV instructions can generate exceptions as part of their instruction execution. Tracing behaves like a very high-priority, internally generated interrupt whenever it is processed. The other internally generated exceptions are caused by unimplemented floating-point instructions, illegal instructions, instruction fetches from odd addresses, and privilege violations.

Exception processing for the CPU32 occurs in the following sequence: 1) an internal copy is made of the status register, 2) the vector number of the exception is determined, 3) current processor status is saved, and 4) the exception vector offset is determined by multiplying the vector number by four. This offset is then added to the contents of the vector base register to determine the memory address of the exception vector. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

SYSTEM INTEGRATION MODULE

The MC68340 system integration module (SIM) consists of five submodules; four of these submodules control the system startup, initialization, configuration, and the external bus with a minimum of external devices. One additional submodule provides for boundary scan testing. The five submodules (see Figure 4) that make up the SIM are as follows:

- System Configuration and Protection
- Clock Synthesizer
- Chip Selects
- External Bus Interface
- IEEE 1149.1 Test Access Port

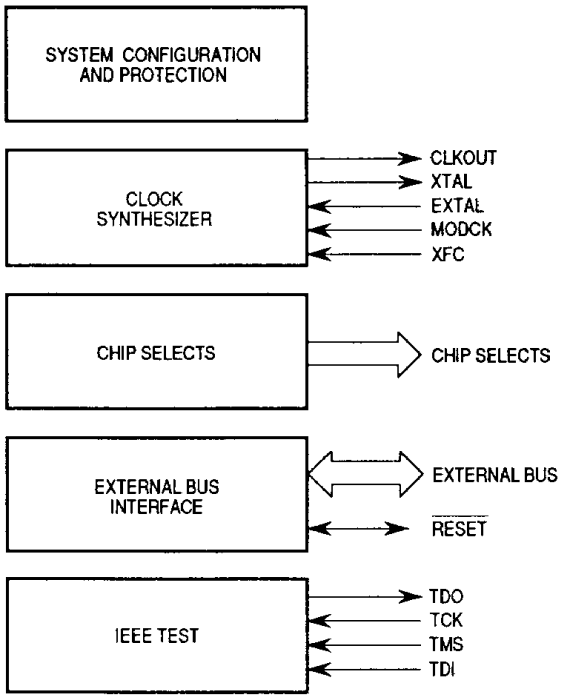


Figure 4. SIM Block Diagram

The system configuration and protection submodule controls system configuration and provides various monitors and timers, including the internal bus monitor, double bus fault monitor, spurious interrupt monitor, software watchdog timer, and the periodic interrupt timer. These system functions are integrated on the MC68340 to reduce board size and the cost incurred with external components.

The clock synthesizer generates the clock signals used by the SIM as well as other modules and external devices. A voltage-controlled oscillator (VCO) and phase-locked loop (PLL) can provide the 16.78-MHz clock (or a wide range of other frequencies, under software control) from an inexpensive watch crystal, or an external oscillator can be used to drive the clock input pin. The system speed can be changed dynamically with the PLL, providing either high performance or low power consumption under software control. With its fully static HCMOS design, it is possible to completely stop the system clock in software, and still preserve the contents of the registers.

The programmable chip-select submodule provides four chip-select signals that can enable external circuits, providing all handshaking and timing signals with up to 265-ns access times (at 16.78-MHz). Each chip-select signal has an associated base address register and an address mask register that contain the

programmable characteristics of that chip select. Block size is programmable from 256 bytes to the 4-Gbyte address capability in increments of 2n. Accesses can be preselected for either 8- or 16-bit transfers. One global chip select can be used to control an external memory device containing the initialization software for both the MC68340 and external system components.

The external bus interface (EBI) handles the transfer of information between the internal CPU and memory, peripherals, or other processing elements in the external address space. Based on the MC68020 bus, the external bus provides 32 address lines and 16 data lines. The data bus allows dynamic sizing between 8- and 16-bit data accesses. External bus arbitration is accomplished by a four-line handshaking interface. Transfers can be made in as little as two clock cycles.

The MC68340 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability.

Figure 5 shows the SIM register locations and the associated submodules (listed in the function column). The FC (function code) column indicates whether a register is restricted to supervisor access (S) or programmable to exist in either supervisor or user space (S/U).

ADDR	FC	15 — 8	7 — 0	
000	S	MODULE CONFIGURATION REGISTER (MCR)		SYSTEM PROTECTION
004	S	CLOCK SYNTHESIZER CONTROL REGISTER (SYNCR)		CLOCK
006	S	AUTOVECTOR REGISTER (AVR)	RESET STATUS REGISTER (RSR)	SYSTEM PROTECTION
010	S/U	RESERVED	PORT A DATA (PORTA)	EBI
012	S/U	RESERVED	PORT A DATA DIRECTION (DDRA)	EBI
014	S	RESERVED	PORT A PIN ASSIGNMENT 1 (PPRA1)	EBI
016	S	RESERVED	PORT A PIN ASSIGNMENT 2 (PPRA2)	EBI
018	S/U	RESERVED	PORT B DATA (PORTB)	EBI
01A	S/U	RESERVED	PORT B DATA (PORTB1)	EBI
01C	S/U	RESERVED	PORT B DATA DIRECTION (DDRB)	EBI
01E	S	RESERVED	PORT B PIN ASSIGNMENT (PPARB)	EBI
020	S	SW INTERRUPT VECTOR (SWIV)	SYSTEM PROTECTION CONTROL (SYPCR)	SYSTEM PROTECTION
022	S	PERIODIC INTERRUPT CONTROL REGISTER (PICR)		SYSTEM PROTECTION
024	S	PERIODIC INTERRUPT TIMING REGISTER (PITR)		SYSTEM PROTECTION
026	S	RESERVED	SOFTWARE SERVICE (SWSR)	SYSTEM PROTECTION
040	S	ADDRESS MASK 1 CS0		CHIP SELECT
042	S	ADDRESS MASK 2 CS0		CHIP SELECT
044	S	BASE ADDRESS 1 CS0		CHIP SELECT
046	S	BASE ADDRESS 2 CS0		CHIP SELECT
048	S	ADDRESS MASK 1 CS1		CHIP SELECT
04A	S	ADDRESS MASK 2 CS1		CHIP SELECT
04C	S	BASE ADDRESS 1 CS1		CHIP SELECT
04E	S	BASE ADDRESS 2 CS1		CHIP SELECT
050	S	ADDRESS MASK 1 CS2		CHIP SELECT
052	S	ADDRESS MASK 2 CS2		CHIP SELECT
054	S	BASE ADDRESS 1 CS2		CHIP SELECT
056	S	BASE ADDRESS 2 CS2		CHIP SELECT
058	S	ADDRESS MASK 1 CS3		CHIP SELECT
05A	S	ADDRESS MASK 2 CS3		CHIP SELECT
05C	S	BASE ADDRESS 1 CS3		CHIP SELECT
05E	S	BASE ADDRESS 2 CS3		CHIP SELECT

Figure 5. SIM Programming Model

DIRECT MEMORY ACCESS CONTROLLER

The DMA controller module provides low-latency transfer capability to an external peripheral or for memory-to-memory data transfer. The DMA, shown in a block diagram in Figure 6, provides two channels that allow operand transfers of bytes, words, or long words. These transfers can be either single or dual address and to either on-chip or off-chip devices. The features for these two channels are as follows:

- Two Independent DMA Channels with Full Programmability
- Single-Address Transfers with 32-Bit Address and 32-Bit Data Capability
- Dual-Address Transfers with 32-Bit Address and 16-Bit Data Capability
- Two 32-Bit Transfer Counters
- Four 32-Bit Address Pointers That Can Increment or Remain Constant
- Operand Packing and Unpacking for Dual-Address Transfers
- Supports All Bus-Termination Modes
- Provides Two-Clock-Cycle Internal Module Access
- Provides Full DMA Handshake for Cycle Steal and Burst Transfers

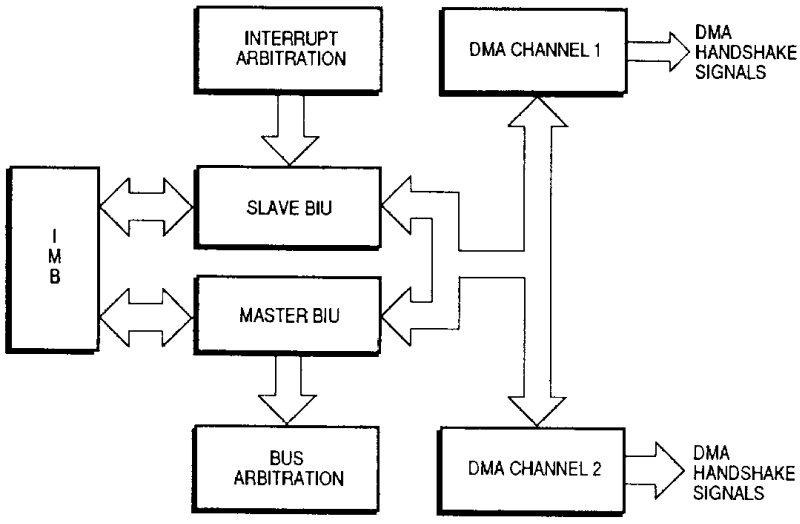


Figure 6. DMA Block Diagram

The DMA module consists of two, independent, programmable channels. In dual-address mode, a channel supports 32 bits of address and 16 bits of data. In single-address mode, a channel supports 32 bits of address and 32 bits of

data. In single-address mode, the DMA provides address and control signals during a single-ended transfer. The requesting device either sends or receives data to or from the specified address. In dual-address mode, two bus transfers occur, one from a source device and the other to a destination device. In dual-address mode, operands are packed or unpacked according to port sizes and addresses.

Each channel has an independent request, acknowledge, and done indication. The request mode can be internal, with four adjustable bus bandwidths, or external, with edge or level trigger. The DMA module can sustain a transfer rate of 33.3 Mbytes per second in single-address mode and nearly 8.4 Mbytes per second in dual-address mode.

Figure 7 shows a programming model (register map) of all registers in the DMA. Each channel has an independent set of registers located at the specified offset from the base address (listed in the address columns). The base address is specified in the SIM base address register. The FC column indicates whether a register is restricted to supervisor access (S) or programmable to exist in either supervisor or user space (S/U).

Unimplemented memory locations return logic zero when accessed. All registers support both byte and word transfers.

ADDRESS CH1	ADDRESS CH2	FC	15 — 8	7 — 0
780	7A0	S	MODULE CONFIGURATION REGISTER (MCR)	
782	7A2	S	RESERVED	
784	7A4	S	INTERRUPT REGISTER	
786	7A6	S/U	RESERVED	
788	7A8	S/U	CHANNEL CONTROL REGISTER	
78A	7AA	S/U	CHANNEL STATUS REGISTER	FUNCTION CODE REGISTER
78C	7AC	S/U	SOURCE ADDRESS REGISTER MSBs	
78E	7AE	S/U	SOURCE ADDRESS REGISTER LSBs	
790	7B0	S/U	DESTINATION ADDRESS REGISTER MSBs	
792	7B2	S/U	DESTINATION ADDRESS REGISTER LSBs	
794	7B4	S/U	BYTE TRANSFER COUNTER MSBs	
796	7B6	S/U	BYTE TRANSFER COUNTER LSBs	
798	7B8	S/U	RESERVED	
79A	7BA	S/U	RESERVED	
79C	7BC	S/U	RESERVED	
79E	7BE	S/U	RESERVED	

Figure 7. DMA Programming Model

SERIAL MODULE

The MC68340 serial module is a dual universal asynchronous/synchronous receiver/transmitter that interfaces directly to the CPU32 via an IMB. The serial module (see Figure 8) consists of the following major functional areas:

- Two Independent Serial Communication Channels
- Baud Rate Generator Logic
- Internal Channel Control Logic
- Interrupt Control Logic
- External and Internal Signal Interfaces

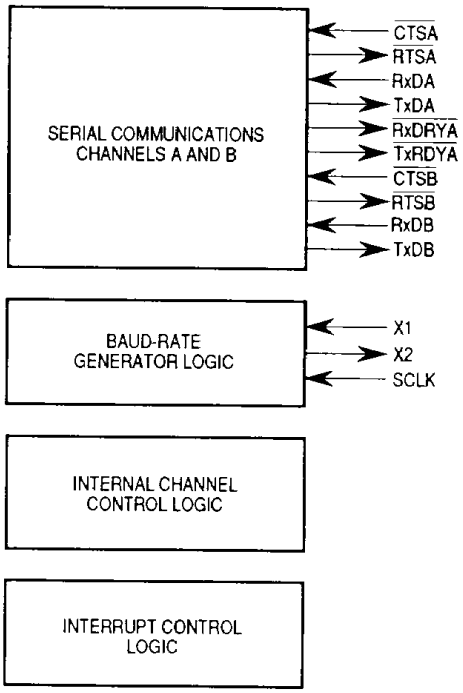


Figure 8. Serial Module Block Diagram

Features of the serial module are as follows:

- CPU32 IMB Submodule
- Two, Independent, Full-Duplex Asynchronous/Synchronous Receiver/Transmitter Channels
- User-Code Compatible with MC2681

- Maximum Data Transfer:
  - — 1× — 3 Mbps
  - — 16× — 188 kbps
- Quadruple-Buffered Receiver
- Double-Buffered Transmitter
- Independently Programmable Baud Rate for Each Receiver and Transmitter Selectable from:
  - — 19 Fixed Rates: 50 to 76.8k Baud
  - — External 1× Clock or 16× Clock
- Programmable Data Format:
  - — Five to Eight Data Bits Plus Parity
  - — Odd, Even, No Parity, or Force Parity
  - — One, One and One-Half, or Two Stop Bits Programmable in One-Sixteenth Bit Increments
- Programmable Channel Modes:
  - — Normal (Full Duplex)
  - — Automatic Echo
  - — Local Loopback
  - — Remote Loopback
- Automatic Wakeup Mode for Multidrop Applications
- Seven Maskable Interrupt Conditions
- Parity, Framing, and Overrun Error Detection
- False-Start Bit Detection
- Line-Break Detection and Generation
- Detection of Breaks Originating in the Middle of a Character
- Start-End Break Interrupt/Status
- On-Chip Crystal Oscillator
- TTL Compatibility

Each communication channel provides a full-duplex asynchronous/synchronous receiver and transmitter using an operating frequency independently selected from a baud rate generator or an external clock input. The transmitter accepts parallel data from the IMB, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits, then outputs a composite serial data stream on the TxD channel. The receiver accepts serial data on the RxD channel, converts it to parallel format, checks for a start bit, stop bit, parity (if any), or break condition, and transfers the assembled character onto the IMB during read operations.

Figure 9 shows a programming model (register map) of all registers in the serial module. The registers are located at the specified offset (listed in the address column) from the base address. The base address is specified in the SIM base address register. Unimplemented memory locations return logic zero when accessed. All registers support both byte and word transfers.

ADDRESS	FC	REGISTER READ (R/W = 1)	REGISTER WRITE (R/W = 0)
700	S[1]	MCR (HIGH BYTE)	MCR (HIGH BYTE)
701	S	MCR (LOW BYTE)	MCR (LOW BYTE)
702	S	DO NOT ACCESS[3]	DO NOT ACCESS[3]
703	S	DO NOT ACCESS[3]	DO NOT ACCESS[3]
704	S	INTERRUPT LEVEL (ILR)	INTERRUPT LEVEL (ILR)
705	S	INTERRUPT VECTOR (IVR)	INTERRUPT VECTOR (IVR)
710	S/U[2]	MODE REGISTER MR1A	MODE REGISTER MR1A
711	S/U	STATUS REGISTER A (SRA)	CLOCK-SELECT REGISTER A (CSRA)
712	S/U	DO NOT ACCESS[3]	COMMAND REGISTER A (CRA)
713	S/U	RECEIVER BUFFER A (RBA)	TRANSMITTER BUFFER A (TBA)
714	S/U	INPUT PORT CHANGE REGISTER (IPCR)	AUXILIARY CONTROL REGISTER (ACR)
715	S/U	INTERRUPT STATUS REGISTER (ISR)	INTERRUPT ENABLE REGISTER (IER)
716	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
717	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
718	S/U	MODE REGISTER MR1B	MODE REGISTER MR1B
719	S/U	STATUS REGISTER B (SRB)	CLOCK SELECT REGISTER B (CSRB)
71A	S/U	DO NOT ACCESS[3]	COMMAND REGISTER B (CRB)
71B	S/U	RECEIVER BUFFER B (RBB)	TRANSMITTER BUFFER B (TBB)
71C	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
71D	S/U	INPUT PORT REGISTER (IP)	OUTPUT PORT CONTROL REGISTER (OPCR)
71E	S/U	DO NOT ACCESS[3]	OUTPUT PORT (OP)[4] BIT SET
71F	S/U	DO NOT ACCESS[3]	OUTPUT PORT (OP)[4] BIT RESET
720	S/U	MODE REGISTER MR2A	MODE REGISTER MR2A
721	S/U	MODE REGISTER MR2B	MODE REGISTER MR2B

NOTES:
1. S — Register permanently defined as supervisor-only access
2. S/U — Register programmable as either supervisor or user access
3. A read or write to these locations currently has no effect.
4. Address-triggered commands

Figure 9. Serial Module Programming Model

TIMERS

Each MC68340 timer module contains a counter/timer (timer 1 and timer 2). Each timer interfaces directly to the CPU32 via an IMB. Each timer (see Figure 10) consists of the following major functional areas:

- A General-Purpose Counter/Timer
- Internal Control Logic
- Interrupt Control Logic
- External and Internal Signal Interfaces
- Versatile General-Purpose Timer
- 8-Bit Prescaler/16-Bit Counter
- Timers Can Be Externally Cascaded for a Maximum Count Width of 48 Bits
- Programmable Timer Modes:
  - — Event Counting
  - — Period and Pulse-Width Measurement
  - — Input Capture
  - — Output Compare
  - — Waveform Generation
  - — Pulse Generation
- Seven Maskable Interrupt Conditions Based on Programmable Events

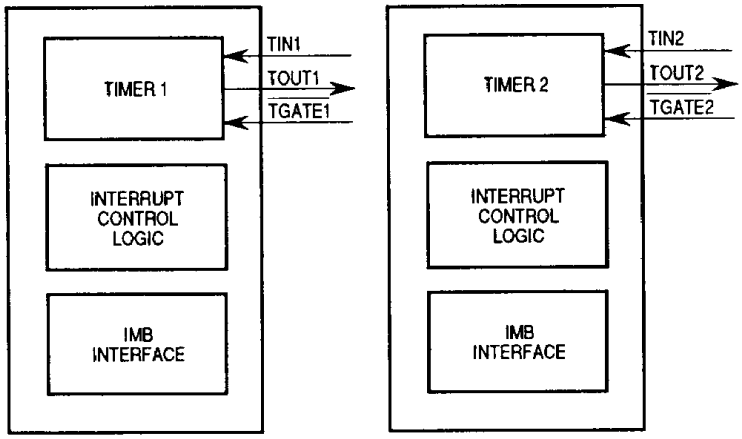


Figure 10. Timer Block Diagram

The timer can perform virtually any application traditionally assigned to timers and counters. The timer can be used to generate precisely timed events that are independent of the timing errors to which real-time programmed microprocessors are susceptible; for example, dynamic memory refreshing, DMA cycle steals, and interrupt servicing.

The timer has several functional areas: an 8-bit countdown prescaler, a 16-bit countdown counter, timeout logic, compare logic, and clock selection logic.

Figure 11 is a programming model (register map) of all registers in the timer module. The registers are located at the specified offset from the base address (listed in the address columns). The base address is specified in the SIM base address register. The FC column indicates whether a register is restricted to supervisor access (S) or programmable to exist in either supervisor or user space (S/U).

Unimplemented memory locations return logic zero when accessed. All registers support both byte and word transfers.

TIMER 1	TIMER 2	FC	15 — 0
$600	$640	S	MODULE CONFIGURATION REGISTER (MCR)
$602	$642	S	RESERVED
$604	$644	S	INTERRUPT REGISTER (IR)
$606	$646	S/U	CONTROL REGISTER (CR)
$608	$648	S/U	STATUS/PRESCALER REGISTER (SR)
$60A	$64A	S/U	COUNTER REGISTER (CNTR)
$60C	$64C	S/U	PRELOAD 1 REGISTER (PREL1)
$60E	$64E	S/U	PRELOAD 2 REGISTER (PREL2)
$610	$650	S/U	COMPARE REGISTER (COM)
$612–$63F	$652–$67F	S/U	RESERVED

Figure 11. Timer Module Programing Model

SIGNAL DESCRIPTION

Figure 12 illustrates the functional signal groups, and Table 4 lists the input and output signals for the MC68340. The test signals, TMS, TCK, TDI, and TDO, comply with subset 1149.1 of the IEEE standard.

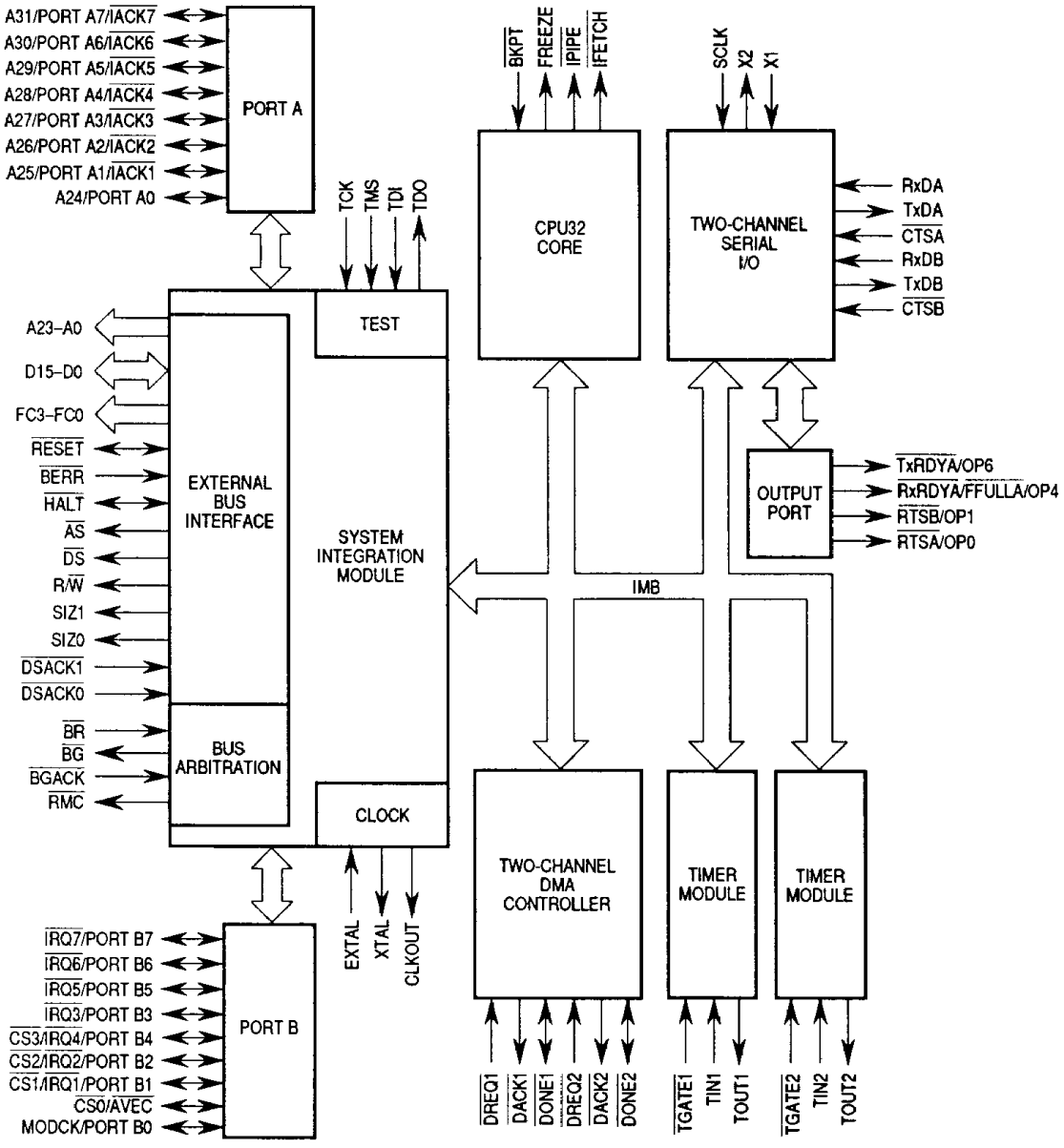


Figure 12. Functional Signal Groups

Table 4. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A23–A0	Lower 24 bits of address bus
Address Bus/Port A7–A0/$\overline{IACK7}$–$\overline{IACK1}$	A31–A24	Upper eight bits of address bus, parallel I/O port, or interrupt acknowledge lines
Data Bus	D15–D0	16-bit data bus used to transfer byte or word data
Function Codes	FC3–FC0	Identifies the processor state and the address space of the current bus cycle
Chip Select/$\overline{IRQ4}$, $\overline{IRQ2}$, $\overline{IRQ1}$/Port B4, B2, B1, $\overline{AVEC}$	$\overline{CS3}$–$\overline{CS0}$	Enables peripherals at programmed addresses or provides parallel I/O and automatic vector request during an interrupt acknowledge cycle
Bus Request	$\overline{BR}$	Indicates that an external device requires bus mastership
Bus Grant	$\overline{BG}$	Indicates that the current bus cycle is complete and the MC68340 has relinquished the bus
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an external device has assumed bus mastership
Data and Size Acknowledge	$\overline{DSACK1}$, $\overline{DSACK0}$	Provides asynchronous data transfers and dynamic bus sizing
Read-Modify-Write Cycle	$\overline{RMC}$	Identifies the bus cycle as part of an indivisible read-modify-write operation
Address Strobe	$\overline{AS}$	Indicates that a valid address is on the address bus
Data Strobe	$\overline{DS}$	During a read cycle, DS indicates that an external device should place valid data on the data bus. During a write cycle, DS indicates that valid data is on the data bus.
Size	SIZ1, SIZ0	Indicates the number of bytes remaining to be transferred for this cycle
Read/Write	R/$\overline{W}$	Indicates the direction of data transfer on the bus
Interrupt Request Level/Port B7, B6, B5, B3	$\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ5}$, $\overline{IRQ3}$	Provides an interrupt priority level to the CPU32 or provides parallel I/O
Reset	$\overline{RESET}$	System reset
Halt	$\overline{HALT}$	Suspends external bus activity
Bus Error	$\overline{BERR}$	Indicates an erroneous bus operation is being attempted
System Clock Out	CLKOUT	Internal system clock
Crystal Oscillator	EXTAL, XTAL	Connections for an external crystal to the internal oscillator circuit

Table 4. Signal Index (Continued)

Signal Name	Mnemonic	Function
External Filter Capacitor	XFC	Connection pin for an external capacitor to filter the circuit of the phase-locked loop
Clock Mode Select/Port B0	MODCK	Selects the source of the internal system clock or furnishes a parallel I/O bit
Instruction Fetch	$\overline{\text{IFETCH}}$	Indicates when the CPU32 is performing an instruction word prefetch and when the instruction pipeline has been flushed
Instruction Pipe	$\overline{\text{IPIPE}}$	Used to track movement of words through the instruction pipeline
Breakpoint	$\overline{\text{BKPT}}$	Signals a hardware breakpoint to the CPU32
Freeze	FREEZE	Indicates that the CPU32 has acknowledged a breakpoint
Receive Data	RxDA, RxDB	Serial input to the serial module
Transmit Data	TxDA, TxDB	Serial output from the serial module
Clear to Send	$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$	Serial module clear to send inputs
Request to Send/OP1, OP0	$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	Serial module request to send outputs or can be parallel outputs
Serial Crystal Oscillator	X1, X2	Connections for an external crystal to the serial module internal oscillator circuit
Serial Clock	SCLK	External serial module clock input
Transmitter Ready/OP6	$\overline{\text{TxRDYA}}$	Indicates transmit buffer has a character or can be a parallel output
Receiver Ready/FIFO Full/OP4	$\overline{\text{RxRDYA}}$	Indicates receive buffer has a character, the receiver FIFO buffer is full, or can be a parallel output
DMA Request	$\overline{\text{DREQ2}}$, $\overline{\text{DREQ1}}$	Input that starts DMA process
DMA Acknowledge	$\overline{\text{DACK2}}$, $\overline{\text{DACK1}}$	Output that signals an access during DMA
DMA Done	$\overline{\text{DONE2}}$, $\overline{\text{DONE1}}$	Bidirectional signal that indicates last transfer
Timer Gate	$\overline{\text{TGATE2}}$, $\overline{\text{TGATE1}}$	Counter enable input to timer
Timer Input	TIN2, TIN1	Time reference input to timer
Timer Output	TOUT2, TOUT1	Output waveform from timer
Test Clock	TCK	Provides a clock for IEEE 1149.1 test logic
Test Mode Select	TMS	Controls test mode operations
Test Data In	TDI	Serial test instructions and test data signal
Test Data Out	TDO	Serial test instructions and test data signal
Synchronizer Power	V_{CCSYN}	Power supply to VCO
System Power Supply and Return	V_{CC}, GND	Power supply and return to the MC68340

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C

The following ratings define a range of conditions in which the device will operate without being damaged. However, sections of the device may not operate normally while being exposed to the electrical extremes. This device contains circuitry to protect against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or VCC).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case	θ_{JA}		°C/W
Ceramic 144-Pin QFP		15*	
Plastic 145-Pin PGA		TBD	

*Estimated

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$ — Watts Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

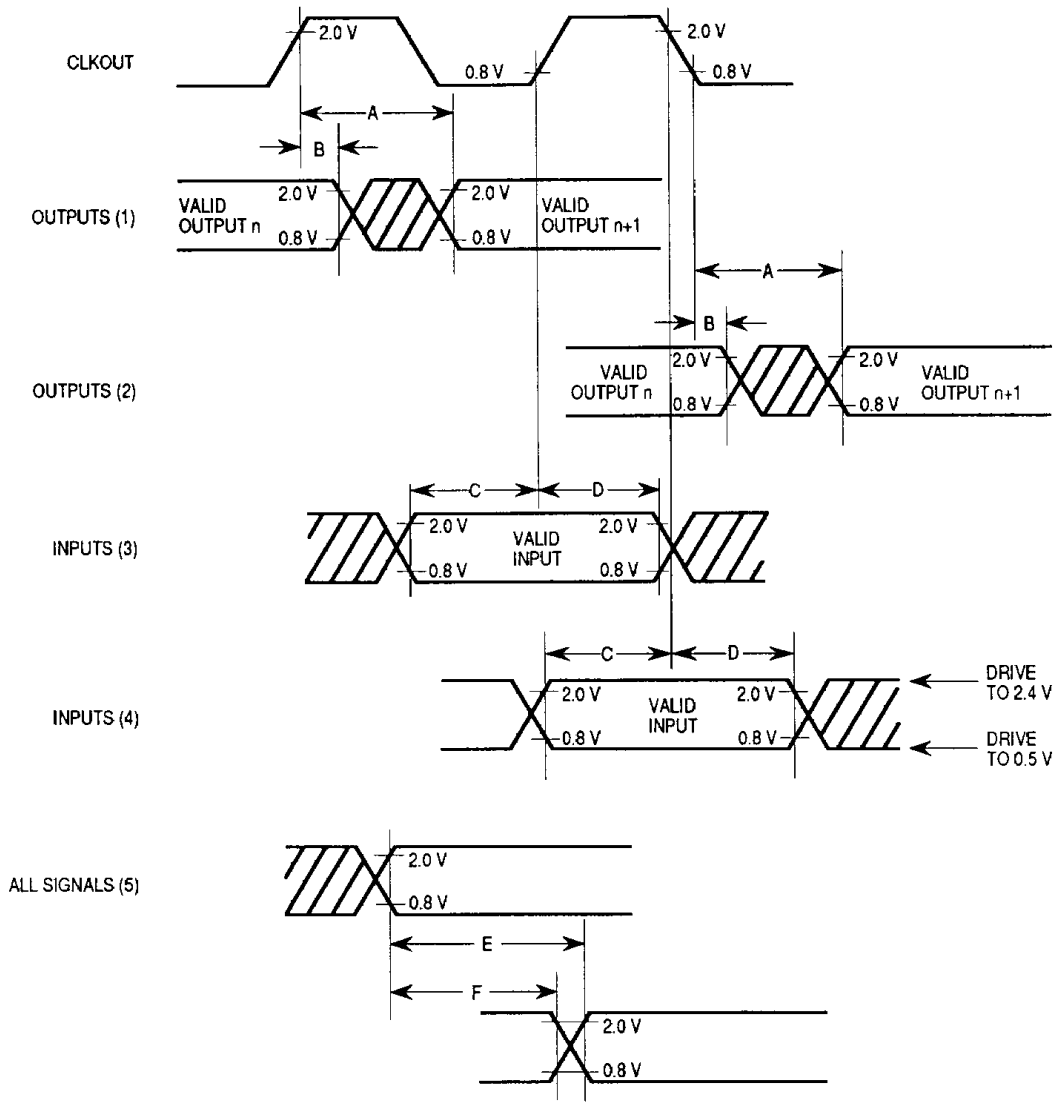
where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 13. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

Note that the testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:

A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 13. Drive Levels and Test Points for AC Specifications