MOTOROLA

MC68606
Technical Summary

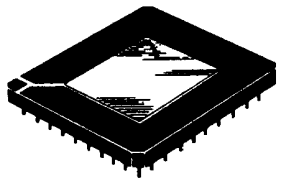
Multi-Link LAPD (MLAPD) Protocol Controller

The Motorola MC68606 Multi-Link LAPD (MLAPD) protocol controller is an integrated circuit implementing the link access procedure (LAPD) protocol. LAPD is the proposed protocol for use at the link layer (ISO-Layer 2) for both signalling and data transfer applications in Integrated Services Digital Network (ISDN) configurations. The LAPD protocol is specified in CCITT Recommendation Q.920/Q.921.

Current product implementations of this link level protocol are accomplished with firmware. This significantly loads the local processor, and presents limitations to both the maximum potential throughput of data and to the number of logical links which may be supported by such packet data interfaces. A generic view of where the MLAPD device can be used to interconnect a diversity of data endpoints in a high speed packet switch network is shown in Figure 1. The data links illustrated could differ functionally and provide data rates in the range of 64 kbps to 2.048 Mbps.

The MLAPD functions as an intelligent peripheral device to a central processing unit (CPU) in a microcomputer system. An on-chip DMA controller transfers data packets to and from a buffer memory. A microcoded buffer management scheme queues packets during transmission and reception. All link management duties are handled by the MLAPD device to maximize the bandwidth available for CPU operation and to increase the throughput for packet data transfer. This VLSI implementation provides a cost effective solution, while encouraging a universal implementation of the LAPD protocol. Key features of the MLAPD device include:

- Full Implementation of CCITT Recommendation Q.920/Q.921 Link Access Procedure (LAPD) with Independent Generation of Commands and Responses for Each Logical Link
- Control of up to 8192 Logical Links Using a Memory-Based Architecture, Wherein the Protocol Controller and the Supervising Microprocessor Communicate Through Shared Memory
- Reliable, Interleaved Data Transfers for Multiple Logical Links with the Following Protocol Actions:
  - HDLC framing with zero-bit insertion/deletion for a serial bit stream; or optional parallel assist mode where zero insertion/deletion is disabled and frame delineation is provided by external pins for supporting a parallel interface to the physical level.
  - Error control using a 16-bit CRC.
  - Flow control to prevent data from accumulating at the receiving end faster than the data can be processed.
- Termination of a Non-Channelized Serial Bit Stream with an Aggregate Rate in Excess of 2.048 Mbps or Optional Memory-to-Memory Operation Allowing the MLAPD to Act as a LAPD Controller Independent of the System's Physical Level Characteristics



RC SUFFIX
PIN GRID ARRAY
(84 PIN)
CASE 793

PIN GRID ARRAY

	1	2	3	4	5	6	7	8	9	10
K	CLK	GND	RxD	V_{DD}	RCLK	V_{DD}	A23	A21	GND	A18
J	V_{DD}	GND	MOTO/$\overline{INT}$	$\overline{RTS}$/$\overline{TSTART}$	TxD	V_{DD}	A20	A19	A17	A15
H	$\overline{RESET}$	$\overline{RETRY}$	GND	$\overline{CTS}$/$\overline{RSTART}$	GND	TCLK	A22	A16	V_{DD}	A14
G	$\overline{IACK}$ ($\overline{INTA}$)	$\overline{BERR}$	$\overline{HALT}$					A13	A12	GND
F	$\overline{BG}$ (HOLDA)	$\overline{BR}$ (HRQ)	$\overline{IRQ}$ (INTR)		BOTTOM VIEW			A9	A11	A10
E	R/$\overline{W}$ ($\overline{WR}$)	GND	$\overline{DTACK}$ (READY)					A8	V_{DD}	GND
D	$\overline{BGACK}$ ($\overline{RD}$)	V_{DD}	$\overline{UDS}$/A0 (A0)					V_{DD}	A5	A7
C	$\overline{LDS}$ ($\overline{BHE}$)	$\overline{CS}$	$\overline{AS}$	GND	V_{DD}	D10	D12	A1	GND	A6
B	GND	D0	D2	D5	GND	D9	GND	D15	A2	A4
A	D1	D3	D4	D6	D7	D8	D11	D13	D14	A3

- Supports User Prioritization of I Frame and XID/UI Frame Transmission
- Supports Optional Receive and Transmit of a User-Defined, Non-Standard LAPD Unnumbered (U) Frame
- On-Chip, Content-Addressable Memory (CAM) Provides Address Translation for Up to 16 Logical Links. When Supporting More Than 16 Logical Links, Translation is Provided Via a Translation Table in Shared Memory
- Provides Error/Statistical Counters and Maskable Interrupts to the Level 3 Process
- Supports Optional Non-Protocol Mode on a Per-Logical Link Basis, Which Allows the Host to Receive and Transmit Frames Without Application of the LAPD Procedures by the MLAPD
- Supports Promiscuous Receive Mode in Which the MLAPD Receives All Frames From the Line and Transfers the Entire Frame to Memory
- System Interface Tailored for Different Microprocessor System Implementations:
  - Motorola M68000 and Intel iAPX86 Family Bus Interface Options
  - 8- and 16-Bit Data Bus Support
  - Direct Addressing of 16 Mbytes of System Memory
- Available in 12.5 MHz and 16.67 MHz System Clock Versions
- 84 Lead PGA and PLCC J-Lead Surface Mount Packages
- 1.5 Micron HCMOS Technology

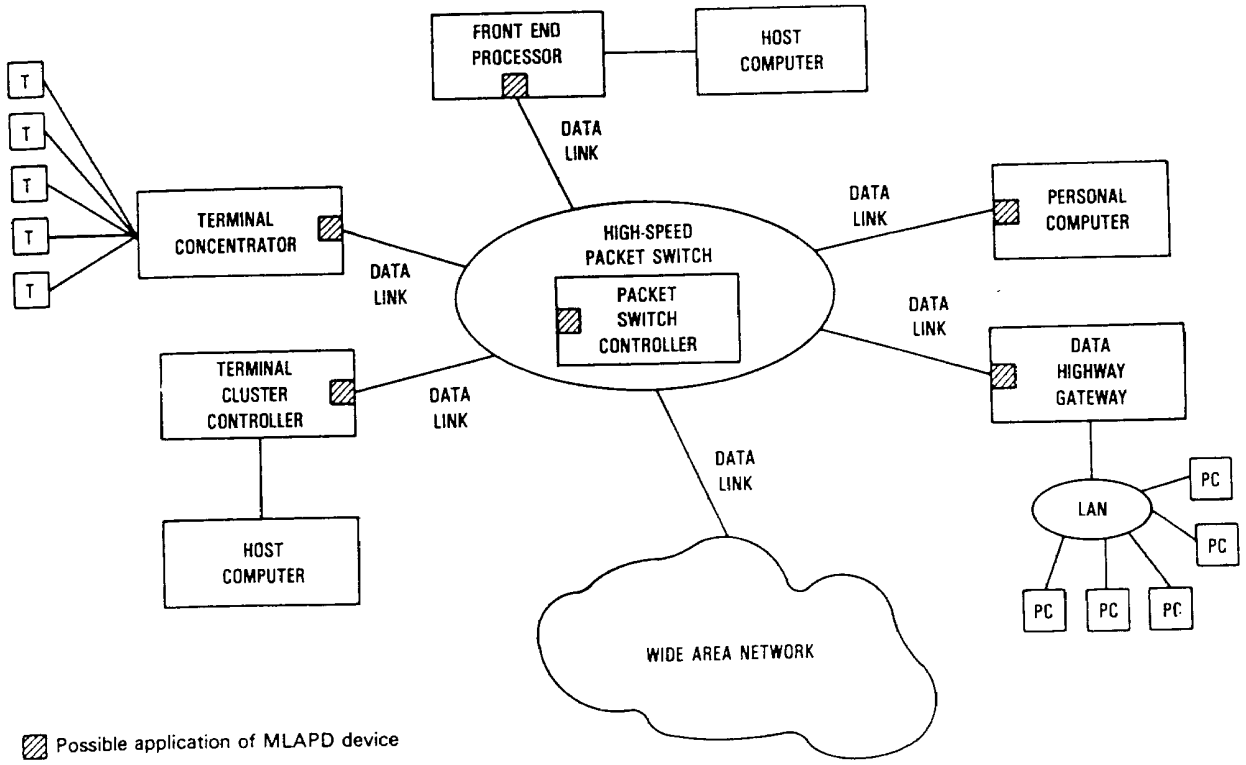


Figure 1. High Speed Data Switching