

MC74VHCT14A

Hex Schmitt Inverter

The MC74VHCT14A is an advanced high speed CMOS Schmitt inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHCT04A, but the inputs have hysteresis and, with its Schmitt trigger function, the VHCT14A can be used as a line receiver which will receive slow input signals.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT14A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0V$. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 5.5ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 2\mu A$ (Max) at $T_A = 25^\circ C$
- TTL-Compatible Inputs: $V_{IL} = 0.8V$; $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: 60 FETs or 15 Equivalent Gates

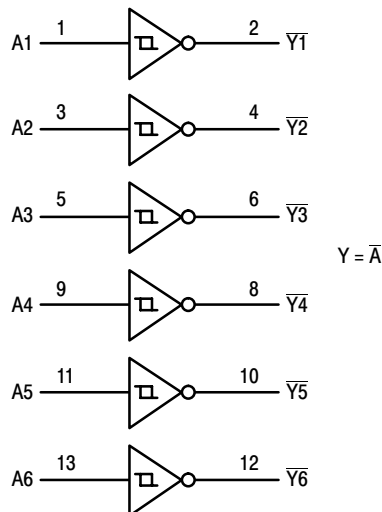
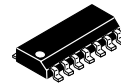


Figure 1. Logic Diagram

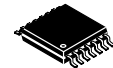


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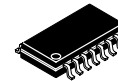
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14-LEAD SOIC
D SUFFIX
CASE 751A

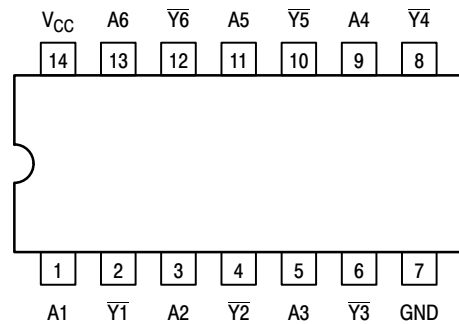


14-LEAD TSSOP
DT SUFFIX
CASE 948G



14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTIONS



Pinout: 14-Lead Packages (Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT14AD	SOIC	55 Units/Rail
MC74VHCT14ADT	TSSOP	96 Units/Rail
MC74VHCT14AM	SOIC EIAJ	50 Units/Rail

FUNCTION TABLE

Inputs	Outputs
A	\bar{Y}
L	H
H	L

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	Output in HIGH or LOW State (Note 1)	-0.5 to V _{CC} +0.5 V
V _{OUT}	V _{CC} = 0 V	-0.5 to 7.0	V
I _{IK}	DC Input Diode Current	-20	mA
I _{OK}	DC Output Diode Current	±20	mA
I _O	DC Output Source/Sink Current	±25	mA
I _{CC}	DC Supply Current per Supply Pin	±50	mA
I _{GND}	DC Ground Current per Ground Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance	SOIC TSSOP	125 170
P _D	Power Dissipation in Still Air	SOIC TSSOP	500 450
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 2000
I _{Latch-Up}	Latch-Up Performance	Above V _{CC} and Below GND at 85°C (Note 5)	±300

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.5	5.5	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage (Note 1)	0	V _{CC}	V
V _O	V _{CC} = 0 V	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	Positive Threshold Voltage		4.5 5.5			1.9 2.1		1.9 2.1		1.9 2.1	V
V _{T-}	Negative Threshold Voltage		4.5 5.5	0.5 0.6			0.5 0.6		0.5 0.6		V
V _H	Hysteresis Voltage		4.5 5.5	0.40 0.40		1.40 1.50	0.40 0.40	1.40 1.50	0.40 0.40	1.40 1.50	V
V _{OH}	Minimum High-Level Output Voltage I _{OH} = -50μA	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50μA	4.5	4.4	4.5		4.4		4.4		V
		I _{OH} = -8mA	5.5	3.94			3.80		3.66		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA	4.5		0.0	0.1		0.1		0.1	V
		I _{OL} = 8mA	5.5			0.36		0.44		0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μA
I _{CC(T)}	Quiescent Supply Current	Input: V _{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I _{OFF}	Output Leakage Current	V _{OUT} = 5.5V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to \bar{Y}	V _{CC} = 5.0 ± 0.5 V C _L = 15pF C _L = 50pF		5.5 7.0	7.6 9.6	1.0 1.0	9.0 11.0	1.0 1.0	11.5 13.5	ns
C _{IN}	Maximum Input Capacitance			2	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 6)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		11		

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/6 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.8	1.0	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.8	-1.0	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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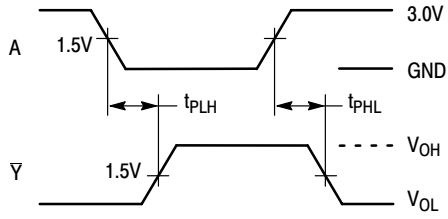
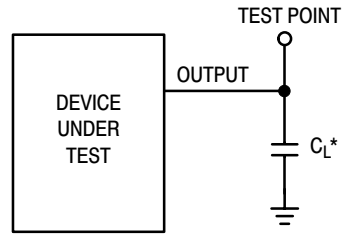


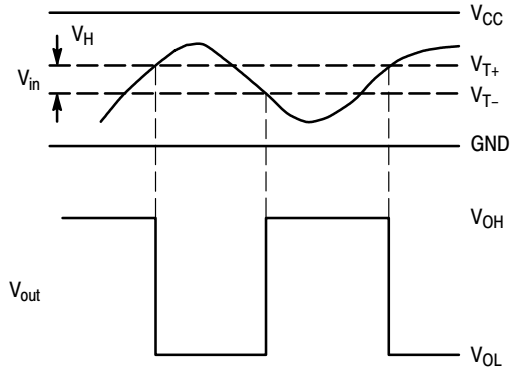
Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

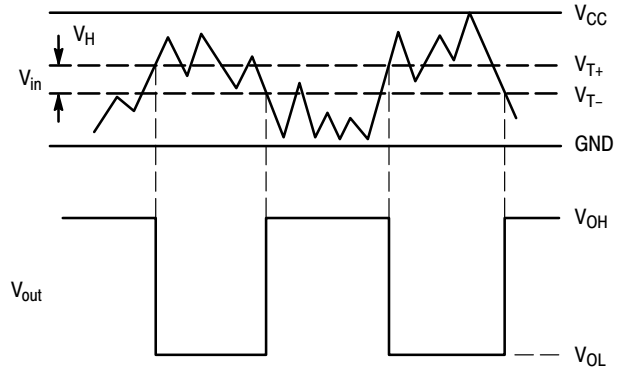
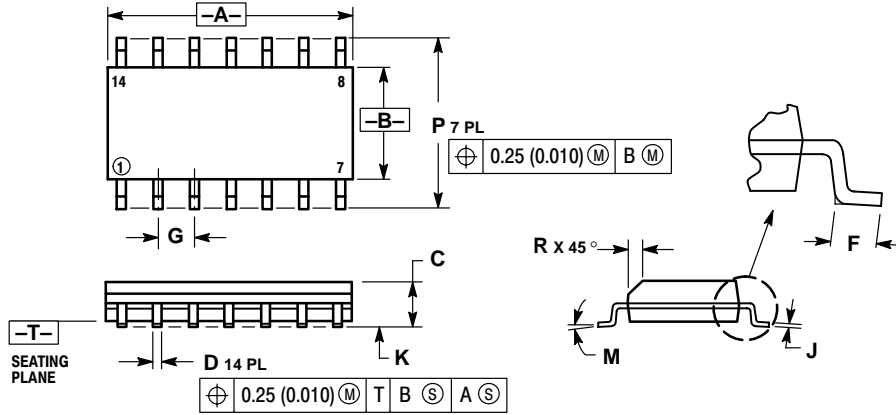


Figure 4. Typical Schmitt-Trigger Applications

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OUTLINE DIMENSIONS

D SUFFIX
SOIC-14
CASE 751A-03
ISSUE F



NOTES:

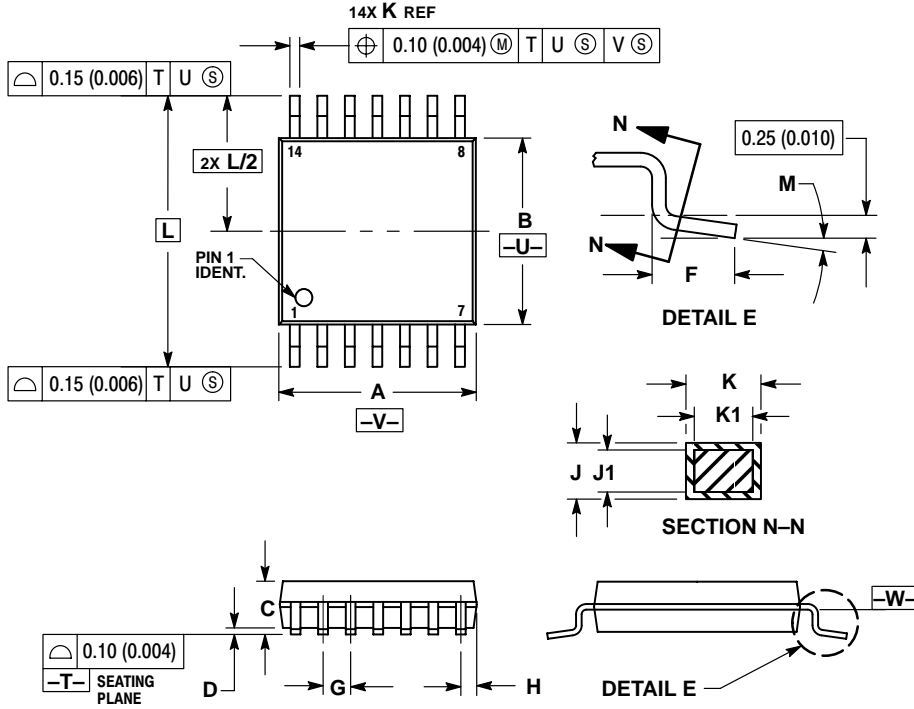
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC74VHCT14A

OUTLINE DIMENSIONS

DT SUFFIX
TSSOP
CASE 948G-01
ISSUE O



NOTES:

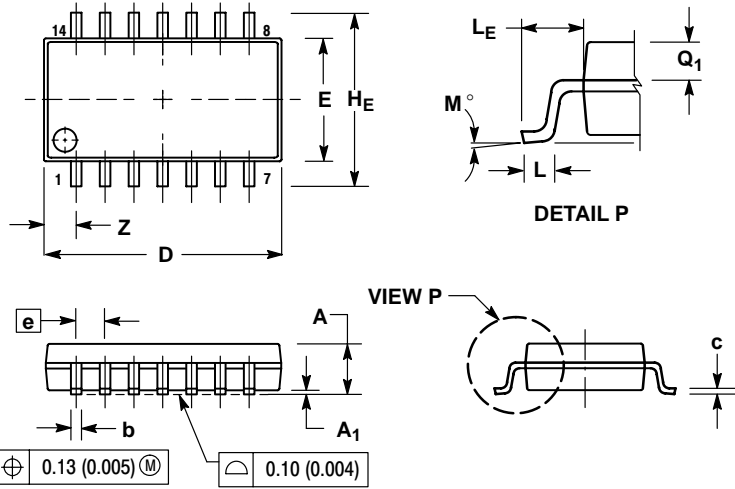
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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OUTLINE DIMENSIONS

M SUFFIX
SO-14
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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