

MC92308

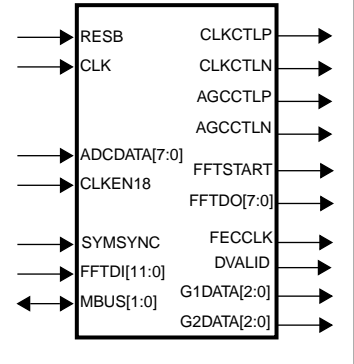
Product Preview

OFDM Demodulator

The MC92308 is a Orthogonal Frequency Division Multiplex Demodulator for 2K transmission mode according to the ETSI specification for digital terrestrial broadcasting (PR ETS 300744). The MC92308 contains all the functionality required to demodulate the information transmitted in one UHF channel.

Feature Summary

- Usable for 8MHz/7MHz/6MHz channels by adjusting the clock rate
- Digital I/Q separation on-chip
- Supports QPSK, 16-QAM and 64-QAM
- Supports all guard interval lengths (1/32, 1/16, 1/8, 1/4)
- Accepts 8-bit TTL-compatible twos-complement data input
- Provides the required control signals for Automatic Gain Control and ADC clock frequency control
- Performs channel estimation and correction by using the embedded pilot carriers
- I²C serial bus compatible interface (M-Bus) and parallel interface for external programming and control of the device
- Transmission Parameter Signalling is decoded and made available to the system controller via M-Bus or parallel microprocessor interface
- Companion to DVB compliant 2K-FFT Processor (MC92307)
- Output interface for DBV compliant FEC
- Fast synchronization at power-on and after channel switch
- Low implementation margin
- 0.5µ CMOS Process at 3.3V



Ordering Information

| Device | Package |
|-----------|----------|
| MC92308CI | 160MQUAD |

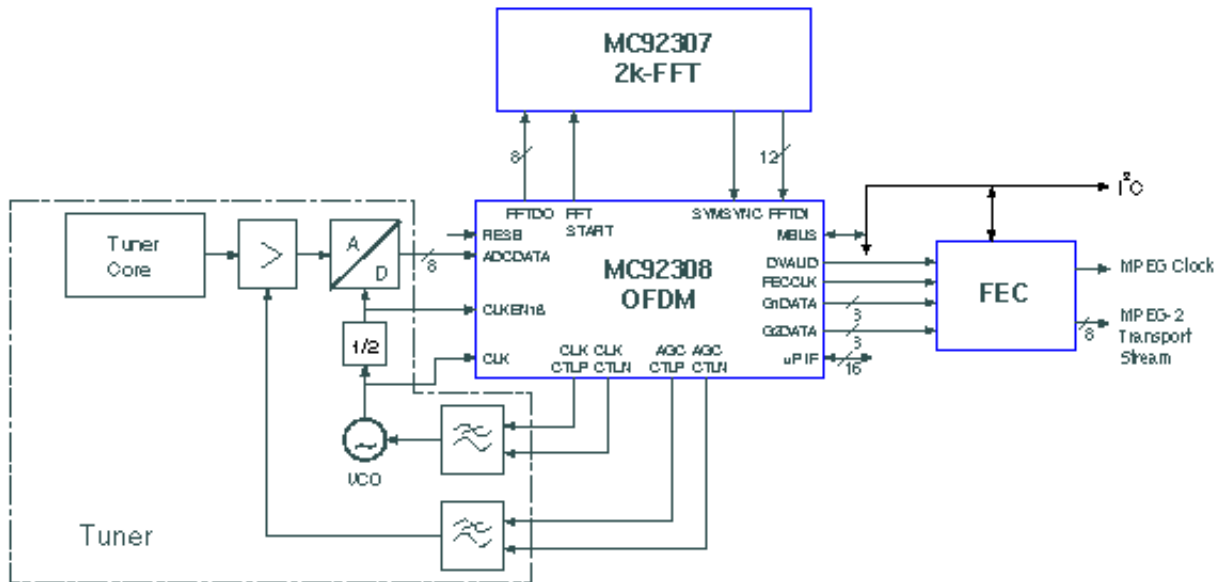
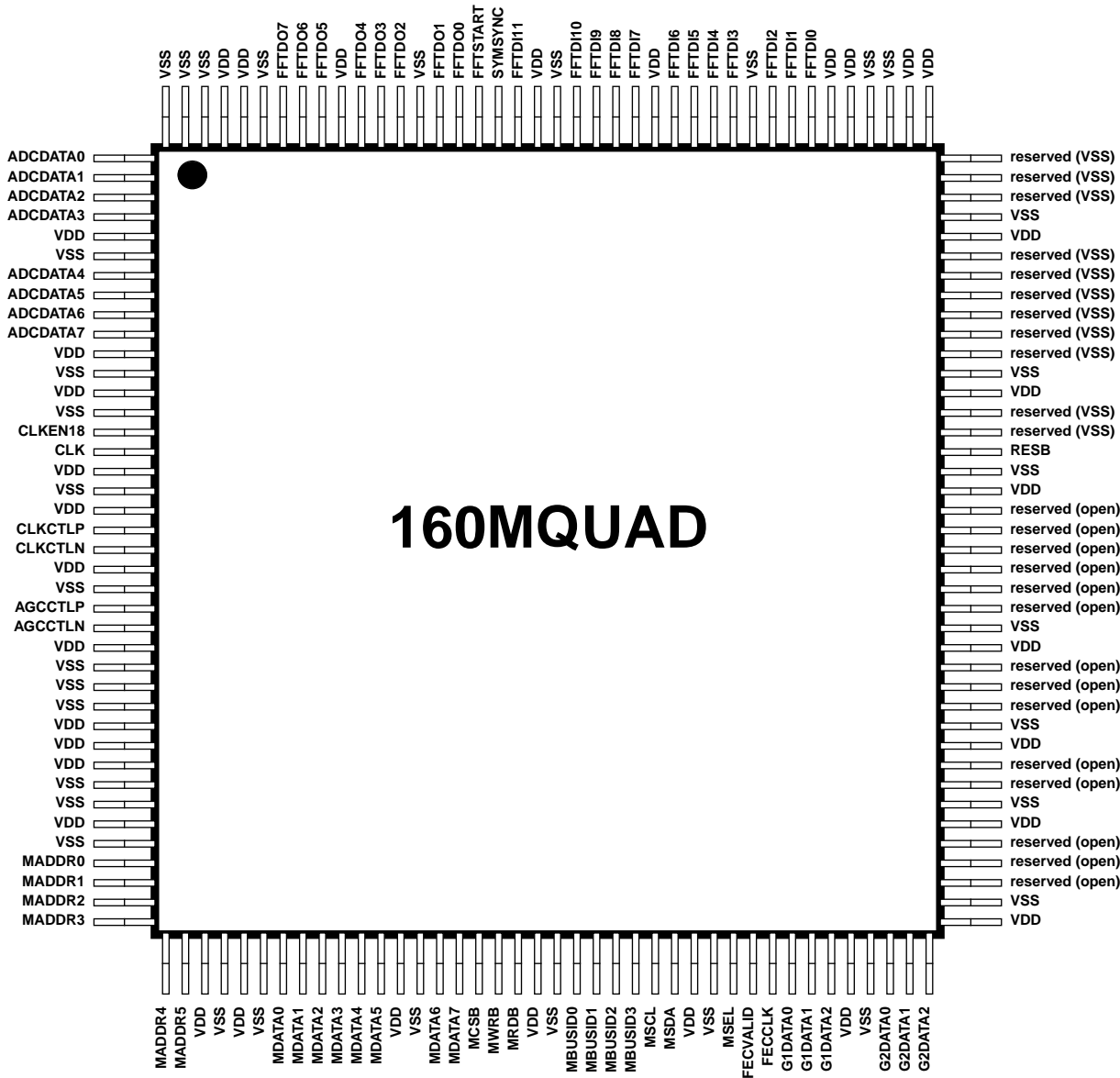


Figure 1. OFDM Frontend Processing

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.





160MQUAD

Table 1. MC92308 Pin Description

| SIGNAL | FUNCTIONALITY | TYPE | POLTY |
|--------------|------------------------------------|-----------|-------|
| CLK | Common clock input (36.57 MHz) | TTL - IN | high |
| RESB | Reset (synchronous) | TTL - IN | low |
| CLKEN18 | ADC data strobe | TTL - IN | high |
| ADCDATA[7:0] | Input for samples from ADC | TTL - IN | high |
| CLKCTLP | ADC clock synchronization loop (+) | TTL - OUT | high |
| CLKCTLN | ADC clock synchronization loop (-) | TTL - OUT | low |
| AGCCTLP | Analog AGC loop (+) | TTL - OUT | high |
| AGCCTLN | Analog AGC loop (-) | TTL - OUT | low |
| FFTSTART | FFT start signal | TTL - OUT | high |
| FFTDO[7:0] | Complex data output to FFT (muxed) | TTL - OUT | high |

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