MC141537

LCD Segment / Common Driver with Controller

CMOS

MC141537 is a CMOS LCD Driver which consists of 3 annunciator outputs and 136 high voltage LCD driving signals (16 common and 120 segment). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit such that limited external component is required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30˚C to 85˚C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 bit Parallel Interface
- Graphic Mode Operation
- On Chip 240 byte Graphic Display Data RAM
- Master clear RAM
- 120 Segment Drivers, 16 Common Drivers
- 1/16 multiplex ratio
- 1:5 bias ratio
- Re-mapping of Row and Column Drivers
- Three stand alone Annunciator driver circuits
- Selectable LCD Drive Voltage Temperature Coefficients
- 16 level Internal Contrast Control
- External Contrast Control
- Available in Bare Die Form

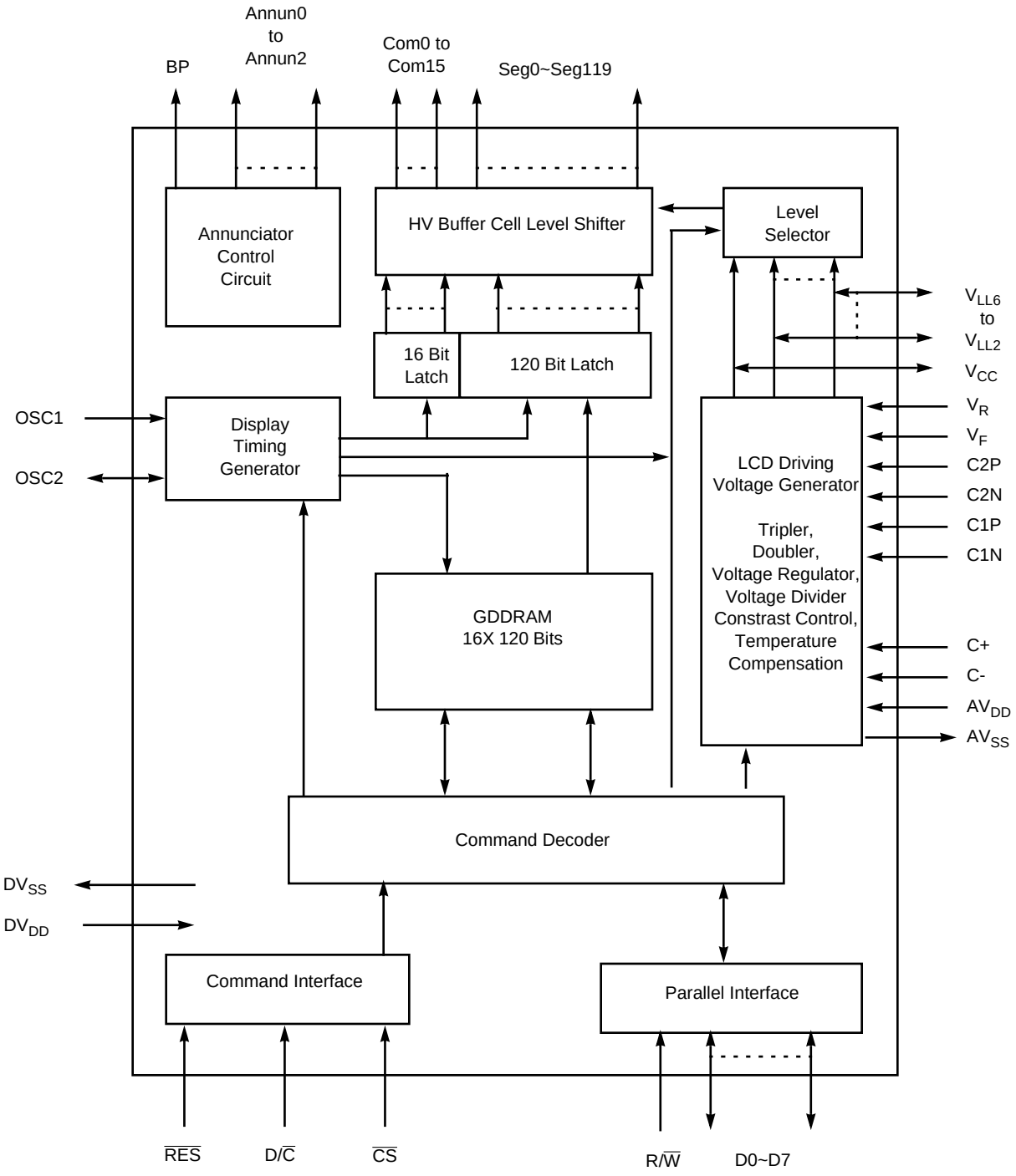
MC141537
Bare Die

ORDERING INFORMATION

MCC141537	Bare Die

REV 7
2/98

BLOCK DIAGRAM



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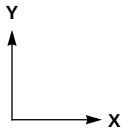


MCC141537 DIE PIN ASSIGNMENT

Refer to the MC141537 Die Pad Coordinate for Pin Name Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
	Operating Temperature		
T_{A1}	For Using Internal Oscillator	-25 to +85	˚C
T_{A2}	For Using External Oscillator	-30 to +85	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

V_{SS} = AV_{SS} = DV_{SS} (DV_{SS} =V_{SS} of Digital circuit, AV_{SS} = V_{SS} of Analogue Circuit)

V_{DD} = AV_{DD} = DV_{DD} (DV_{DD} =$V_{DD}$of Digital circuit, AV_{DD} = V_{DD} of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DV_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.4	3.0	3.5	V
AV_{DD}	Voltage Generator Circuit Supply Voltage Range		2.4	-	3.5	V
I_{AC}	Access Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/Off, R/W accessing, T_{cyc}=1MHz, Osc. Freq.=38.4KHz, Display On.	0	200	300	µA
AI_{DP}	Display Mode Supply Current Drain (AV_{DD} Pin)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/OFF, R/W halt, Osc. Freq.=38.4KHz, Display On.	0	70	150	µA
DI_{DP}	Display Mode Supply Current Drain (DV_{DD} Pin)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/OFF, R/W halt, Osc. Freq.=38.4KHz, Display On.	0	6	15	µA
I_{SB1}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Display off, Oscillator Disabled, R/W halt.	0	300	500	nA
I_{SB2}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, External Oscillator, Oscillator Enabled, Display Off, R/W halt, Ext Osc. Freq.=38.4KHz.	0	1	2	µA
I_{SB3}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal Oscillator, Oscillator Enabled, Display Off, R/W halt, Int Osc. Freq.=38.4KHz.	0	5	10	µA
V_{CC1}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Tripler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Doubler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage Input (V_{CC} Pin)	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
V_{OH1}	Output High Voltage (D0-D7, Annun0-2, BP, OSC2)	I_{out}=100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D0-D7, Annun0-2, BP, OSC2)	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source (V_R Pin)	Regulator Enabled (V_R voltage depends on TC and Int/Ext Contrast Control)	0	-	V_{CC}	V
V_{R2}	LCD Driving Voltage Source (V_R Pin)	Regulator Disable.	-	Floating	-	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0	-	0.2*V_{DD}	V
V_{LL6}	LCD Display Voltage Output	Voltage Divider Enabled	-	V_R	-	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		-	0.8*V_R	-	V
V_{LL4}			-	0.6*V_R	-	V
V_{LL3}			-	0.4*V_R	-	V
V_{LL2}			-	0.2*V_R	-	V
V_{LL6}	LCD Display Voltage Input	External Voltage Generator, Voltage Divider Disable	0	-	V_{CC}	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		0	-	V_{CC}	V
V_{LL4}			0	-	V_{CC}	V
V_{LL3}			0	-	V_{CC}	V
V_{LL2}			0	-	V_{CC}	V
I_{OH}	Output High Current Source (D0-D7, Annun0-2, BP, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D0-D7, Annun0-2, BP, OSC2)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (D0-D7, OSC2)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		-1	-	1	µA
R_{on}	Channel resistance between LCD driving signal-pins (SEG and COM) and driving voltage input pins (V_{LL2} to V_{LL6})	During Display on, 0.1V apply between two terminals, VCC within operating voltage range	-	-	10	KΩ
V_{SB}	Memory Retention Voltage (DV_{DD})	Standby mode, retain all internal configuration and RAM data	2	-	-	V
C_{IN}	Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
	Temperature Coefficient Compensation*					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%
V_{CN}	Internal Contrast Control (V_R Output Voltage)	Regulator Enabled, Internal Contrast control Enabled. (16 Voltage Levels Controlled by Software. Each level is typically 2.25% of the Regulator Output Voltage.)	-	± 18	-	%

*The formula for the temperature coefficient (TC) is:

$$TC(\%)= \frac{V_R \text{ at } 50^\circ C - V_R \text{ at } 0^\circ C}{50^\circ C - 0^\circ C} \times \frac{1}{V_R \text{ at } 25^\circ C} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (T_A=25˚C, Voltage referenced to V_{SS}, AV_{DD}=DV_{DD}=3V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	60Hz Frame Frequency Either External Clock Input or Internal Oscillator Enabled	-	38.4	-	KHz
F_{ANN}	Backplane Frequency of Annunciator (Annun0-2, BP)	50% duty cycle Annunciator on, Fosc=38.4KHz	-	30	-	Hz
F_{FRM}	Frame Frequency	Graphic Display Mode, Timing generator freq. within specification	-	60	-	Hz
OSC	Internal Oscillation Frequency with different value of feedback resistor	Internal Oscillator Enabled, V_{DD} within operation range	See Figure 1 for the relationship			

Note: $F_{FRM}=F_{OSC}/640$
$F_{ANN}=F_{OSC}/1280$

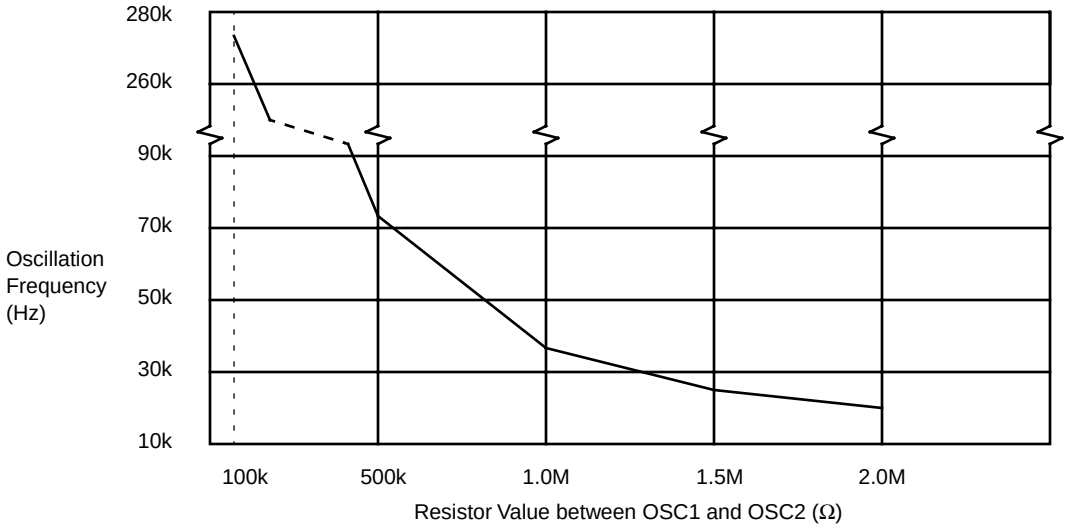


Figure 1. Internal Oscillator Frequency Relationship with External Resistance

TABLE 2. Parallel Timing Characteristics (Write Cycle) (T_A=-30 to 85˚C, DV_{DD}=2.4 to 3.5V, V_{SS}=0)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{DS}	Data Setup Time	350	-	-	ns
t_{DH}	Data Hold Time	30	-	-	ns
t_{AH}	Address Hold Time	30	-	-	ns

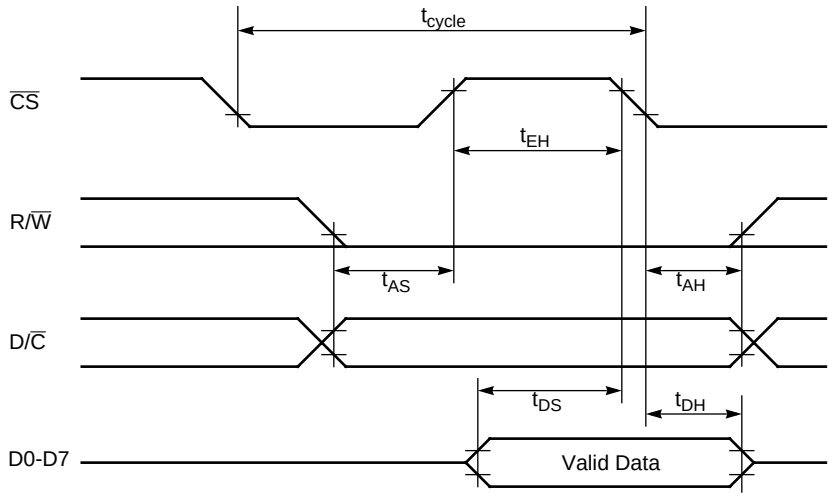


Figure 3a. Parallel Timing Characteristics (Write Cycle)

TABLE 3. Parallel Timing Characteristics (Read Cycle) (T_A=-30 to 85˚C, DV_{DD}=2.4 to 3.5V, V_{SS}=0)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{DS}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	30	-	-	ns
t_{AH}	Address Hold Time	30	-	-	ns

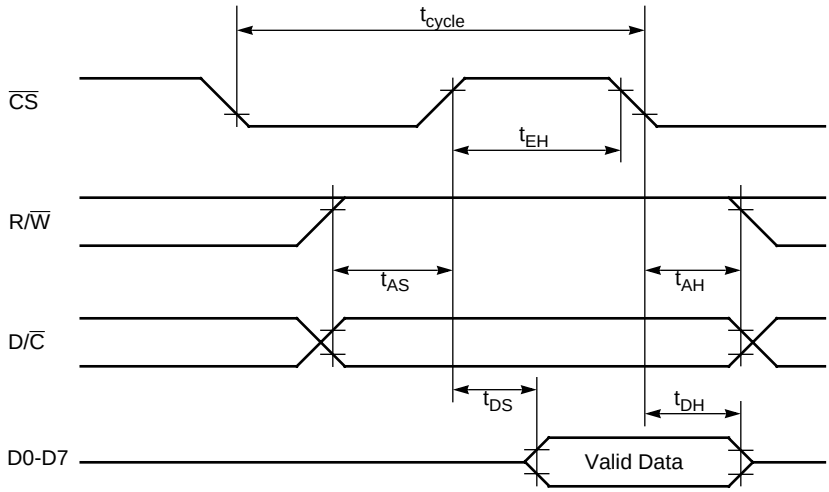


Figure 3b. Parallel Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)

This input pin tell the driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Input Clock)

This pin is normal Low clock input. Input on D0-D7 is latched at the falling edge of CS.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 μs.

D0-D7

This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read/Write)

This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a capacitor to AV_{SS} is required on each pin.

C1N and C1P

If Internal DC/DC Converter is enabled, a capacitor is required to connect these two pins.

C2N and C2P

If Internal DC/DC Converter is enable with Tripler enable, a capacitor is required to connect between these two pins. Otherwise, it should be left open.

C+ and C-

If internal divider circuit is enabled, a capacitor is required to connect between these two pins.

VR and VF

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 μF capacitor placed between VR and AVSS. (Refer to the Application Circuit Section)

COM0-COM15 (Row Drivers)

These pins provide the row driving signal to LCD panel. They output 0V during display off.

SEG0-SEG119 (Column Drivers)

These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)

This pin combines with Annun0-Annun2 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANN} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun2 (Annunciator Frontplanes)

These pins are three independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANN} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

AVDD and AVSS

AVDD is the positive supply to the LCD bias voltage generator. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 μF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the operating mode of the part and the status of the D/$\overline{C}$ line. If D/$\overline{C}$ High, data is written to Graphic Display Data RAM (GDDRAM). D/$\overline{C}$ Low indicates that the data is interpreted as a Command.

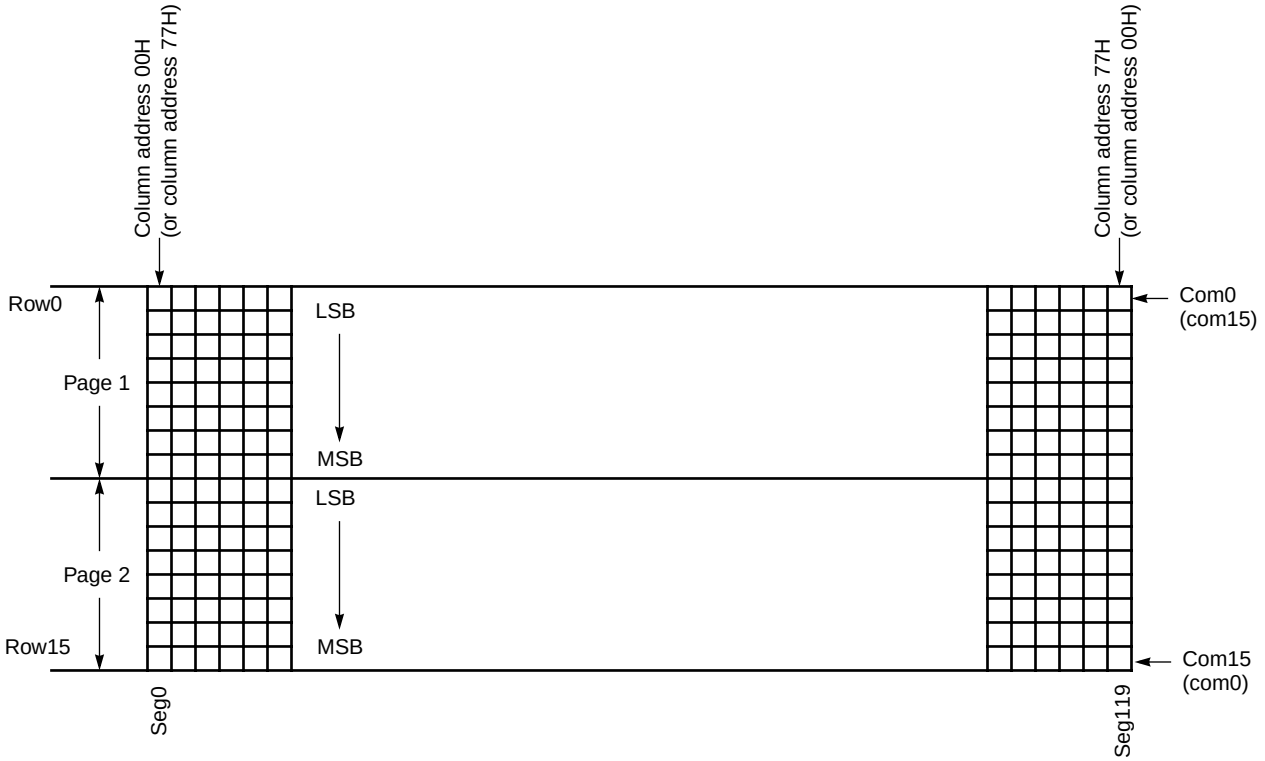
Reset has the same function as Power ON Reset (POR). Once $\overline{RES}$ received the POR pulse, all internal circuitry will reset to its initial status. Refer to Command description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7) plus R/$\overline{W}$ and $\overline{CS}$. The R/$\overline{W}$ line High indicates a read of the Graphic Display Data RAM (GDDRAM). R/$\overline{W}$ line Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ line. The $\overline{CS}$ line serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM that holds the bit pattern to be displayed at graphic display mode. The size of the RAM is determined by number of row times the number of column drivers (120x16 = 1920 bits). Figure 4 is a description of GDDRAM address map. For mechanical feasibility, re-mapping on both Segment and Common outputs are provided.



Note : The configuration in parentheses represent the remapping of Commons and Columns

Figure 4. Graphic Display Data RAM Address MAP

Display Timing Generator

The part is an on chip low power RC oscillator circuitry (figure 5). The oscillator frequency is selected by external resistor in the range of 15 kHz to 50 kHz. The circuitry can be enabled with software control. For external clock application, feed clock into OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 3 Annunciators and BP are generated by this block. The 3 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit. The Oscillator must be enabled before selecting the annunciator on. Annunciator display waveform is shown in Figure 6.

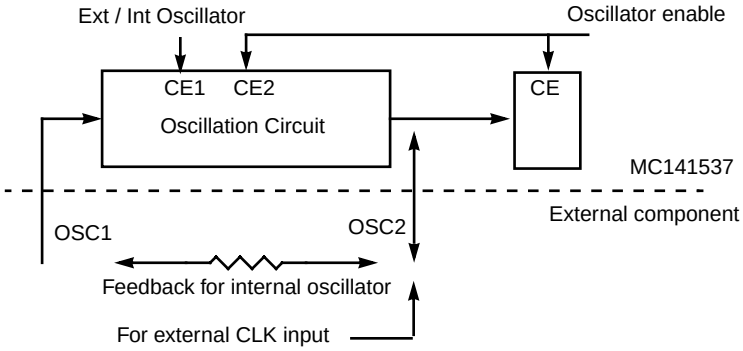


Figure 5. Oscillator Circuitry

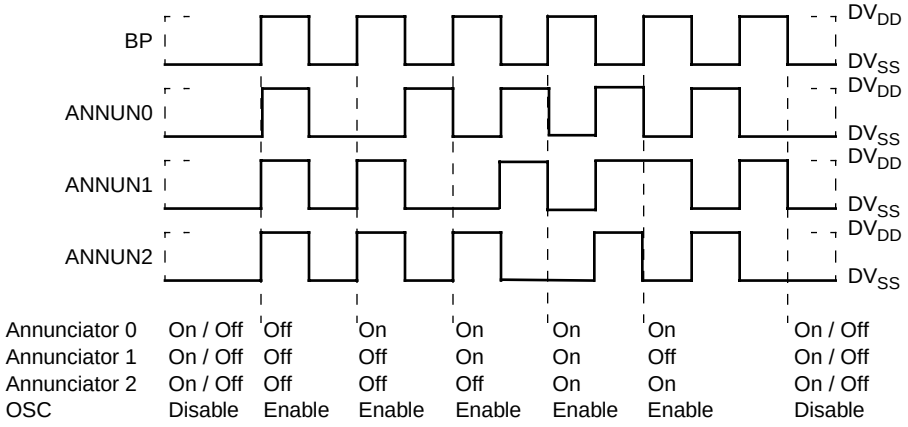


Figure 6. Annunciators and BP display waveform

LCD Drive Voltage Generator

This module generates the LCD voltages needed for display output. This section should take a single supply input and generate necessary bias voltage.

It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Doubler is used for LCD panel which needs lower driving voltage for less power consumption. Tripler is used for LCD panel which needs higher driving voltage.
2. Voltage Regulator
   Feedback gain control for initial LCD display voltage. One can also use it as an external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which consumes very little I_{LCD} current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. This temperature coefficients can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD display voltage.

All blocks can be individually turned off if external voltage generator is provided.

16 Bit Latch / 120 Bit Latch

A 136 bit long register which carries the display signal information. First 16 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the Level Shifter for bumping up to the required level.

Level Selector

Level selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycle. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV buffer cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with a internal FRM clock which comes from the Display Timing Generator. The voltage levels are determined by the level selector which is synchronized with the internal M signal.

LCD Panel Driving Waveform

This is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveform shown in figure 7a, 7b and 7c illustrates the desired multiplex scheme.

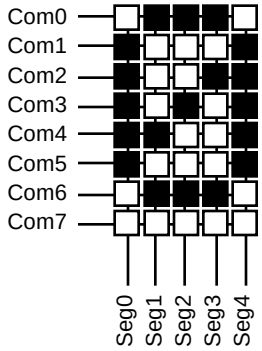


Figure 7a. LCD Display Waveform

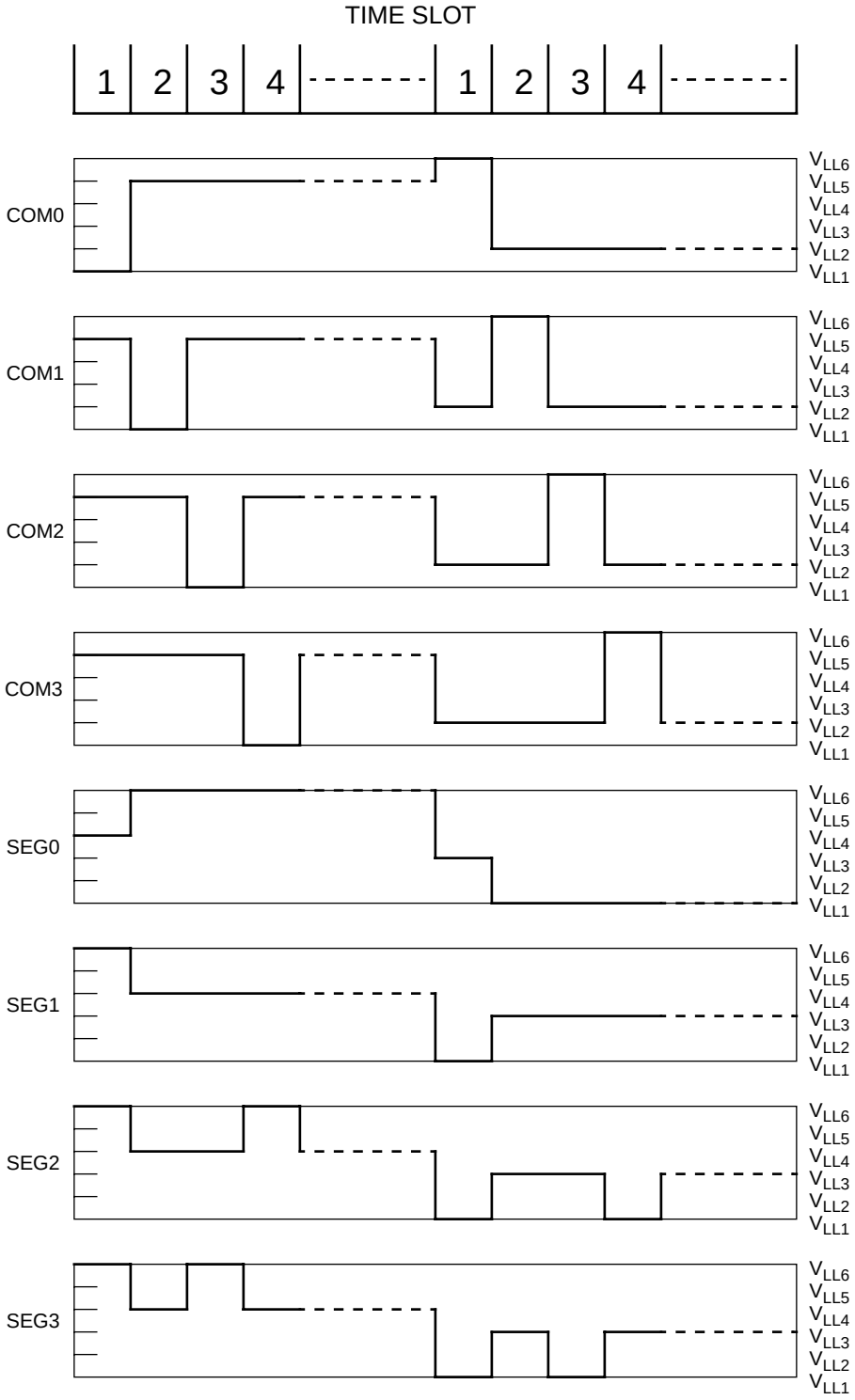


Figure 7b. LCD Driving Signal from MC141537

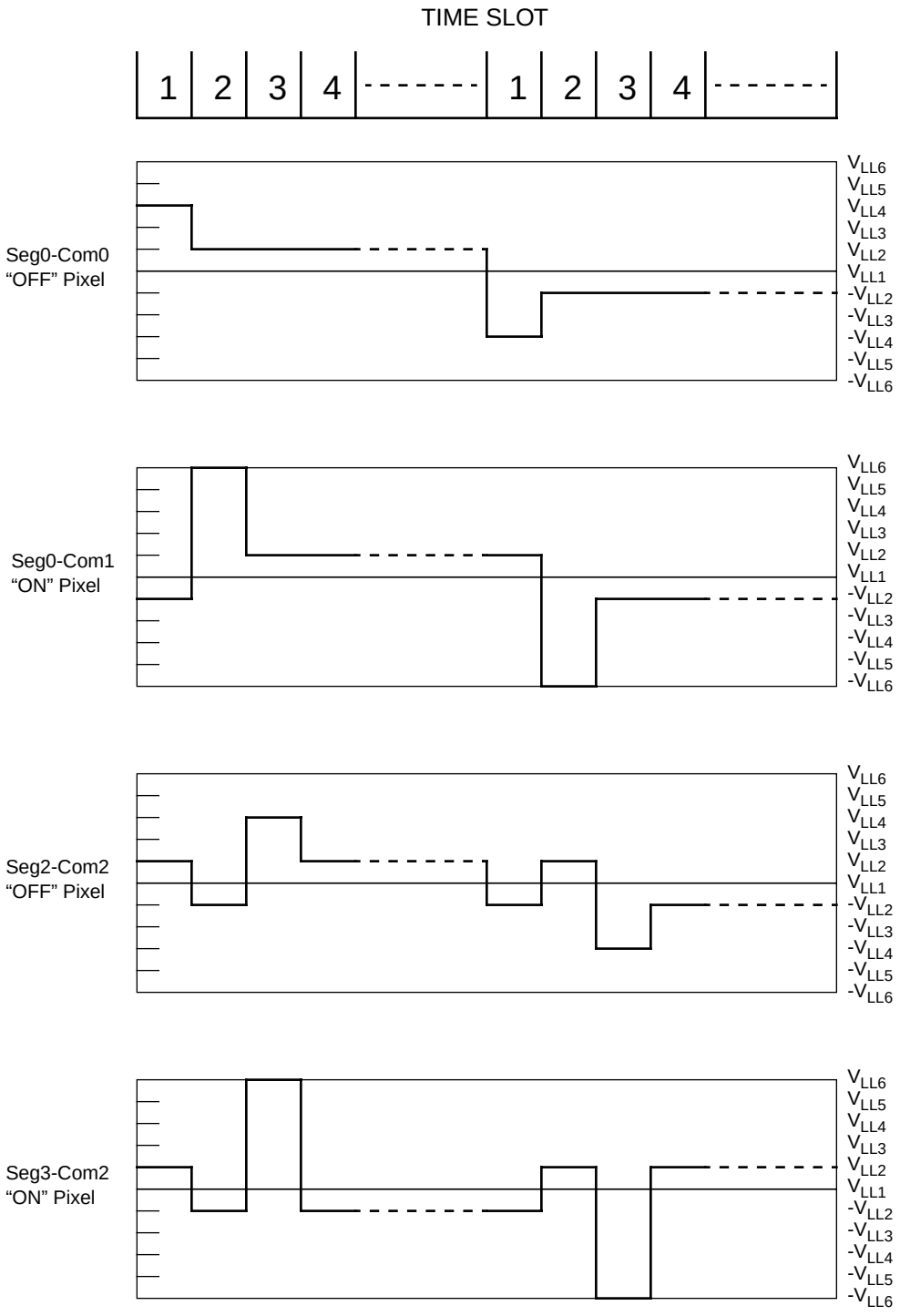


Figure 7c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by mode)

The Display On command controls the selecting of the LCD output voltage and has no effect on the annunciator drivers. The Display On command causes the conversion of data in GDDRAM to the necessary waveforms on the Common and Segment driver outputs. It enables the on-chip bias generator. (Note : "Set Oscillator On" command should be issued before "display on")

The Display Off Command turns the display off and the state of the LCD driver are as follow during display off:
1) The Common and Segment driver outputs are fixed at V_{LL1} (V_{SS}).
2) The bias voltage generator is turned off.
3) The content of all registers and RAM are retained.
4) IC will accept new commands and data.
5) Annunciators is not affected by this command.
6) Oscillator is not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column boundary. The address can be set to location 00H-77H (120 columns). The column address will be increased automatically after a read or write operation. Refer to figure 4, "Address Increment Table" and command "Set GDDRAM Page Address" for further information.

Set GDDRAM Page Address

This command positions the row address pointer to 1 of 2 possible positions in GDDRAM. Refer to figure 4.

Master Clear GDDRAM

This command is a MASTER clear of the GDDRAM. The internal RAM data will be set to Zero after the command is issued. The clear RAM action will be taken if a dummy Write follows the "Clear GDDRAM" command.

Set Vertical Scroll Value

When display is turned on, this command maps the selected GDDRAM row (00H-0FH) to Com0-Com15. With scroll value equal to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 15 are mapped to Com1 through Com15 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 15 will be mapped to Com1 through Com14 respectively and Row 0 will be mapped to Com15.

Save / Restore Column Address

With a bit option = 1, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this instruction restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing idle graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment Drivers for mechanically flexibility. There are 2 selected mappings:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0 - Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119 - Seg0 respectively.

See section "Display Output Description by Example" for related information.

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 15 of GDDRAM to Common 0 - Common 15 respectively;
2. Row 0 - Row 15 of GDDRAM to Common 15 - Common 0 respectively.

See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 3 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on / off Oscillator. For either internal or external oscillator, this command should be executed. This command is not affected by the command " Set Display On/Off" and "Annunciator On/Off". See command "Ext/Int Oscillator" for more information.

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is being selected, feedback resistor between OSC1 and OSC2 is needed. For External oscillation circuit, clock should be input to OSC2. OSC1 should be left open.

Set Internal DC/DC Converter On/Off

This command selects the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external V_{CC} is provided.

Set Voltage Doubler / Tripler

This command selects the Voltage Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

With different bit option values, this command either enables or disables the regulator which consists of internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is enabled, an external power supply should be applied to V_{LL6}- V_{LL2}. If the divider is enabled, the internal circuit will automatically generate the 1:5 bias level driving voltage.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage between the bias voltages. If the bit option = 1, the software selected for delta bias voltage control is enabled. If the bit option = 0, the external contrast control through an external resistor is enabled. Note: The software contrast control and the external feedback contrast controls cannot be both enabled at the same time.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is the lowest.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The constrast level starts from the lowest value after POR.

Set Temperature Coefficient

This instruction selects 4 different LCD drive voltage temperature coefficients allowing for various liquid crystal temperature grades. These temperature coefficients are specified in Electrical Characteristics Tables.

COMMAND TABLE

	Bit Pattern	Command	Comment
1	$0000000X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X0 as address bit. X_0=0: page 1(POR) x_0=1: page 2
30	$0001X_3X_2X_1X_0$	Set Contrast Level	Enable one of the 16 Internal Contrast Value using X3X2X1X0 as data bits. Reset to 0000 during POR.
2	$0010000X_0$	Set Voltage Tripler / Doubler	X_0=0: tripler enabled (POR) X_0=1: doubler enabled
3	$0010001X_0$	Set Colum Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
4	$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 (POR) X_0=1: Row0 to Com15
5	$0010011X_0$	Reserved for Expansion	
6	$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
7	$0010101X_0$	Set Internal DC/DC Converter Enable	X_0=0: disable generator(POR) X_0=1: enable generator
8	$0010110X_0$	Set Internal Regulator On/Off	X_0=0: disable regulator (POR) X_0=1: enable regulator When application uses a supply with built-in temperature compensation, the regulator should be disabled .
9	$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: disable voltage divider (POR) X_0=1: enable voltage divider When an external bias network is used, the voltage divider should be disabled.
10	0011000X0	Set Internal Contrast Control On/Off	X_0=0: disable constrast control (POR) X_0=1: enable constrast control Internal contrast circuits should be disabled if external contrast circuits is used.
11	$0011001X_0$	Reserved for Expansion	
12	$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
13	00110110	Master Clear GDDRAM	Master Clear GDDRAM
14	$0011100X_0$	Reserved for Expansion	
15	$0011101X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode (Note: Be sure to set X0=0 during application)
16	$001111X_1X_0$	Reserved for Expansion	
17	$0100X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_3X_2X_1X_0$ as scroll amount. Scroll value = 0 upon POR
18	$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 0(POR) A_1A_0=01: select annunciator 1 A_1A_0=10: select annunciator 2 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
19	$011010X_1X_0$	Reserved for Expansion	
20	$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%

	Bit Pattern	Command	Comment
21	$0111000X_0$	Increment/Decrement Contrast Level	X_0=0: decrement by one level X_0=1: increment by one level (Note: increment/decrement wraps around; total 16 contrast levels. Start at the lowest level when POR.)
22	$0111001X_0$	Reserved for Expansion	
23	$0111010X_0$	Reserved for Expansion	
24	$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Be sure to set X0=0 during application)
25	$0111100X_0$	Reserved for Expansion	
26	$0111101X_0$	Set External / Internal Oscillator	X_0=0: external oscillator (POR) X_0=1: internal oscillator For internal oscillator circuit enabled, place resistor between OSC1 and OSC2. At external oscillator mode, feed clock to OSC2.
27	$0111110X_0$	Reserved For Expansion	
28	$0111111X_0$	Oscillator Enable	X_0=0: oscillator disable (POR) X_0=1: oscillator enable. This is the master control for oscillator circuitry. Issue command 26 before this command.
29	1X6X5X4X3X2X1X0	Set GDDRAM Column Address	Set GDDRAM Column Address. Use X6X5X4X3X2X1X0 as address bits

DATA READ/WRITE TABLE

	Bit Pattern	Command	Comment
1	$X_7X_6X_5X_4X_3X_2X_1X_0$	Data Read / Data Write D/$\overline{C}$ line high	When R/$\overline{W}$ line low, Data write into GDDRAM. RAM column address pointer will have increment automatically. When R/$\overline{W}$ line high, Data read from GDDRAM. RAM column address pointer will have increment automatically. Address Auto increment will not apply if the last command is Clear RAM. This is a dummy write.

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Parallel Mode Write Command	No	
0	1	Parallel Mode Read Command	No (invalid mode)	1
1	0	Parallel Mode Write Data	Yes	2
1	1	Parallel Mode Read Data	Yes	

Address Increment is done automatically after command being sent or data read write. Only the Column address pointer of GDDRAM is affected.

Remark : 1. Under this condition, the data, not command will be read from RAM.
2. If write data is issued after Command Clear RAM, address inc is not applied.
3. Column Address wraps around.

Commands Required for R/W Actions on RAMs

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address, Set GDDRAM Column Address, Read/Write Data.	$(0000000X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increment GDDRAM Address by one	Dummy Read Data	$(X_7X_6X_5X_4X_3X_2X_1X_0)$
Clear GDDRAM Address.	Master Clear GDDRAM, Dummy Write Data.	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Graphic Mode	Set External / Internal Oscillator, Set Oscillator Enable, Set Display On.	$(0111101X_0)$* (01111111)* (00101001)*
Annunciator Display	Set External / Internal Oscillator, Set Oscillator Enable, Set Annunciator On/Off.	$(0111101X_0)$* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator, Set Display Off, Set Oscillator Enable. Set Annunciator On/Off.	(01111010)* (00101000)* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode 3.	Set Internal Oscillator, Set Display Off, Set Oscillator Enable. Set Annunciator On/Off.	(01111011)* (00101000)* (01111111)* $(01100A_1A_0X_0)$*

1. Other Related Command with Graphic Mode :
   Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

2. Commands Related to Voltage Generator :
   Set Oscillator Enable / Disable, Set External / Internal Oscillator, Set Voltage Doubler / Tripler , Set Temperature Coefficient, Set Internal Regulator On/Off, Set Internal Constrast Control On/Off, Increase / Decrease Contrast Level, Set Contrast Level, Set Internal Voltage Divider On/Off, Set Display On/Off.

* No need if set already.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set External / Internal Oscillator	External	*1
Set Voltage Tripler / Doubler	Tripler	*1
Internal DC/DC Converter Enable	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Set Contrast Level	Contrast Level = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	*1
Set Column Mapping	Seg. 0 = Col. 0	*1
Set Row Mapping	Com. 0 = Row 0	*1
Set Vertical Scroll Value	Scroll Value = 0	*1
Set Oscillator Enable	Disable	
Set Annunciator Control Signals	All Annunciators off	*1
Master Clear RAM	Random	
Dummy Write Data		
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Display Output Description by Example

This an example of output pattern on the LCD panel. Figure 8a, 8b and 8c are data map of GDDRAM and the output pattern on the LCD display with different command enabled. (Scrolling, Column Re-map and Row Re-map)

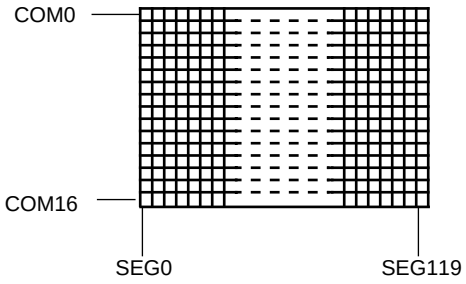
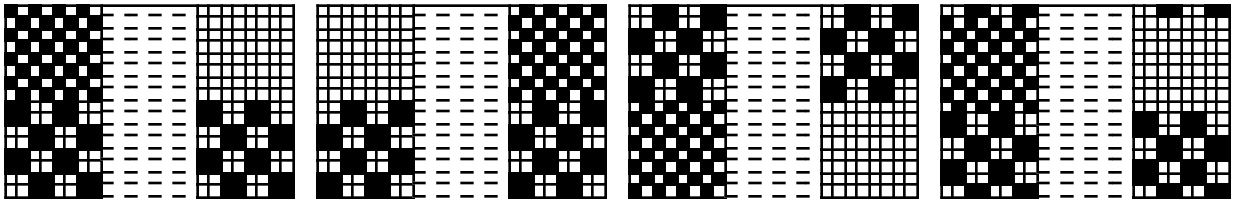


Figure 8a

Content of GDDRAM

PAGE 1	5 A 5 A 5 A - - - 0 0 0 0 0 0 5 A 5 A 5 A - - - 0 0 0 0 0 0
PAGE 2	3 3 C C 3 3 - - - C C 3 3 C C 3 3 C C 3 3 - - - C C 3 3 C C

Figure 8b



Graphic Mode
Column remap disable
Row remap disable

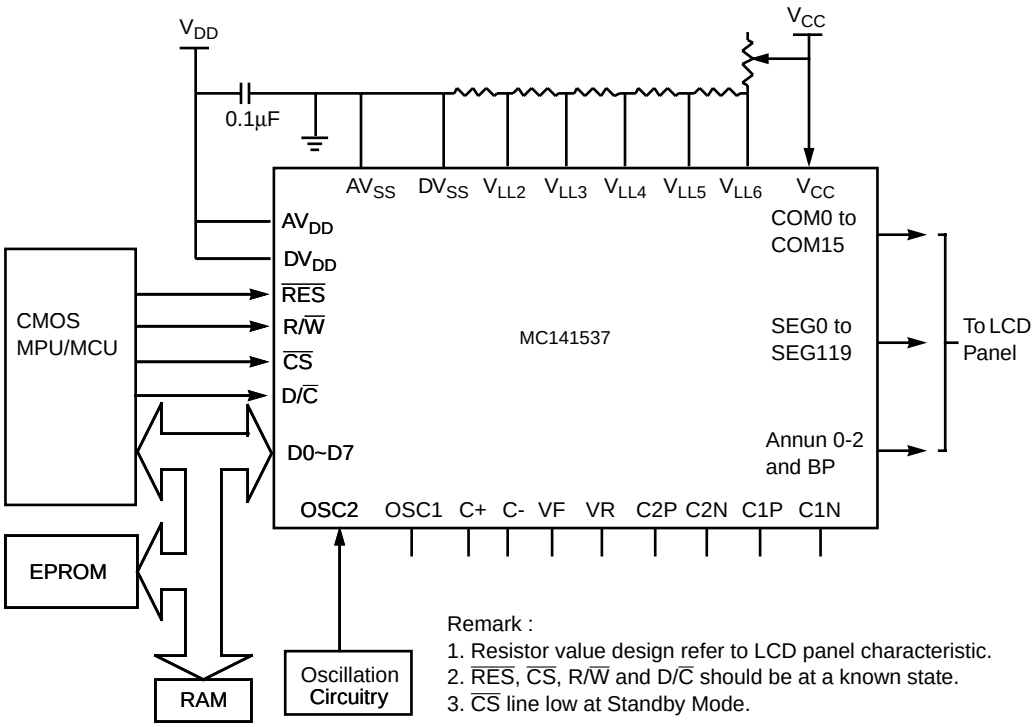
Graphic Mode
Column remap enable
Row remap disable

Graphic Mode
Column remap disable
Row remap enable

Graphic Mode
Column remap disable
Row remap disable
Scroll Value = 0FH

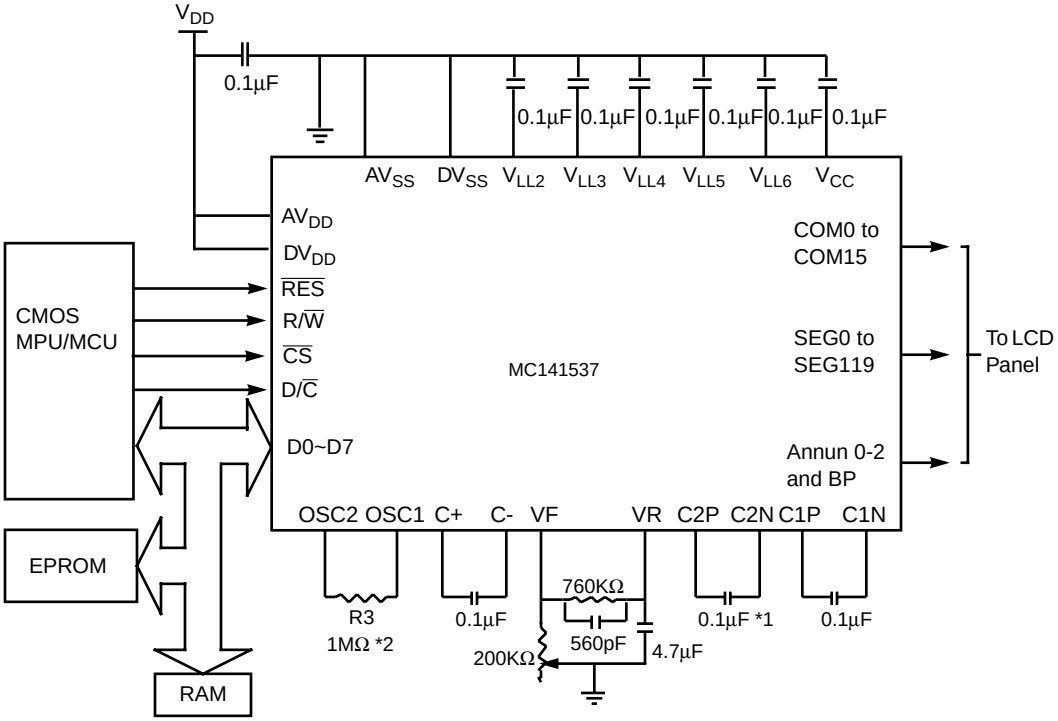
Figure 8c

Application Circuit: (All Internal Analog Block Disabled, External Voltage Generator used)



Remark :
1. Resistor value design refer to LCD panel characteristic.
2. $\overline{RES}$, $\overline{CS}$, R/$\overline{W}$ and D/$\overline{C}$ should be at a known state.
3. $\overline{CS}$ line low at Standby Mode.

Application Circuit: (All Internal Analog Block Enabled)



Remark :
1. Capacitor between C2N and C2P can be omitted only if doubler is enable.
2. R3 can be omitted for external oscillator.
3. VR and VF can be left open for Regulator disable, TC = 0% and Contrast Disable.
4. $\overline{RES}$, $\overline{CS}$, R/$\overline{W}$ and D/$\overline{C}$ should be at a known state.
5. $\overline{CS}$ line low at Standby Mode.

MC141537 Die Pad Coordinate

Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)
1	COM9	-2900.06	-1958.41	59	SEG109	2953.34	-1723.46	94	DUMMY	2705.44	2035.37	148	SEG28	-2953.71	1780.81
2	COM8	-2798.31	-1958.41	60	SEG108	2953.34	-1621.71	95	DUMMY	2603.69	2035.37	149	SEG27	-2953.71	1679.06
3	COM7	-2696.56	-1958.41	61	SEG107	2953.34	-1519.96	96	DUMMY	2501.94	2035.37	150	SEG26	-2953.71	1577.31
4	COM6	-2594.81	-1958.41	62	SEG106	2953.34	-1418.21	97	DUMMY	2400.19	2035.37	151	SEG25	-2953.71	1475.56
5	COM5	-2493.06	-1958.41	63	SEG105	2953.34	-1316.46	98	SEG74	2289.19	1958.41	152	SEG24	-2953.71	1373.81
6	COM4	-2391.31	-1958.41	64	SEG104	2953.34	-1214.71	99	SEG73	2187.44	1958.41	153	SEG23	-2953.71	1272.06
7	COM3	-2289.56	-1958.41	65	SEG103	2953.34	-1068.19	100	SEG72	2085.69	1958.41	154	SEG22	-2953.71	1170.31
8	COM2	-2187.81	-1958.41	66	SEG102	2953.34	-966.44	101	SEG71	1983.94	1958.41	155	SEG21	-2953.71	1068.56
9	COM1	-2086.06	-1958.41	67	SEG101	2953.34	-864.69	102	SEG70	1882.19	1958.41	156	SEG20	-2953.71	966.81
10	COM0	-1984.31	-1958.41	68	SEG100	2953.34	-762.94	103	SEG69	1780.44	1958.41	157	SEG19	-2953.71	865.06
11	DUMMY2	-1882.56	-1958.41	69	SEG99	2953.34	-661.19	104	SEG68	1678.69	1958.41	158	SEG18	-2953.71	763.31
12	OSC2	-1780.81	-1958.41	70	SEG98	2953.34	-559.44	105	SEG67	1576.94	1958.41	159	SEG17	-2953.71	661.56
13	AVSS	-1679.06	-1958.41	71	SEG97	2953.34	-457.69	106	SEG66	1475.19	1958.41	160	SEG16	-2953.71	559.81
14	VR	-1577.31	-1958.41	72	SEG96	2953.34	-355.94	107	SEG65	1373.44	1958.41	161	SEG15	-2953.71	458.06
15	VF	-1475.56	-1958.41	73	SEG95	2953.34	-254.19	108	SEG64	1271.69	1958.41	162	SEG14	-2953.71	356.31
16	VCC	-1373.81	-1958.41	74	SEG94	2953.34	-152.44	109	SEG63	1169.94	1958.41	163	SEG13	-2953.71	254.56
17	C-	-1272.06	-1958.41	75	SEG93	2953.34	-50.69	110	SEG62	1068.19	1958.41	164	SEG12	-2953.71	152.81
18	C+	-1170.31	-1958.41	76	SEG92	2953.34	51.06	111	SEG61	966.44	1958.41	165	SEG11	-2953.71	51.06
19	VLL6	-1068.56	-1958.41	77	SEG91	2953.34	152.81	112	SEG60	864.69	1958.41	166	SEG10	-2953.71	-50.69
20	VLL5	-966.81	-1958.41	78	SEG90	2953.34	254.56	113	SEG59	762.94	1958.41	167	SEG9	-2953.71	-152.44
21	VLL4	-865.06	-1958.41	79	SEG89	2953.34	356.31	114	SEG58	661.19	1958.41	168	SEG8	-2953.71	-254.19
22	OSC1	-763.31	-1958.41	80	SEG88	2953.34	458.06	115	SEG57	559.44	1958.41	169	SEG7	-2953.71	-355.94
23	VLL3	-661.56	-1958.41	81	SEG87	2953.34	559.81	116	SEG56	457.69	1958.41	170	SEG6	-2953.71	-457.69
24	VLL2	-559.81	-1958.41	82	SEG86	2953.34	661.56	117	SEG55	355.94	1958.41	171	SEG5	-2953.71	-559.44
25	C1N	-458.06	-1958.41	83	SEG85	2953.34	763.31	118	SEG54	254.19	1958.41	172	SEG4	-2953.71	-661.19
26	C1P	-356.31	-1958.41	84	SEG84	2953.34	865.06	119	SEG53	152.44	1958.41	173	SEG3	-2953.71	-762.94
27	C2N	-254.56	-1958.41	85	SEG83	2953.34	966.81	120	SEG52	50.69	1958.41	174	SEG2	-2953.71	-864.69
28	C2P	-152.81	-1958.41	86	SEG82	2953.34	1068.56	121	SEG51	-51.06	1958.41	175	SEG1	-2953.71	-966.44
29	AVDD	-51.06	-1958.41	87	SEG81	2953.34	1170.31	122	SEG50	-152.81	1958.41	176	SEG0	-2953.71	-1068.19
30	D7	50.69	-1958.41	88	SEG80	2953.34	1272.06	123	SEG49	-254.56	1958.41	177	COM15	-2953.71	-1214.71
31	D6	152.44	-1958.41	89	SEG79	2953.34	1373.81	124	SEG48	-356.31	1958.41	178	COM14	-2953.71	-1316.46
32	D5	254.19	-1958.41	90	SEG78	2953.34	1475.56	125	SEG47	-458.06	1958.41	179	COM13	-2953.71	-1418.21
33	D4	355.94	-1958.41	91	SEG77	2953.34	1577.31	126	SEG46	-559.81	1958.41	180	COM12	-2953.71	-1519.96
34	D3	457.69	-1958.41	92	SEG76	2953.34	1679.06	127	SEG45	-661.56	1958.41	181	COM11	-2953.71	-1621.71
35	D2	559.44	-1958.41	93	SEG75	2953.34	1780.81	128	SEG44	-763.31	1958.41	182	COM10	-2953.71	-1723.46
36	D1	661.19	-1958.41					129	SEG43	-865.06	1958.41				
37	D0	762.94	-1958.41					130	SEG42	-966.81	1958.41				
38	DVSS	864.69	-1958.41					131	SEG41	-1068.56	1958.41				
39	CS	966.44	-1958.41					132	SEG40	-1170.31	1958.41				
40	R/W	1068.19	-1958.41					133	SEG39	-1272.06	1958.41				
41	D/C	1169.94	-1958.41					134	SEG38	-1373.81	1958.41				
42	RES	1271.69	-1958.41					135	SEG37	-1475.56	1958.41				
43	DVDD	1373.44	-1958.41					136	SEG36	-1577.31	1958.41				
44	BP	1475.19	-1958.41					137	SEG35	-1679.06	1958.41				
45	DUMMY1	1576.94	-1958.41					138	SEG34	-1780.81	1958.41				
46	ANNUN2	1678.69	-1958.41					139	SEG33	-1882.56	1958.41				
47	ANNUN1	1780.44	-1958.41					140	SEG32	-1984.31	1958.41				
48	ANNUN0	1882.19	-1958.41					141	SEG31	-2086.06	1958.41				
49	SEG119	1983.94	-1958.41					142	SEG30	-2187.81	1958.41				
50	SEG118	2085.69	-1958.41					143	SEG29	-2289.56	1958.41				
51	SEG117	2187.44	-1958.41					144	DUMMY	-2400.56	2035.37				
52	SEG116	2289.19	-1958.41					145	DUMMY	-2502.31	2035.37				
53	SEG115	2390.94	-1958.41					146	DUMMY	-2604.06	2035.37				
54	SEG114	2492.69	-1958.41					147	DUMMY	-2705.81	2035.37				
55	SEG113	2594.44	-1958.41												
56	SEG112	2696.19	-1958.41												
57	SEG111	2797.94	-1958.41												
58	SEG110	2899.69	-1958.41												

Die Size is 254 mil x 180 mil