



MOTOROLA

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilarly designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

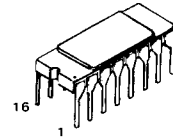
- Quiescent Current = 0.5 μ A/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

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CMOS LSI

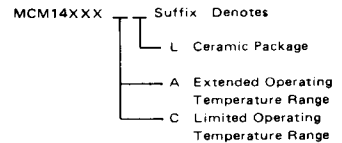
(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

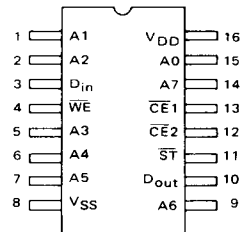


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mA _{dc}
Operating Temperature Range — AL Device	T_A	-55 to +125	$^{\circ}$ C
CL/CP Device		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD Vdc	T _{low} *		25°C			T _{high} *		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Noise Immunity # (V _{out} ≈ 0.8 Vdc) (V _{out} ≈ 1.0 Vdc) (V _{out} ≈ 1.5 Vdc) (V _{out} ≈ 0.8 Vdc) (V _{out} ≈ 1.0 Vdc) (V _{out} ≈ 1.5 Vdc)	V _{NL}	5.0	1.5	-	1.5	2.25	-	1.4	-	Vdc	
		10	3.0	-	3.0	4.50	-	2.9	-		
		15	4.5	-	4.5	6.75	-	4.4	-		
	V _{NH}	5.0	1.4	-	1.5	2.25	-	1.5	-	Vdc	
		10	2.9	-	3.0	4.50	-	3.0	-		
		15	4.4	-	4.5	6.75	-	4.5	-		
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mA _{dc}	
		10	-0.25	-	-0.2	-0.36	-	-0.14	-		
		15	-0.62	-	-0.5	-0.9	-	-0.35	-		
	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mA _{dc}	
		10	1.6	-	1.3	2.25	-	0.9	-		
		15	4.2	-	3.4	8.8	-	2.4	-		
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	mA _{dc}	
		10	-0.2	-	-0.16	-0.36	-	-0.12	-		
		15	-0.5	-	-0.4	-0.9	-	-0.3	-		
	Sink I _{OL}	5.0	0.52	-	0.44	0.88	-	0.36	-	mA _{dc}	
		10	1.3	-	1.1	2.25	-	0.9	-		
		15	3.6	-	3.0	8.8	-	2.4	-		
Input Current (AL Device)	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μA _{dc}	
Input Current (CL/CP Device)	I _{in}	15	-	±1.0	-	±0.00001	±1.0	-	±14	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	-	100	-	0.5	100	-	1800	μA _{dc}	
		10	-	200	-	1.0	200	-	3600		
		15	-	400	-	1.5	400	-	7200		
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	-	100	-	0.5	100	-	1800	μA _{dc}	
		10	-	200	-	1.0	200	-	3600		
		15	-	400	-	1.5	400	-	7200		
Total Supply Current** I _T (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.46 μA/kHz) f + I _{DD}							μA _{dc}	
		10	I _T = (2.91 μA/kHz) f + I _{DD}								
		15	I _T = (4.37 μA/kHz) f + I _{DD}								
Three-State Leakage Current (AL Device)	I _{TL}	15	-	±0.1	-	±0.00001	±0.1	-	±3.0	μA _{dc}	
Three-State Leakage Current (CL/CP Device)	I _{TL}	15	-	±1.0	-	±0.00001	±1.0	-	±7.5	μA _{dc}	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
 2.0 Vdc min @ V_{DD} = 10 Vdc
 2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	3	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	3	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Read Access Time from \overline{ST} or $\overline{CE2}$ $t_{acc} = (1.4 \text{ ns/pF}) C_L + 2480 \text{ ns}$ $t_{acc} = (0.7 \text{ ns/pF}) C_L + 690 \text{ ns}$ $t_{acc} = (0.5 \text{ ns/pF}) C_L + 393 \text{ ns}$	4, 5	$t_{acc}(R)$	5.0 10 15	400 150 115	2500 700 400	6000 2000 1500	ns
Output Enable Delay from $\overline{CE1}$ or $\overline{CE2}$	5, 6	$t_{acc}(\overline{CE}_n)$	5.0 10 15	70 25 20	300 100 70	900 300 225	ns
Setup Time from A_n to \overline{ST} or $\overline{CE2}$	4, 5, 6, 7	$t_{su}(A)$	5.0 10 15	1800 600 450	600 200 140	— — —	ns
Hold Time from A_n to \overline{ST} or $\overline{CE2}$	4, 5, 6, 7	$t_h(A)$	5.0 10 15	600 240 180	200 80 55	— — —	ns
Data Hold Time	7	$t_h(D)$	5.0 10 15	1400 500 375	480 160 110	— — —	ns
Data Setup Time	7	$t_{su}(D)$	5.0 10 15	3600 1800 1350	1200 600 420	— — —	ns
Write Enable Hold Time	7	$t_h(\overline{WE})$	5.0 10 15	150 60 45	50 20 15	— — —	ns
Write Enable Setup Time	7	$t_{su}(\overline{WE})$	5.0 10 15	720 240 180	240 80 55	— — —	ns
Write Enable to D_{out} Disable**	4	t_{WE}	5.0 10 15	720 240 180	240 80 55	— — —	ns
Strobe or $\overline{CE2}$ Pulse Width When Reading	4, 5, 6	$t_{WL}(R)$	5.0 10 15	1350 450 340	450 150 100	— — —	ns
Strobe, $\overline{CE1}$ or $\overline{CE2}$ Pulse Width When Writing	7	$t_{WL}(W)$	5.0 10 15	2400 1260 945	1200 600 420	— — —	ns
Write Recovery Time $t_W = (1.4 \text{ ns/pF}) C_L + 219 \text{ ns}$ $t_W = (0.7 \text{ ns/pF}) C_L + 70 \text{ ns}$ $t_W = (0.5 \text{ ns/pF}) C_L + 47.5 \text{ ns}$	4	$t_R(W)$	5.0 10 15	70 25 20	240 80 55	720 240 180	ns
$\overline{CE1}$ or $\overline{CE2}$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0 10 15	70 25 20	300 100 70	900 300 225	ns
Read Setup Time	4, 5	$t_{su}(R)$	5.0 10 15	0 0 0	-100 -40 -30	— — —	ns
Read Hold Time	4, 5	$t_h(R)$	5.0 10 15	540 240 180	180 60 45	— — —	ns
Read Cycle Time	4, 5	$t_{cyc}(R)$	5.0 10 15	— — —	2500 700 500	6000 2100 1575	ns
Write Cycle Time	7	$t_{cyc}(W)$	5.0 10 15	— — —	1400 700 500	4800 2100 1575	ns

* The formula given is for the typical characteristics only.

**10% output change into a 1.0 k Ω load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT

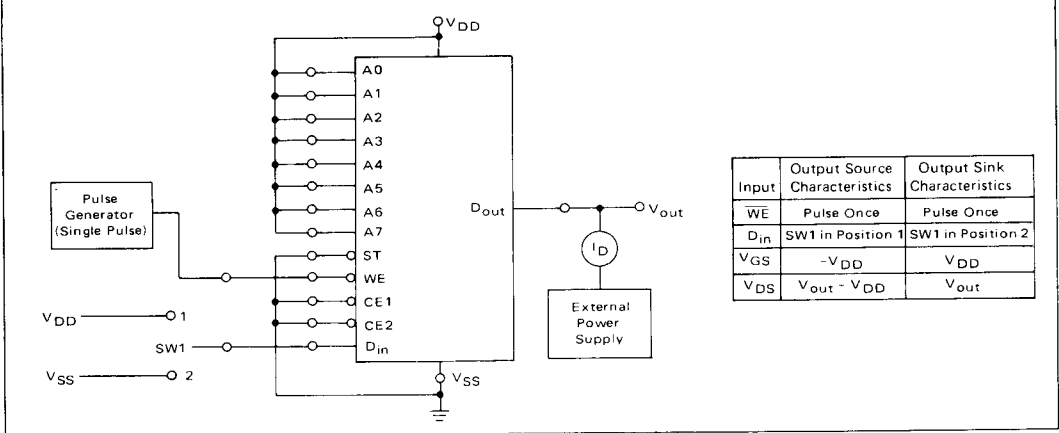


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

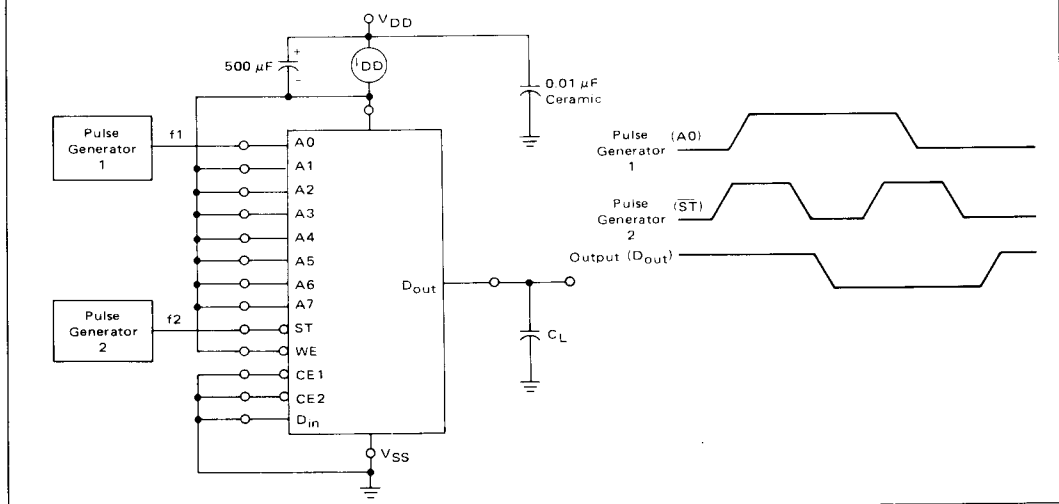
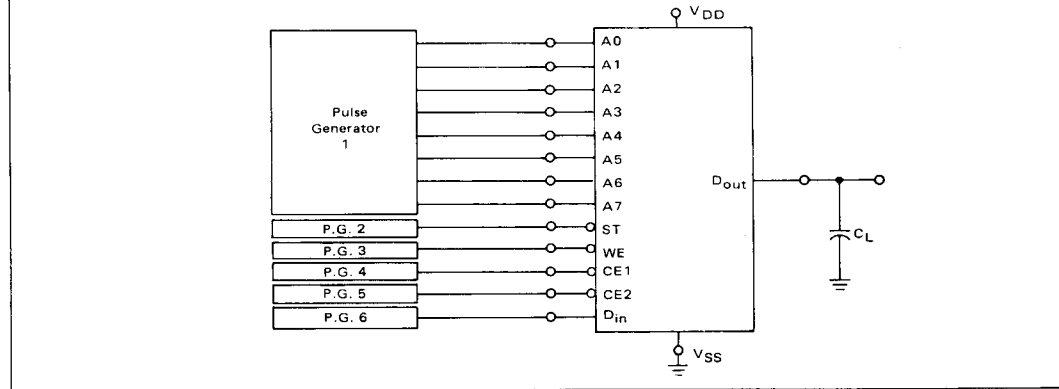


FIGURE 3 – AC TEST CIRCUIT



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FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY

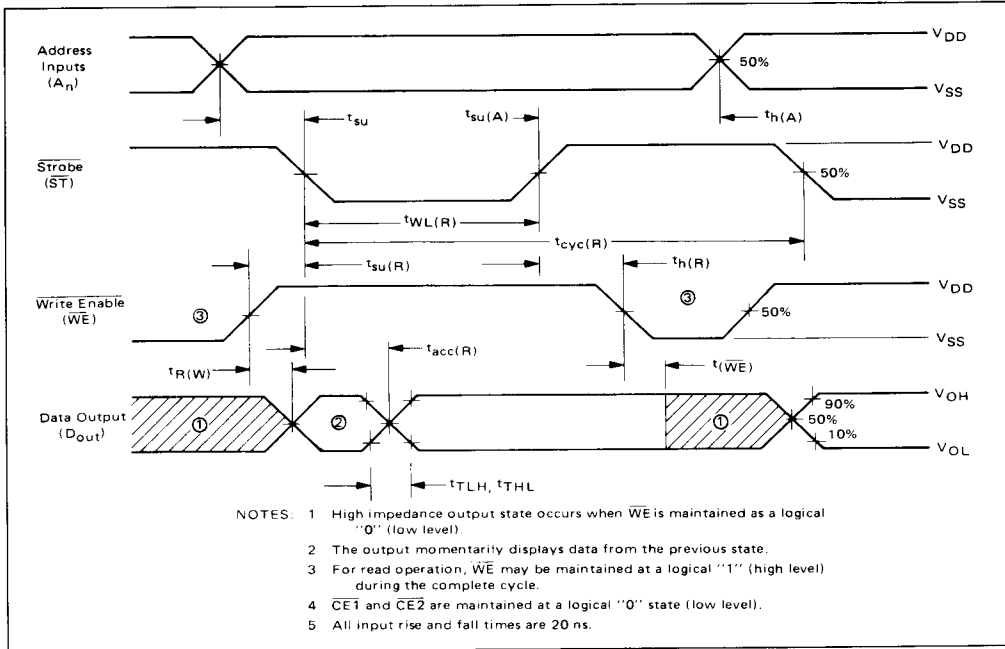
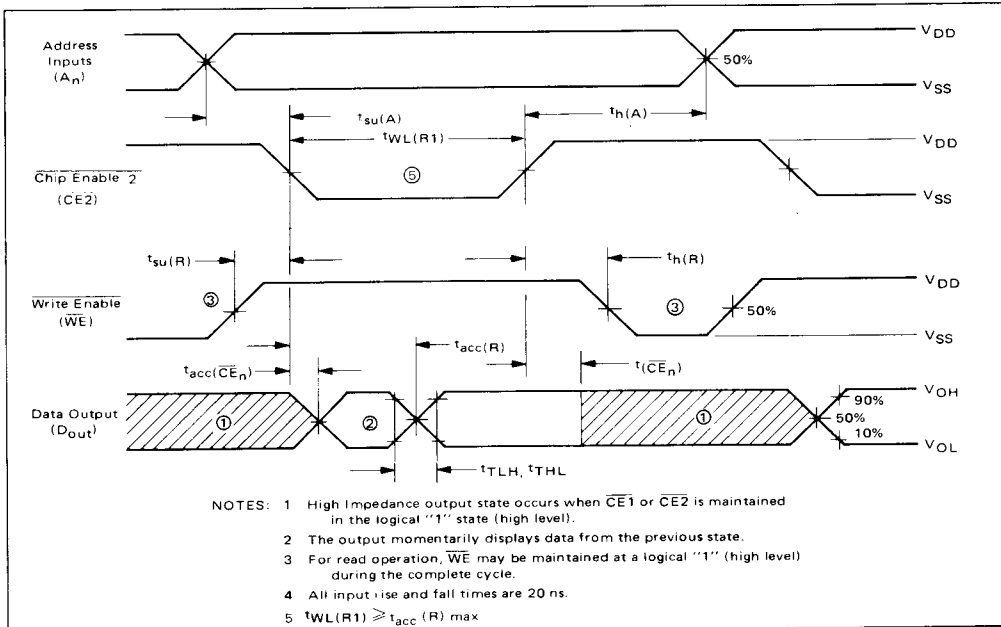
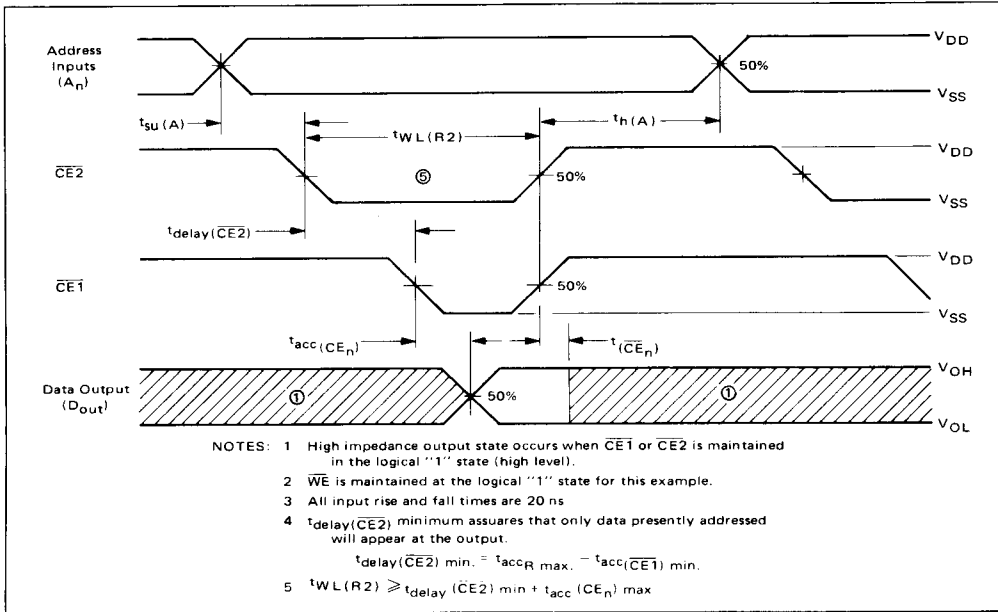


FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



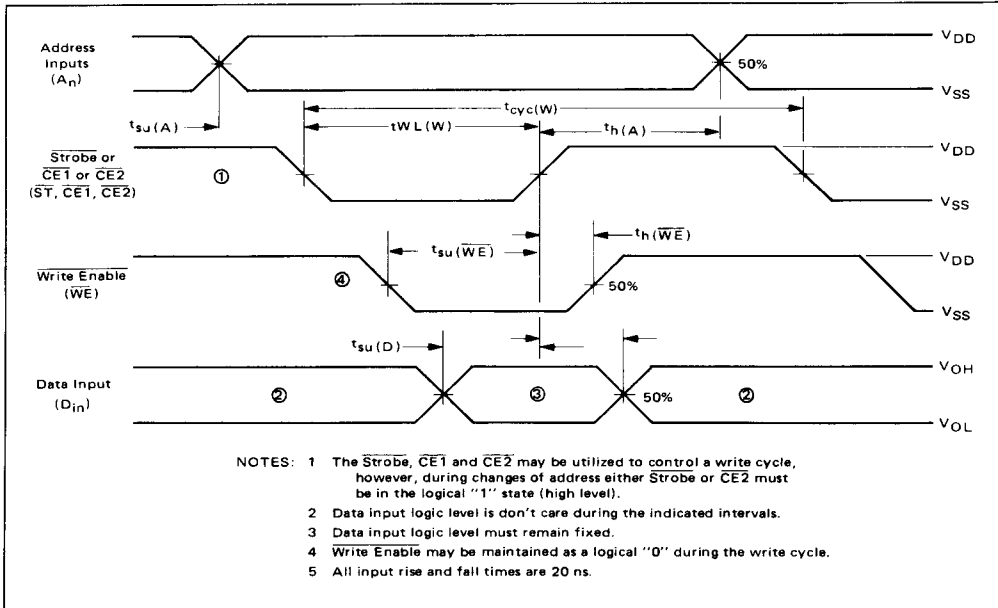
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FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY

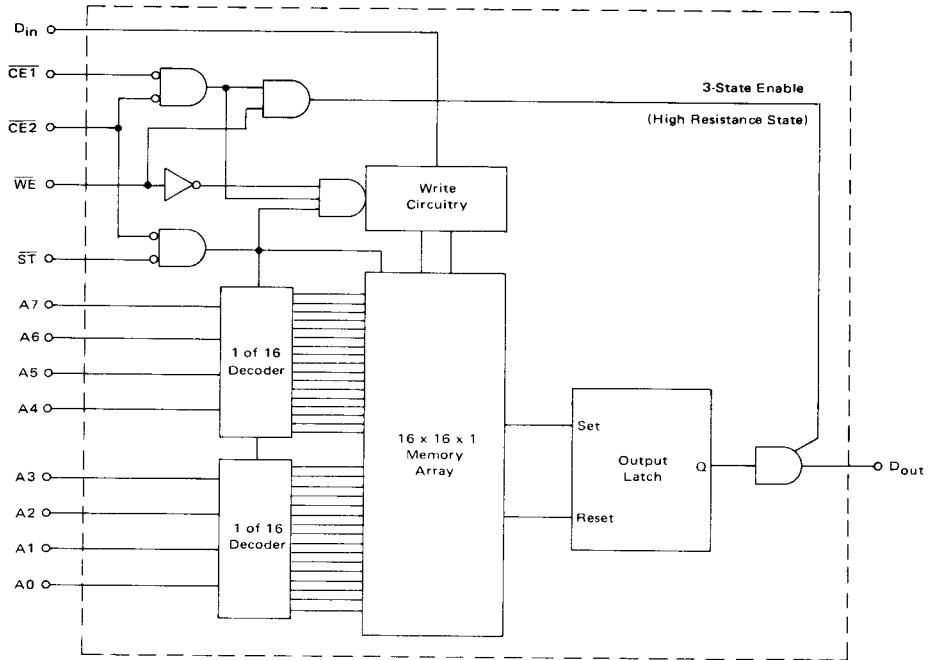


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FIGURE 7 – WRITE CYCLE WAVEFORMS



LOGIC/BLOCK DIAGRAM

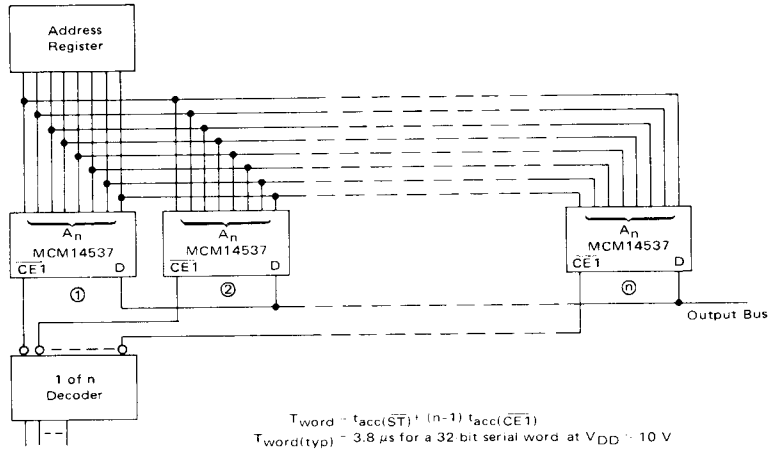


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FUNCTION	CE1	CE2	ST	WE	D _{in}	D _{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D _{out} will be active if CE1 and CE2 = "0" and WE = "1".
	X	1	X	X	X	R	CE2 = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D _{out} disabled in high resistance state	1	X	X	X	X	R	CE1 = "1" disables write cycle and D _{out} .
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	WE = "0" enables writing into memory if CE1, CE2, and ST = "0".
D _{out} enabled in active state	0	0	X	1	X	A	If ST = "1", the output stores and reads the previous data from or written into memory.
	0	0	0	1	X	A	The output reads the present contents that are addressed.
Read addressed memory location into output latch.	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D _{in} is written into memory and into the output latch.
Write disabled	1	X	X	X	X	R	WE = "1" is a read enable. WE = "0" is a write enable.
	X	1	X	X	X	R	
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

R = High resistance state at D_{out}
 A = An active level of either V_{SS} or V_{DD}
 R/A = An R or A condition depending on the don't care condition
 X = Don't care condition (must be in the "1" or "0" state)
 1 = A high level at V_{DD}
 0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES



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