

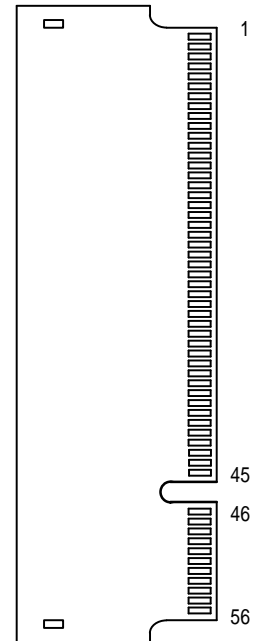
*Advance Information*  
**256KB Secondary Cache Module**  
**With Tag and Optional Dirty for**  
**486 Processor Systems**

These 256K Byte cache modules offer dual asynchronous 32K x 32 banks of memory. There is a 16K x 8 tag memory for main memory cacheability up to 64 Megabytes. The MCM32N865 and MCM32P865 include a 16K x 1 common I/O dirty bit for writeback cache capability. The modules are designed to support common 486 chipsets which utilize chip enable ( $\overline{CE}$ ) byte control and bank write enable ( $\overline{CWEx}$ ). The MCM32N864 and MCM32N865 operate at 5 V while the MCM32P864 and MCM32P865 operate at 3.3 V power. PD pins are provided for cache size identification at system startup

- 64MB of Cacheable Memory
- Low Profile Edge Connector: Burndy Part Number: CELP2X56SC3Z48
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Cycle Time: Up to External Processor Bus Speed of 33 MHz
- Cache Bank Write, Byte Chip Enable, Bank Output Enable
- Decoupling Capacitors are Used for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Planes
- 5 V and 3.3 V Power Supplies are Supported

**MCM32N864**  
**MCM32N865**  
**MCM32P864**  
**MCM32P865**

112-LEAD  
CARD EDGE  
CASE 1112-01  
TOP VIEW



This document contains information on a new product. Specifications and information herein are subject to change without notice.

**PIN ASSIGNMENT  
CACHE MODULE  
112 PIN CARDEDGE  
TOP VIEW**

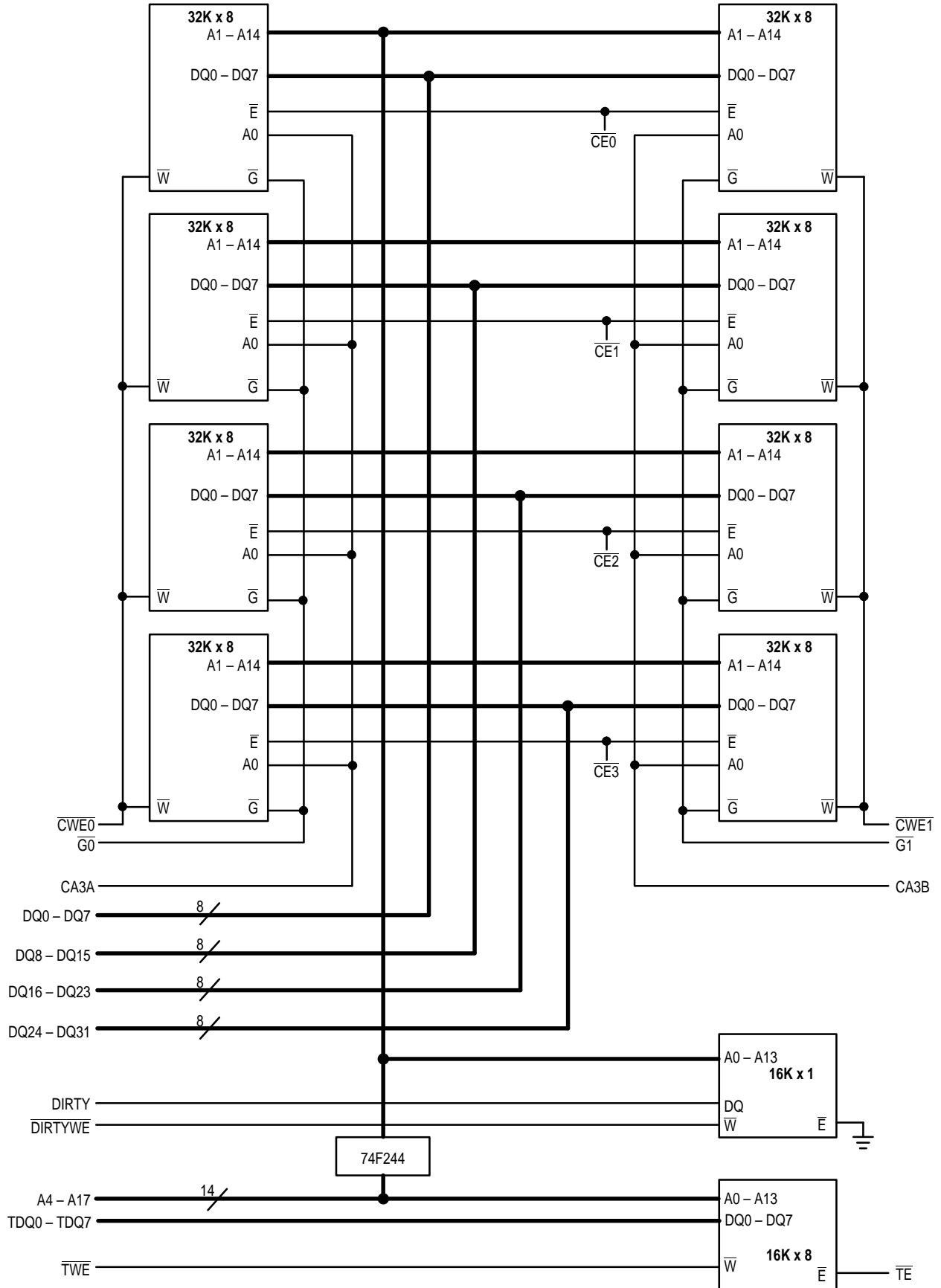
PD3	PD2	PD1	PD0	Cache Size	Dirty	Module
NC	NC	NC	NC	—	—	No Module
NC	GND	NC	NC	256KB	No	32N864 32P864
GND	GND	NC	NC	256KB	Yes	32N865 32P865

PIN NAMES	
A4 – A17	Address Inputs
CA3A, CA3B	Bank Address Inputs
CWEx	Bank Write Enable
CEx	Byte Chip Enable
G0, G1	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TDQ0 – TDQ8	Tag Data Input/Output
TWE	Tag Write Enable
TE	Tag Chip Enable
DIRTYWE	Dirty Write Enable
DIRTY	Dirty Input/Output
PD0 – PD3	Presence Detect
NC	No Connect
VCC5	+5 V Power Supply
VCC3	+3.3 V Power Supply
VSS	Ground

VSS	57	1	VSS
DQ0	58	2	DQ1
DQ2	59	3	DQ3
DQ4	60	4	DQ5
DQ6	61	5	DQ7
VCC5	62	6	VCC3
NC	63	7	NC
DQ8	64	8	DQ9
DQ10	65	9	DQ11
DQ12	66	10	DQ13
VSS	67	11	VSS
DQ14	68	12	DQ15
DQ16	69	13	DQ17
DQ18	70	14	DQ19
DQ20	71	15	DQ21
VCC5	72	16	VCC3
DQ22	73	17	DQ23
NC	74	18	NC
DQ24	75	19	DQ25
DQ26	76	20	DQ27
VSS	77	21	VSS
DQ28	78	22	DQ29
DQ30	79	23	DQ31
CA3B	80	24	NC
CA3A	81	25	NC
VCC5	82	26	VCC3
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	A17
NC	90	34	NC
VSS	91	35	VSS
NC	92	36	NC
TDQ0	93	37	TDQ1
TDQ2	94	38	TDQ3
TDQ4	95	39	TDQ5
VSS	96	40	VSS
TDQ6	97	41	TDQ7
NC	98	42	DIRTY*
TE	99	43	NC
TWE	100	44	CE0
VCC5	101	45	VCC3
VSS	102	46	VSS
NC	103	47	CE1
*DIRTYWE	104	48	CE2
NC	105	49	CE3
VCC5	106	50	VCC3
G0	107	51	G1
CWE0	108	52	CWE1
PD0	109	53	PD1
PD2	110	54	PD3
NC	111	55	NC
VSS	112	56	VSS

\* No Connect for MCM32N864 and MCM32P864

**MCM32N865**  
**486 256KB CACHE MODULE BLOCK DIAGRAM**  
**WITH 8 TAG BITS AND DIRTY**



**MCM32N864**  
**486 128KB CACHE MODULE BLOCK DIAGRAM**  
**WITH 8 TAG BITS**

