

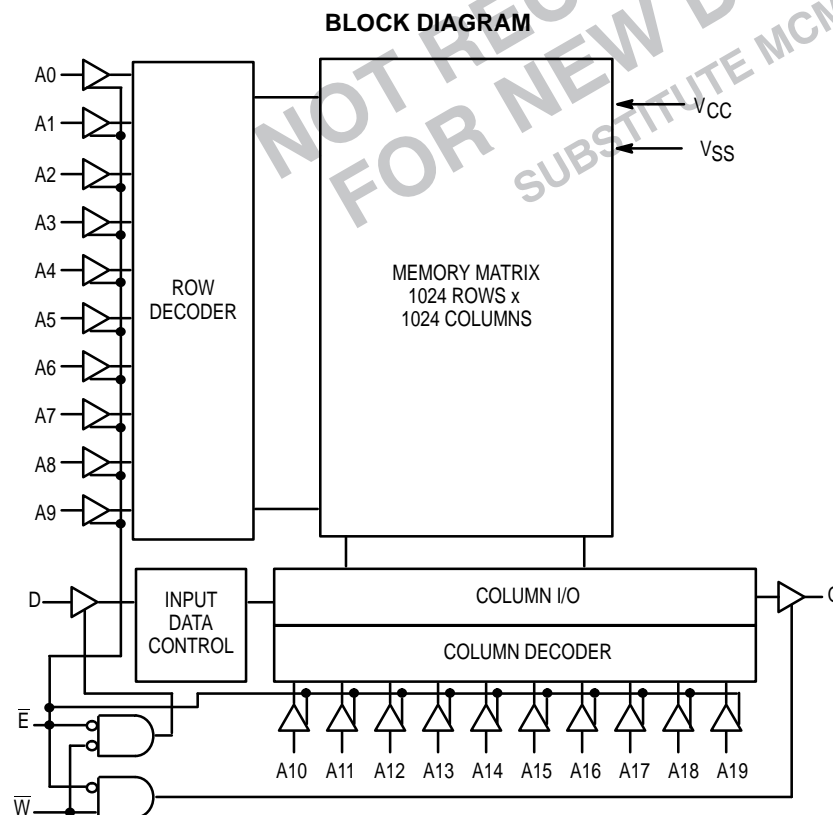
# 1M x 1 Bit Static Random Access Memory

The MCM6227A is a 1,048,576 bit static random-access memory organized as 1,048,576 words of 1 bit, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

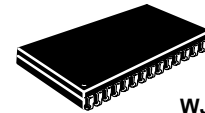
The MCM6227A is equipped with a chip enable ( $\bar{E}$ ) pin. In less than a cycle time after  $\bar{E}$  goes high, the part enters a low-power standby mode, remaining in that state until  $\bar{E}$  goes low again.

The MCM6227A is available in 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three-State Output
- Low Power Operation: 160/140/130/120 mA Maximum, Active AC



## MCM6227A



**WJ PACKAGE**  
**400 MIL SOJ**  
**CASE 810-03**

### PIN ASSIGNMENT

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| A0              | 1  | 28 | V <sub>CC</sub> |
| A1              | 2  | 27 | A19             |
| A2              | 3  | 26 | A18             |
| A3              | 4  | 25 | A17             |
| A4              | 5  | 24 | A16             |
| A5              | 6  | 23 | A15             |
| NC              | 7  | 22 | A14             |
| A6              | 8  | 21 | NC              |
| A7              | 9  | 20 | A13             |
| A8              | 10 | 19 | A12             |
| A9              | 11 | 18 | A11             |
| Q               | 12 | 17 | A10             |
| $\bar{W}$       | 13 | 16 | D               |
| V <sub>SS</sub> | 14 | 15 | $\bar{E}$       |

### PIN NAMES

|                 |                    |
|-----------------|--------------------|
| A0 – A19        | Address Inputs     |
| $\bar{W}$       | Write Enable       |
| $\bar{E}$       | Chip Enable        |
| D               | Data Input         |
| Q               | Data Output        |
| NC              | No Connection      |
| V <sub>CC</sub> | + 5 V Power Supply |
| V <sub>SS</sub> | Ground             |

## MCM6227A TRUTH TABLE

| $\bar{E}$ | $\bar{W}$ | Mode         | I/O Pin   | Cycle | Current            |
|-----------|-----------|--------------|-----------|-------|--------------------|
| H         | X         | Not Selected | High-Z    | —     | $I_{SB1}, I_{SB2}$ |
| L         | H         | Read         | $D_{out}$ | Read  | $I_{CCA}$          |
| L         | L         | Write        | High-Z    | Write | $I_{CCA}$          |

H = High, L = Low, X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating                                                   | Symbol            | Value                   | Unit        |
|----------------------------------------------------------|-------------------|-------------------------|-------------|
| Power Supply Voltage Relative to $V_{SS}$                | $V_{CC}$          | - 0.5 to 7.0            | V           |
| Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ | $V_{in}, V_{out}$ | - 0.5 to $V_{CC} + 0.5$ | V           |
| Output Current                                           | $I_{out}$         | $\pm 20$                | mA          |
| Power Dissipation                                        | $P_D$             | 1.1                     | W           |
| Temperature Under Bias                                   | $T_{bias}$        | - 10 to + 85            | $^{\circ}C$ |
| Operating Temperature                                    | $T_A$             | 0 to + 70               | $^{\circ}C$ |
| Storage Temperature                                      | $T_{stg}$         | - 55 to + 150           | $^{\circ}C$ |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 V \pm 10\%$ ,  $T_A = 0$  to  $70^{\circ}C$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

| Parameter                                | Symbol   | Min    | Max                 | Unit |
|------------------------------------------|----------|--------|---------------------|------|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.5    | 5.5                 | V    |
| Input High Voltage                       | $V_{IH}$ | 2.2    | $V_{CC} + 0.3^{**}$ | V    |
| Input Low Voltage                        | $V_{IL}$ | - 0.5* | 0.8                 | V    |

\*  $V_{IL}(\text{min}) = -0.5 V$  dc;  $V_{IL}(\text{min}) = -2.0 V$  ac (pulse width  $\leq 20$  ns).

\*\*  $V_{IH}(\text{max}) = V_{CC} + 0.3 V$  dc;  $V_{IH}(\text{max}) = V_{CC} + 2 V$  ac (pulse width  $\leq 20$  ns).

### DC CHARACTERISTICS AND SUPPLY CURRENTS

| Parameter                                                                                                                                                                                                        | Symbol       | Min | Typ*                    | Max                      | Unit    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----|-------------------------|--------------------------|---------|
| Input Leakage Current (All Inputs, $V_{in} = 0$ to $V_{CC}$ )                                                                                                                                                    | $I_{lkg(I)}$ | —   | —                       | $\pm 1$                  | $\mu A$ |
| Output Leakage Current ( $\bar{E} = V_{IH}$ , $V_{out} = 0$ to $V_{CC}$ )                                                                                                                                        | $I_{lkg(O)}$ | —   | —                       | $\pm 1$                  | $\mu A$ |
| AC Active Supply Current ( $I_{out} = 0$ mA, $V_{CC} = \text{max}$ )<br>MCM6227A-20: $t_{AVAV} = 20$ ns<br>MCM6227A-25: $t_{AVAV} = 25$ ns<br>MCM6227A-35: $t_{AVAV} = 35$ ns<br>MCM6227A-45: $t_{AVAV} = 45$ ns | $I_{CCA}$    | —   | 120<br>110<br>100<br>90 | 160<br>140<br>130<br>120 | mA      |
| AC Standby Current ( $V_{CC} = \text{max}$ , $\bar{E} = V_{IH}$ , $f = f_{max}$ )                                                                                                                                | $I_{SB1}$    | —   | 7                       | 20                       | mA      |
| CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2 V$ , $V_{in} \leq V_{SS} + 0.2 V$<br>or $\geq V_{CC} - 0.2 V$ , $V_{CC} = \text{max}$ , $f = 0$ MHz)                                                           | $I_{SB2}$    | —   | 4                       | 15                       | mA      |
| Output Low Voltage ( $I_{OL} = + 8.0$ mA)                                                                                                                                                                        | $V_{OL}$     | —   | —                       | 0.4                      | V       |
| Output High Voltage ( $I_{OH} = - 4.0$ mA)                                                                                                                                                                       | $V_{OH}$     | 2.4 | —                       | —                        | V       |

\* Typical values are measured at  $25^{\circ}C$ ,  $V_{CC} = 5 V$ .

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

| Characteristic                                                                    | Symbol            | Typ    | Max    | Unit |
|-----------------------------------------------------------------------------------|-------------------|--------|--------|------|
| Input Capacitance<br>All Inputs Except Clocks and D, Q<br>$\bar{E}$ and $\bar{W}$ | $C_{in}$          | 4<br>5 | 6<br>8 | pF   |
| Input and Output Capacitance<br>D, Q                                              | $C_{in}, C_{out}$ | 5      | 8      | pF   |

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V      Output Timing Measurement Reference Level ..... 1.5 V  
 Input Rise/Fall Time ..... 2 ns      Output Load ..... See Figure 1A  
 Input Timing Measurement Reference Level ..... 1.5 V

**READ CYCLE TIMING** (See Notes 1 and 2)

| Parameter                       | Symbol       | 6227A-20 |     | 6227A-25 |     | 6227A-35 |     | 6227A-45 |     | Unit | Notes   |
|---------------------------------|--------------|----------|-----|----------|-----|----------|-----|----------|-----|------|---------|
|                                 |              | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |         |
| Read Cycle Time                 | $t_{AVAV}$   | 20       | —   | 25       | —   | 35       | —   | 45       | —   | ns   | 2,3     |
| Address Access Time             | $t_{AVQV}$   | —        | 20  | —        | 25  | —        | 35  | —        | 45  | ns   |         |
| Enable Access Time              | $t_{ELQV}$   | —        | 20  | —        | 25  | —        | 35  | —        | 45  | ns   | 4       |
| Output Hold from Address Change | $t_{AXQX}$   | 5        | —   | 5        | —   | 5        | —   | 5        | —   | ns   |         |
| Enable Low to Output Active     | $t_{ELQX}$   | 5        | —   | 5        | —   | 5        | —   | 5        | —   | ns   | 5, 6, 7 |
| Enable High to Output High-Z    | $t_{EHQZ}$   | 0        | 9   | 0        | 10  | 0        | 12  | —        | 18  | ns   | 5, 6, 7 |
| Power Up Time                   | $t_{ELICCH}$ | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |         |
| Power Down Time                 | $t_{EHICCL}$ | —        | 20  | —        | 25  | —        | 35  | —        | 45  | ns   |         |

NOTES:

- $\bar{W}$  is high for read cycle.
- Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
- All timings are referenced from the last valid address to the first transitioning address.
- Addresses valid prior to or coincident with  $\bar{E}$  going low.
- At any given voltage and temperature,  $t_{EHQZ}$  max is less than  $t_{ELQX}$  min, both for a given device and from device to device.
- Transition is measured  $\pm 500 \text{ mV}$  from steady-state voltage with load of Figure 1B.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ( $\bar{E} \leq V_{IL}$ ).

**AC TEST LOADS**

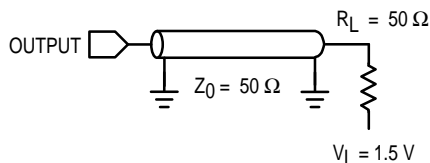


Figure 1A

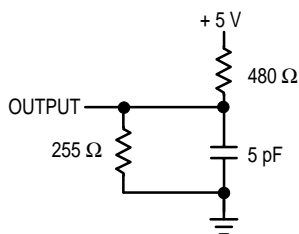
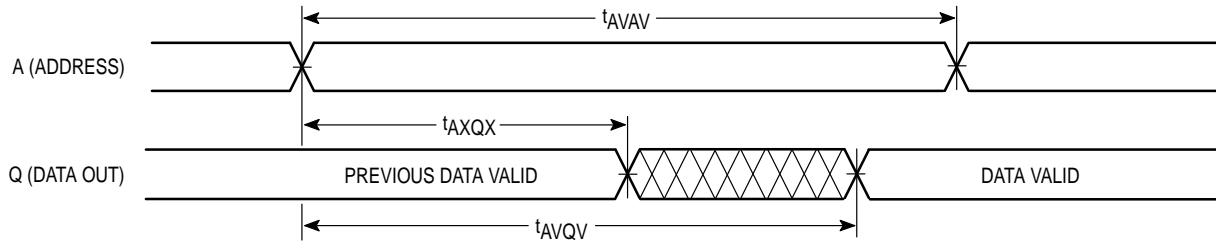


Figure 1B

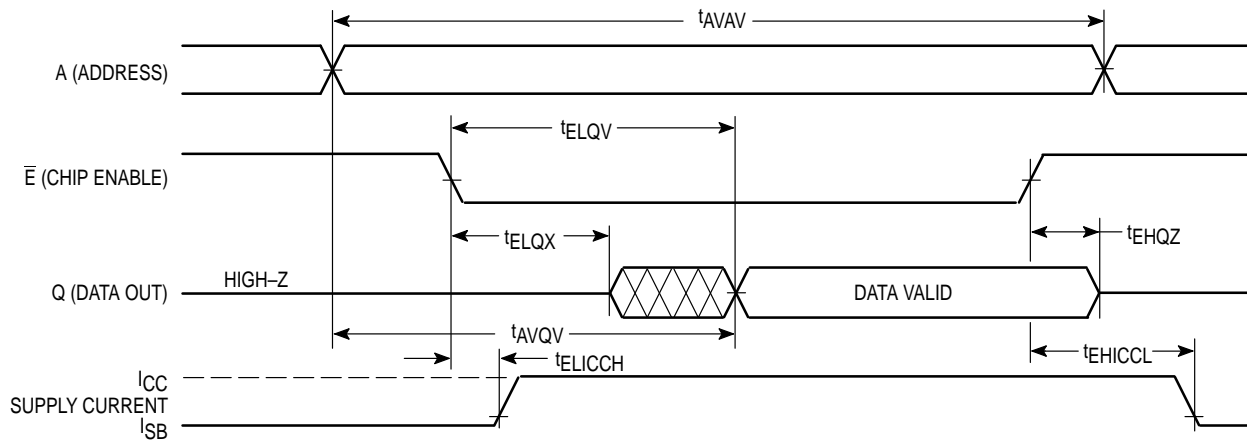
**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Notes 1, 2, and 8)



**READ CYCLE 2** (See Note 4)

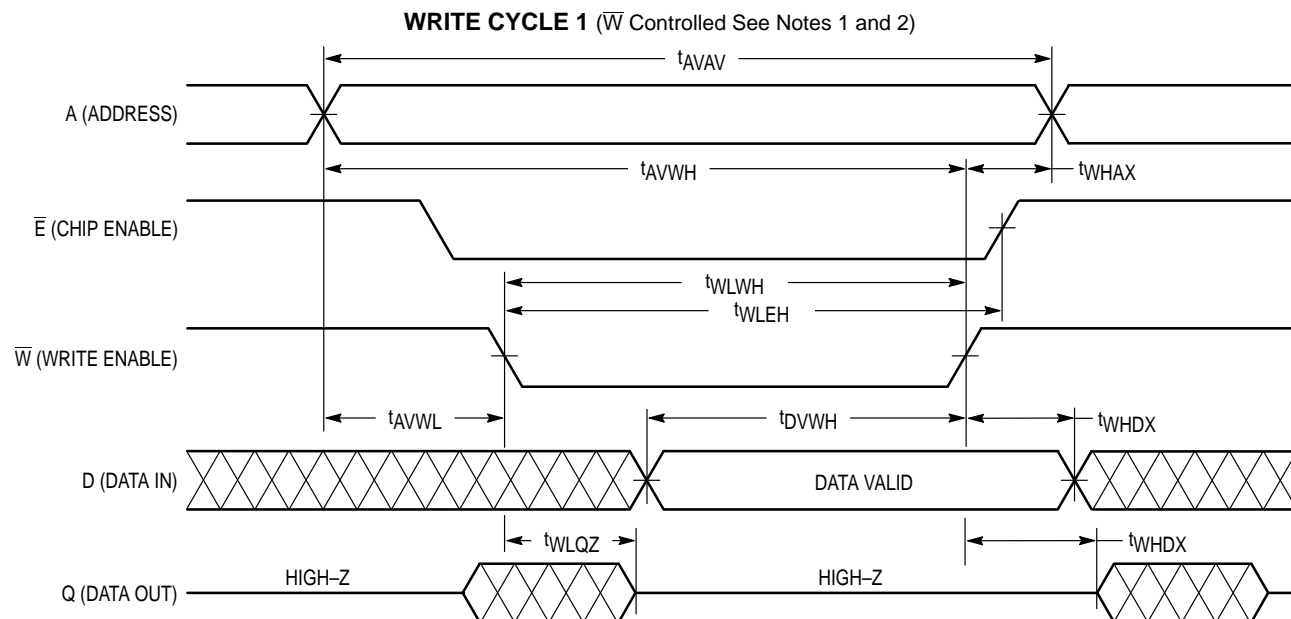


**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)

| Parameter                     | Symbol                     | 6227A-20 |     | 6227A-25 |     | 6227A-35 |     | 6227A-45 |     | Unit | Notes   |
|-------------------------------|----------------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|---------|
|                               |                            | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |         |
| Write Cycle Time              | $t_{AVAV}$                 | 20       | —   | 25       | —   | 35       | —   | 45       | —   | ns   | 3       |
| Address Setup Time            | $t_{AVWL}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |         |
| Address Valid to End of Write | $t_{AVWH}$                 | 15       | —   | 17       | —   | 20       | —   | 25       | —   | ns   |         |
| Write Pulse Width             | $t_{WLWH}$ ,<br>$t_{WLEH}$ | 15       | —   | 17       | —   | 20       | —   | 25       | —   | ns   |         |
| Data Valid to End of Write    | $t_{DVWH}$                 | 10       | —   | 10       | —   | 15       | —   | 20       | —   | ns   |         |
| Data Hold Time                | $t_{WHDX}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |         |
| Write Low to Data High-Z      | $t_{WLQZ}$                 | 0        | 9   | 0        | 10  | 0        | 15  | 0        | 20  | ns   | 4, 5, 6 |
| Write High to Output Active   | $t_{WHQX}$                 | 5        | —   | 5        | —   | 5        | —   | 5        | —   | ns   | 4, 5, 6 |
| Write Recovery Time           | $t_{WHAX}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |         |

**NOTES:**

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.



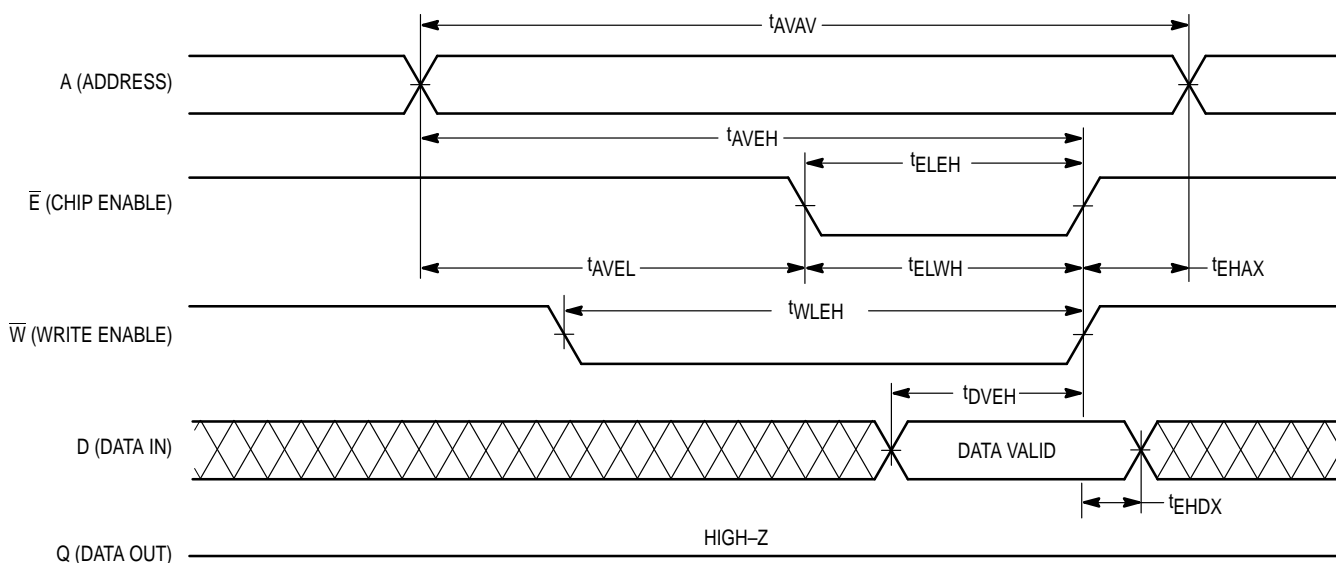
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1 and 2)

| Parameter                     | Symbol                     | 6227A-20 |     | 6227A-25 |     | 6227A-35 |     | 6227A-45 |     | Unit | Notes |
|-------------------------------|----------------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|-------|
|                               |                            | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |       |
| Write Cycle Time              | $t_{AVAV}$                 | 20       | —   | 25       | —   | 35       | —   | 45       | —   | ns   | 3     |
| Address Setup Time            | $t_{AVEL}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |       |
| Address Valid to End of Write | $t_{AVEH}$                 | 15       | —   | 17       | —   | 20       | —   | 25       | —   | ns   |       |
| Enable to End of Write        | $t_{ELEH}$ ,<br>$t_{ELWH}$ | 15       | —   | 17       | —   | 20       | —   | 25       | —   | ns   | 4, 5  |
| Write Pulse Width             | $t_{WLEH}$                 | 15       | —   | 17       | —   | 20       | —   | 25       | —   | ns   |       |
| Data Valid to End of Write    | $t_{DVEH}$                 | 10       | —   | 10       | —   | 15       | —   | 20       | —   | ns   |       |
| Data Hold Time                | $t_{EHDX}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |       |
| Write Recovery Time           | $t_{EHAX}$                 | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   |       |

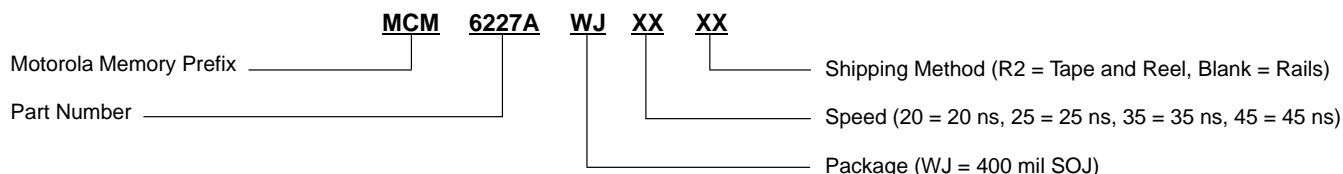
**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
5. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance state.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled See Notes 1 and 2)



**ORDERING INFORMATION**  
(Order by Full Part Number)

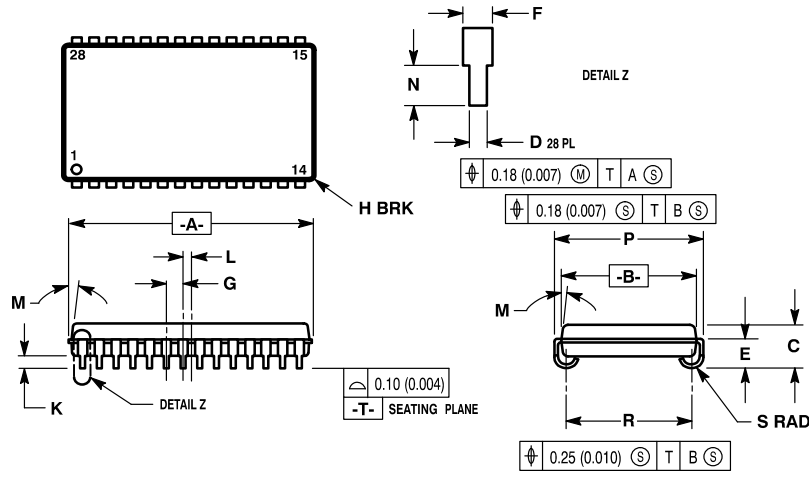


Full Part Numbers —

|              |                |
|--------------|----------------|
| MCM6227AWJ20 | MCM6227AWJ20R2 |
| MCM6227AWJ25 | MCM6227AWJ25R2 |
| MCM6227AWJ35 | MCM6227AWJ35R2 |
| MCM6227AWJ45 | MCM6227AWJ45R2 |

# PACKAGE DIMENSIONS


28 LEAD  
400 MIL SOJ  
CASE 810-03



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 18.29       | 18.54 | 0.720     | 0.730 |
| B   | 10.04       | 10.28 | 0.395     | 0.405 |
| C   | 3.26        | 3.75  | 0.128     | 0.148 |
| D   | 0.39        | 0.50  | 0.015     | 0.020 |
| E   | 2.24        | 2.48  | 0.088     | 0.098 |
| F   | 0.67        | 0.81  | 0.026     | 0.032 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| H   | —           | 0.50  | —         | 0.020 |
| K   | 0.89        | 1.14  | 0.035     | 0.045 |
| L   | 0.64 BSC    |       | 0.025 BSC |       |
| M   | 0°          | 5°    | 0°        | 5°    |
| N   | 0.76        | 1.14  | 0.030     | 0.045 |
| P   | 11.05       | 11.30 | 0.435     | 0.445 |
| R   | 9.15        | 9.65  | 0.360     | 0.380 |
| S   | 0.77        | 1.01  | 0.030     | 0.040 |

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MCM6227A/D

