

1M x 1 Bit Static Random Access Memory

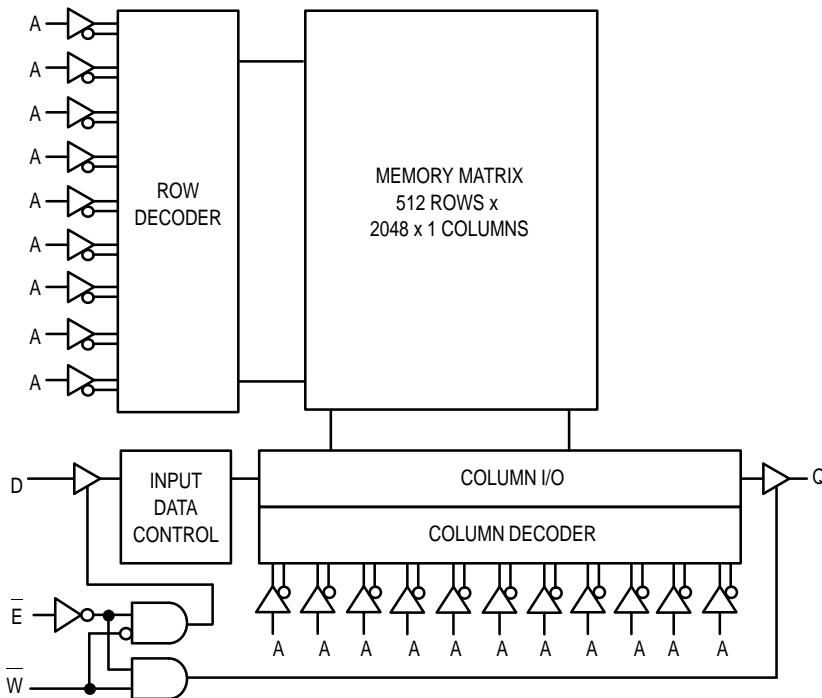
The MCM6227B is a 1,048,576 bit static random-access memory organized as 1,048,576 words of 1 bit. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227B is each equipped with a chip enable (\bar{E}) pin. This feature provides reduced system power requirements without degrading access time performance.

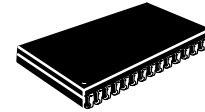
The MCM6227B is available in 300 mil and 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V \pm 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three-State Output
- Low Power Operation: 115/110/105/100/95 mA Maximum, Active AC

BLOCK DIAGRAM



MCM6227B



J PACKAGE
300 MIL SOJ
CASE 810B-03

WJ PACKAGE
400 MIL SOJ
CASE 810-03

PIN ASSIGNMENT

A	1	28	VCC
A	2	27	A
A	3	26	A
A	4	25	A
A	5	24	A
A	6	23	A
NC	7	22	A
A	8	21	NC*
A	9	20	A
A	10	19	A
A	11	18	A
Q	12	17	A
\bar{W}	13	16	D
VSS	14	15	\bar{E}

PIN NAMES

A	Address Inputs
\bar{W}	Write Enable
E	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
VCC	+ 5 V Power Supply
VSS	Ground

*If not used for no connect, then do not exceed voltages of - 0.5 to VCC + 0.5 V. This pin is used for manufacturing diagnostics.

TRUTH TABLE

E	W	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I _{SB1} , I _{SB2}
L	H	Read	D _{out}	Read	I _{CCA}
L	L	Write	High-Z	Write	I _{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V _{SS}	V _{CC}	-0.5 to 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	-0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 20	mA
Power Dissipation	P _D	1.1	W
Temperature Under Bias	T _{bias}	-10 to +85	°C
Operating Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3**	V
Input Low Voltage	V _{IL}	-0.5*	0.8	V

* V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 20 ns).

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{kg(I)}	—	± 1	μA
Output Leakage Current (E = V _{IH} , V _{out} = 0 to V _{CC})	I _{kg(O)}	—	± 1	μA
AC Active Supply Current (I _{out} = 0 mA, V _{CC} = max) MCM6227B-15: t _{AVAV} = 15 ns MCM6227B-17: t _{AVAV} = 17 ns MCM6227B-20: t _{AVAV} = 20 ns MCM6227B-25: t _{AVAV} = 25 ns MCM6227B-35: t _{AVAV} = 35 ns	I _{CCA}	—	115 110 105 100 95	mA
AC Standby Current (V _{CC} = max, E = V _{IH} , f ≤ f _{max}) MCM6227B-15: t _{AVAV} = 15 ns MCM6227B-17: t _{AVAV} = 17 ns MCM6227B-20: t _{AVAV} = 20 ns MCM6227B-25: t _{AVAV} = 25 ns MCM6227B-35: t _{AVAV} = 35 ns	I _{SB1}	—	40 35 30 25 20	mA
CMOS Standby Current (E ≥ V _{CC} - 0.2 V, V _{in} ≤ V _{SS} + 0.2 V or ≥ V _{CC} - 0.2 V, V _{CC} = max, f = 0 MHz)	I _{SB2}	—	5	mA
Output Low Voltage (I _{OL} = +8.0 mA)	V _{OL}	—	0.4	V
Output High Voltage (I _{OH} = -4.0 mA)	V _{OH}	2.4	—	V

CAPACITANCE ($f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
All Inputs Except Clocks and D, Q E and W		5	8	
Input and Output Capacitance	D, Q C_{in}, C_{out}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Pulse Levels 0 to 3.0 V Output Timing Measurement Reference Level 1.5 V
 Input Rise/Fall Time 2 ns Output Load See Figure 1a
 Input Timing Measurement Reference Level 1.5 V

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	—	6	—	7	—	7	—	8	—	8	ns	5, 6, 7

NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with E going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured $\pm 500 \text{ mV}$ from steady-state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($E \leq V_{IL}$).

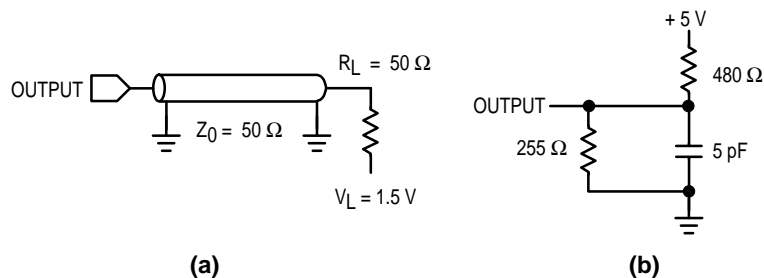
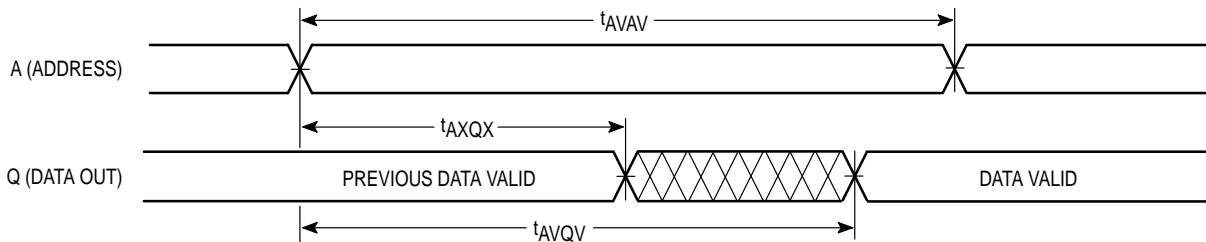


Figure 1. AC Test Loads

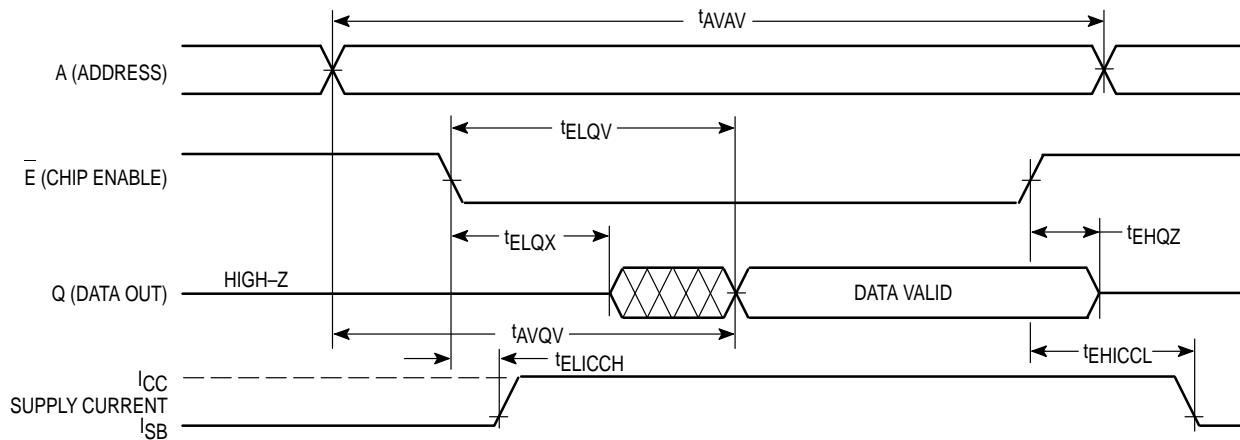
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)



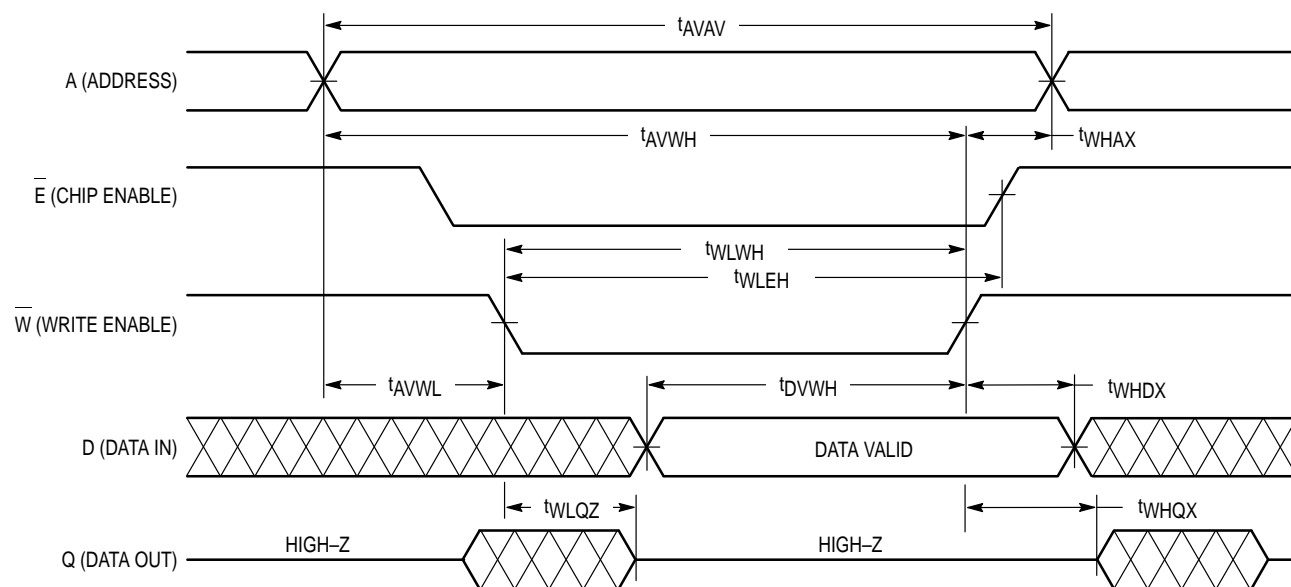
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	—	6	—	7	—	7	—	8	—	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 (\overline{W} Controlled See Notes 1 and 2)

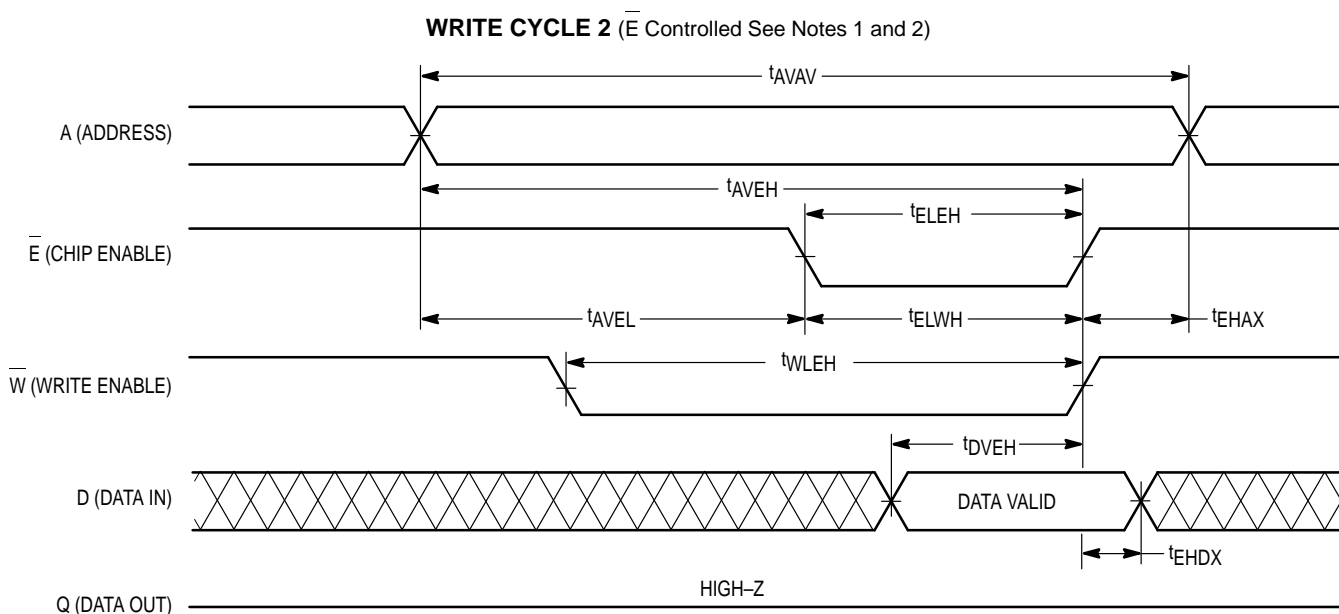


WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

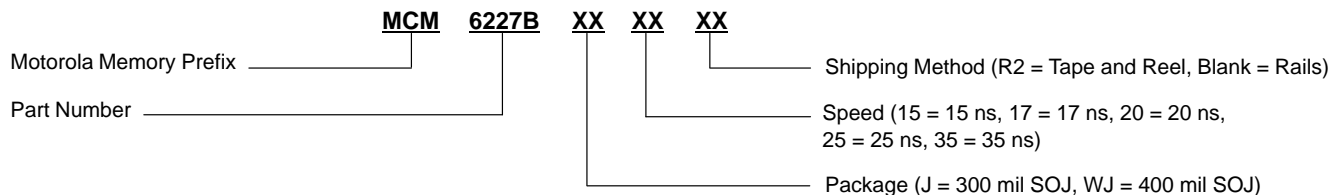
Parameter	Symbol	6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH} , t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	4, 5
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
5. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high-impedance state.



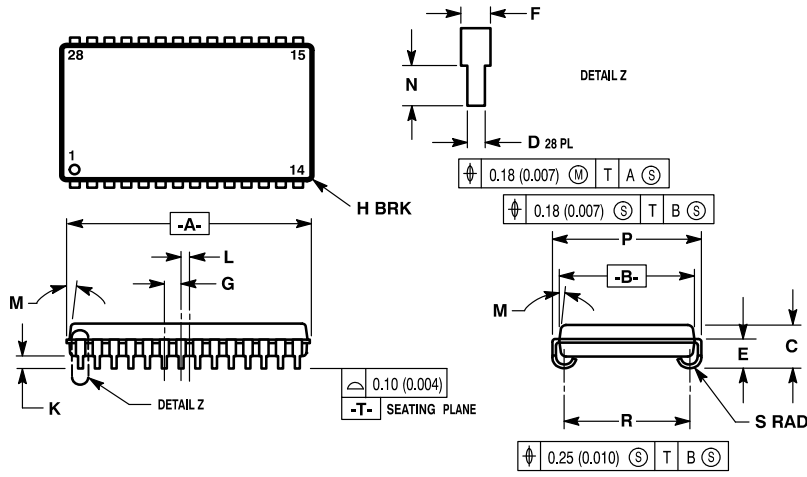
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM6227BJ15	MCM6227BJ15R2	MCM6227BWJ15	MCM6227BWJ15R2
	MCM6227BJ17	MCM6227BJ17R2	MCM6227BWJ17	MCM6227BWJ17R2
	MCM6227BJ20	MCM6227BJ20R2	MCM6227BWJ20	MCM6227BWJ20R2
	MCM6227BJ25	MCM6227BJ25R2	MCM6227BWJ25	MCM6227BWJ25R2
	MCM6227BJ35	MCM6227BJ35R2	MCM6227BWJ35	MCM6227BWJ35R2

PACKAGE DIMENSIONS

28 LEAD 400 MIL SOJ CASE 810-03

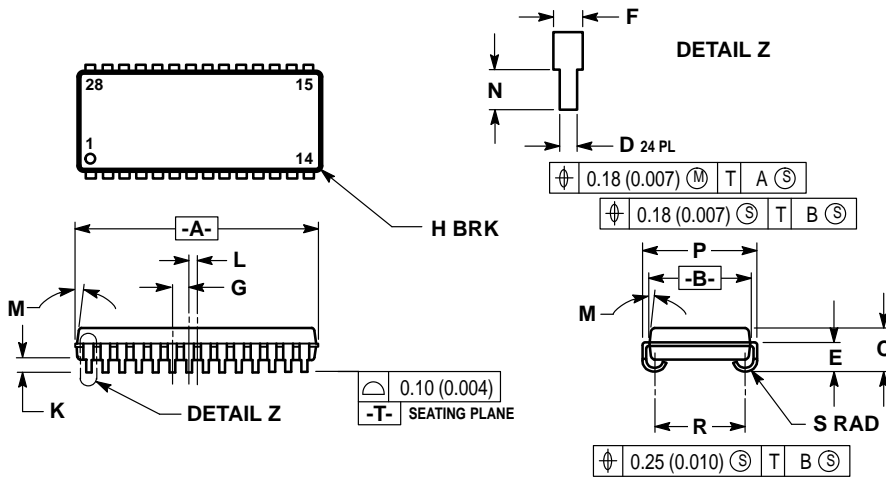


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040


28 LEAD 300 MIL SOJ CASE 810B-03



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. 810B-01 AND -02 OBSOLETE, NEW STANDARD 810B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

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