MCM64AF32

Product Preview

256K Asynchronous Secondary Cache Module for Pentium™

The MCM64AF32 is designed to provide 256K of asynchronous L2 cache for the Pentium microprocessor in conjunction with Intel's Triton chip set. The module is configured as 32K x 64 bits in a 160 pin card edge connector. The module uses eight Motorola 3.3 V 32K x 8 FSRAMs for the cache memory, one Motorola 5 V 32K x 8 FSRAM for the tag RAM, and an upper order address latch.

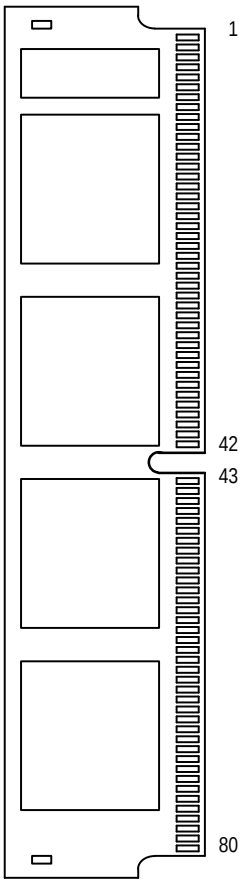
Eight write enables are provided for byte write control.

PD0–PD4 identify density and functionality.

This cache module is plug and pin compatible with the other members of Motorola's Triton chip set module family, the MCM72JG32SG66 (a 256K byte pipelined BurstRAM module) and the MCM72JG64SG66 (a 512K byte pipelined BurstRAM module).

- Low–Cost Asynchronous Solution for Triton Chip Set
- All Cache Data Inputs and Outputs are LVTTL (3.3 V I/O) Compatible
- All Tag I/Os are TTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 15 ns for Data RAMs and Tag RAM
- Decoupling Capacitors for each Fast Static RAM and Logic Device
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 160 Pin Card Edge Module
- Burndy Connector, Part Number: CELP2X80SC3Z48

160–LEAD CARD EDGE CASE TBD* TOP VIEW



* SEE BACK PAGE FOR PRELIMINARY CASE OUTLINE.

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Pentium is a trademark of Intel Corp.

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MOTOROLA

PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
(RSVD) NC	86	6	NC (RSVD)
$V_{CC}5$	87	7	$V_{CC}3$
(RSVD) NC	88	8	TWE
(CADV) CAA4	89	9	CAA3 (CADS)
V_{SS}	90	10	V_{SS}
COE	91	11	CWE4
CWE5	92	12	CWE6
CWE7	93	13	CWE0
CWE1	94	14	CWE2
$V_{CC}5$	95	15	$V_{CC}3$
CWE3	96	16	CAB4 (CCS)
CAB3	97	17	NC (GWE)
CALE	98	18	NC (BWE)
V_{SS}	99	19	V_{SS}
(RSVD) NC	100	20	NC (A3)
(A4) NC	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
$V_{CC}5$	105	25	$V_{CC}3$
A17	106	26	NC (A18)
V_{SS}	107	27	V_{SS}
A9	108	28	A12
A14	109	29	A13
A15	110	30	NC (ADSP)
(RSVD) NC	111	31	NC (CS/ECS1)
PD0	112	32	NC (ECS2)
PD2	113	33	PD1
PD4	114	34	PD3
V_{SS}	115	35	V_{SS}
(CLK0) NC	116	36	NC (CLK1)
V_{SS}	117	37	V_{SS}
DQ63	118	38	DQ62
$V_{CC}5$	119	39	$V_{CC}3$
DQ61	120	40	DQ60
DQ59	121	41	DQ58
DQ57	122	42	DQ56
V_{SS}	123	43	V_{SS}
DQ55	124	44	DQ54
DQ53	125	45	DQ52
DQ51	126	46	DQ50
DQ49	127	47	DQ48
V_{SS}	128	48	V_{SS}
DQ47	129	49	DQ46
DQ45	130	50	DQ44
DQ43	131	51	DQ42
$V_{CC}5$	132	52	$V_{CC}3$
DQ41	133	53	DQ40
DQ39	134	54	DQ38
DQ37	135	55	DQ36
V_{SS}	136	56	V_{SS}
DQ35	137	57	DQ34
DQ33	138	58	DQ32
DQ31	139	59	DQ30
$V_{CC}5$	140	60	$V_{CC}3$
DQ29	141	61	DQ28
DQ27	142	62	DQ26
DQ25	143	63	DQ24
V_{SS}	144	64	V_{SS}
DQ23	145	65	DQ22
DQ21	146	66	DQ20
DQ19	147	67	DQ18
$V_{CC}5$	148	68	$V_{CC}3$
DQ17	149	69	DQ16
DQ15	150	70	DQ14
DQ13	151	71	DQ12
V_{SS}	152	72	V_{SS}
DQ11	153	73	DQ10
DQ9	154	74	DQ8
DQ7	155	75	DQ6
$V_{CC}5$	156	76	$V_{CC}3$
DQ5	157	77	DQ4
DQ3	158	78	DQ2
DQ1	159	79	DQ0
V_{SS}	160	80	V_{SS}

PRESENCE DETECT TABLE

Cache Size and Functionality	Module	PD4	PD3	PD2	PD1	PD0
256KB Async	MCM64AF32	V_{SS}	NC	V_{SS}	V_{SS}	NC
512KB Async	—	V_{SS}	V_{SS}	NC	V_{SS}	NC
256K Burst	—	V_{SS}	NC	V_{SS}	NC	V_{SS}
256K Pipe Burst	MCM72JG32	V_{SS}	NC	V_{SS}	NC	NC
512K Burst	—	V_{SS}	V_{SS}	NC	NC	V_{SS}
512K Pipe Burst	MCM72JG64	V_{SS}	V_{SS}	NC	NC	NC
512K 2–Bank Burst	—	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}

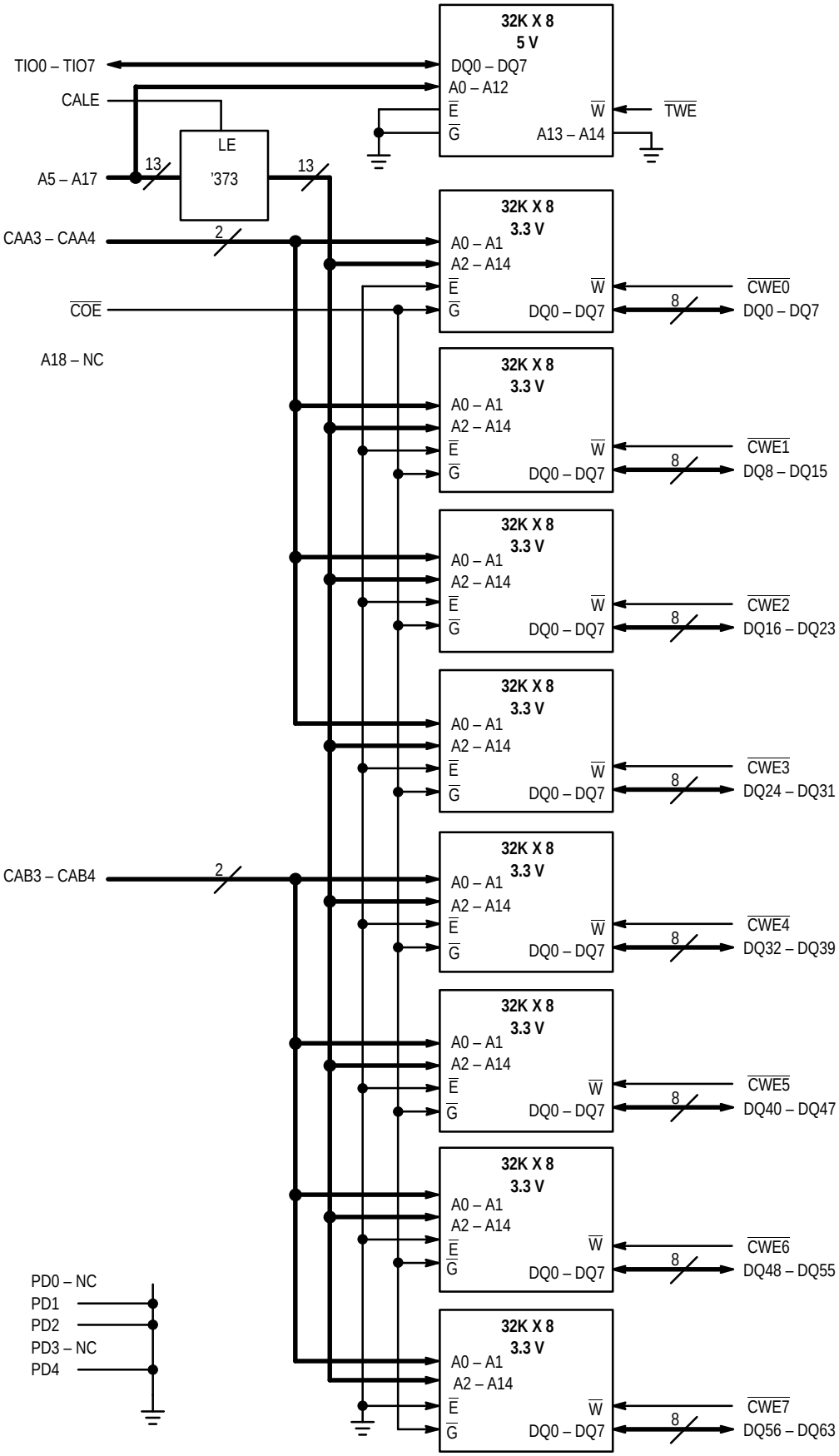
PIN NAMES

TIO0 – TIO7 . . . . . Tag RAM I/O
TWE . . . . . Tag Write Enable
CALE . . . . . Address Latch Enable
A5 – A17 . . . . . Address Inputs
CWE0 – CWE7 . . . . . Cache Write Enable
CAA3 –CAA4 . . . . . Cache Address A
CAB3 – CAB4 . . . . . Cache Address B
COE . . . . . Cache Output Enable
DQ0 – DQ63 . . . . . Data Input/Output
PD0 – PD4 . . . . . Presence Detect
$V_{CC}3$ . . . . . + 3.3 V Power Supply
$V_{CC}5$ . . . . . + 5.0 V Power Supply
V_{SS} . . . . . Ground
NC . . . . . No Connection

For proper operation of the device, V_{SS} must be connected to ground.

NOTE: Signals in parentheses indicate pin designations for burstable members of the Triton chip set module family.

MCM64AF32 MODULE BLOCK DIAGRAM



PIN DESCRIPTIONS

160–Lead Card Edge Pin Locations	Symbol	Type	Description
21, 22, 23, 24, 28, 29, 102, 103, 104, 106, 108, 109, 110	A5 – A17	Input	Address Inputs: These inputs are latched into data RAMs and must meet setup and hold times. The tag RAM addresses are not latched. (See Block Diagram).
9, 89	CAA3, CAA4	Input	Cache Address A: Low order address inputs for bursting. Not latched.
16, 97	CAB3, CAB4	Input	Cache Address B: Low order address inputs for bursting. Not latched.
98	CALE	Input	Address Latch Enable: Active low signal latches A5 – A17.
11, 12, 13, 14, 92, 93, 94, 96	$\overline{\text{CWE0}}$ – $\overline{\text{CWE7}}$	Input	Cache Data Write Enable: Active low write signal for data RAMs.
8	$\overline{\text{TWE}}$	Input	Tag Write Enable: Active low write signal for tag RAMs.
—	$\overline{\text{CS}}$	Input	Chip Select: Active low chip enable for tag and data RAMs. Not used.
91	$\overline{\text{COE}}$	Input	Cache Output Enable: Asynchronous active low output enable for data RAMs.
38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159	DQ0 – DQ63	I/O	Data I/O
2, 3, 4, 5, 82, 83, 84, 85	TIO0 – TIO7	I/O	Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles.
33, 34, 112, 113, 114	PD0 – PD4		Presence Detect: See Presence Detect Table.
7, 15, 25, 39, 52, 60, 68, 76	$V_{CC}3$	Supply	Power Supply: 3.3 V ± 5%.
87, 95, 105, 119, 132, 140, 148, 156	$V_{CC}5$	Supply	Power Supply: 5.0 V ± 5%.
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	V_{SS}	Supply	Ground
6, 17, 18, 20, 26, 30, 31, 32, 36, 86, 88, 100, 101, 111, 116	NC	—	No Connection: There is no connection to the module.

TRUTH TABLE FOR TAG AND DATA RAMs (X = Don't Care)

$\overline{COE}$	$\overline{CWE}$	Mode	V_{CC} Current	Output	Cycle
H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Power Supply Voltage	for Tag for Data	V_{CC5} V_{CC3}	– 0.5 to + 7.0 – 0.5 to + 5.0	V
Voltage Relative to V_{SS}		V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5*	V
Output Current (per I/O)		I_{out}	± 20	mA
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_A	0 to + 70	°C
Storage Temperature – Plastic		T_{stg}	– 55 to + 125	°C

* For data RAMs, V_{CC} + 2.0 V ac to V_{SS} – 2.0 V ac (pulse width ≤ 20 ns).

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}3$ = 3.3 V ± 5%, V_{CC5} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	Tag RAM Data RAM and Latch	V_{CC}	4.75 3.135	5.0 3.3	5.25 3.465	V
Input High Voltage		V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage		V_{IL}	– 0.5**	0.0	0.8	V

* For Tag, V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns).
For Data, V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min)).

** For Tag, V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
For Data, V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min)).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 2	μA
Output Leakage Current ($\overline{COE}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 2	μA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
CMOS Output Low Voltage (I_{OL} = 100 μA)	V_{OL2}	—	0.1	V
CMOS Output High Voltage (I_{OH} = – 100 μA)	V_{OH2}	V_{CC} – 0.1	—	V

NOTE: NOTE: Good decoupling of the local power supply should always be used.

POWER SUPPLY CURRENTS

Parameter	Symbol	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	780	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	($\overline{TWE}$, CALE, $\overline{CWE0}$ – $\overline{CWE7}$) (A5 – A17) (CAA3, CAA4, CAB3, CAB4) ($\overline{COE}$)	C_{in}	8 14 26 50	pF
Input/Output Capacitance	(DQ0 – DQ63) (TIO0 – TIO7)	$C_{I/O}$	8 10	pF

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

DATA RAMs READ CYCLE (See Note 1)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time (CAAx, CABx)	t_{AVQV}	—	15	ns	
Latched Address Access Time (A5 – A17)	t_{LAVQV}	—	22	ns	
Latched Address to CALE Low Setup Time	t_{AVCALL}	4	—	ns	
Latched Address to CALE Low Hold Time	t_{CALAX}	3	—	ns	
Enable Access Time	t_{ELQV}	—	15	ns	3
Output Enable Access Time	t_{GLQV}	—	8	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	6
Enable Low to Output Active	t_{ELQX}	4	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	0	8	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	7	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	ns	

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Addresses valid prior to or coincident with $\overline{CS}$ going low.
4. At any given voltage and temperature, t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{COE}$ = V_{IL}).

AC TEST LOADS

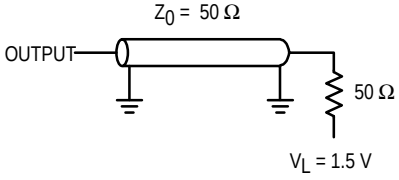


Figure 1A

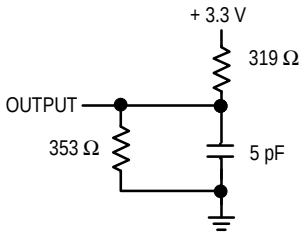
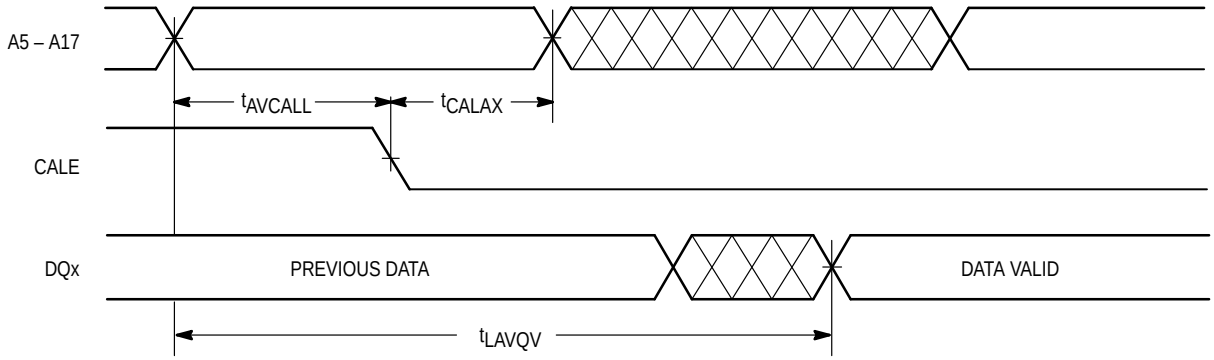


Figure 1B

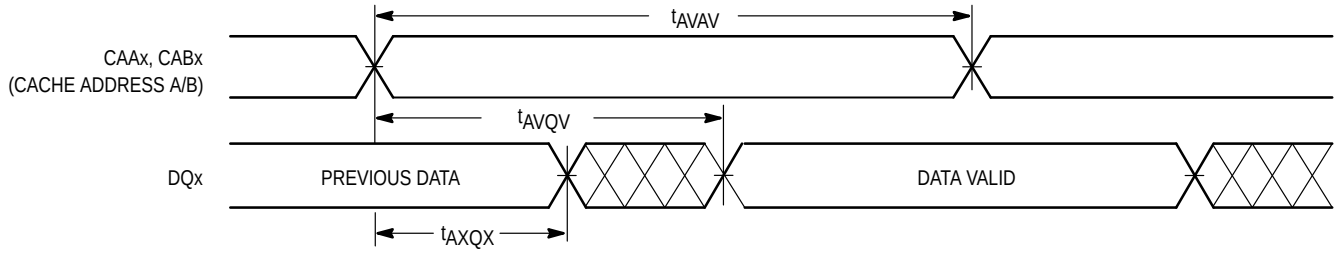
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

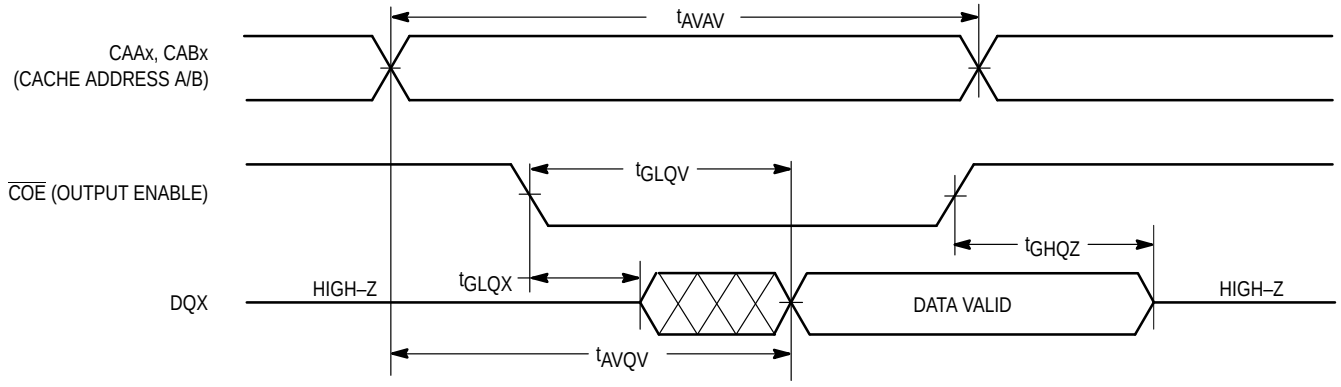
DATA RAMs FIRST ACCESS READ CYCLE (See Note 7)



DATA RAMs BURST ACCESS READ CYCLE (CALE ≤ V_{IL}) (See Note 7)



DATA RAMs READ CYCLE 3 (CALE ≤ V_{IL}) (See Note 3)

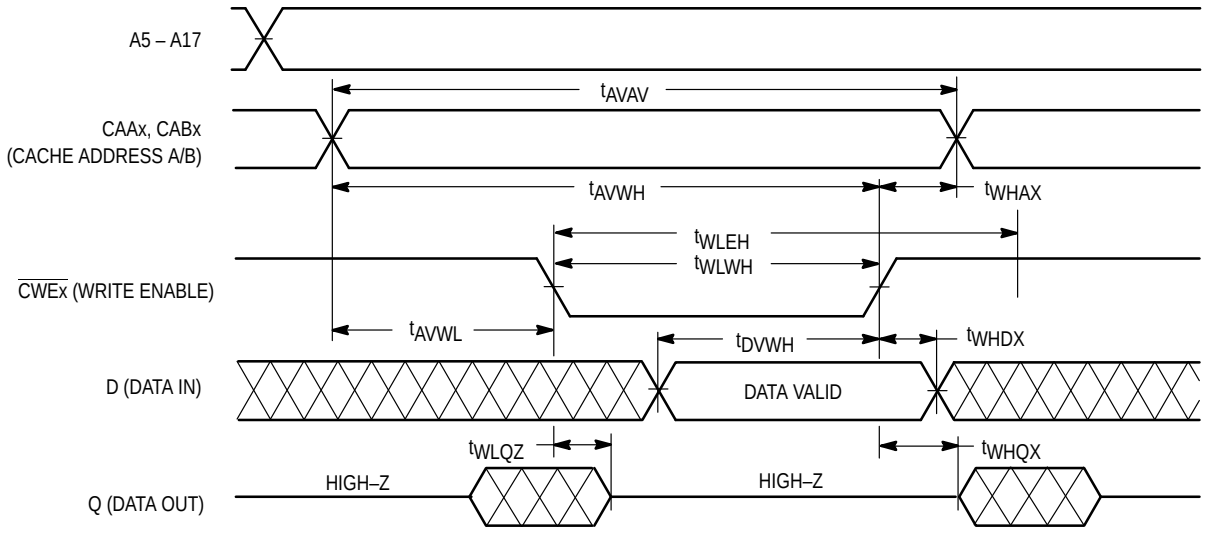


DATA RAMs WRITE CYCLE ($\overline{CWE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	ns	
Write Pulse Width, $\overline{COE}$ High	t_{WLWH}, t_{WLEH}	10	—	ns	4
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	4	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

DATA RAMs WRITE CYCLE (CALE ≥ V_{IH}) ($\overline{CWE}$ Controlled, See Notes 1 and 2)



TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

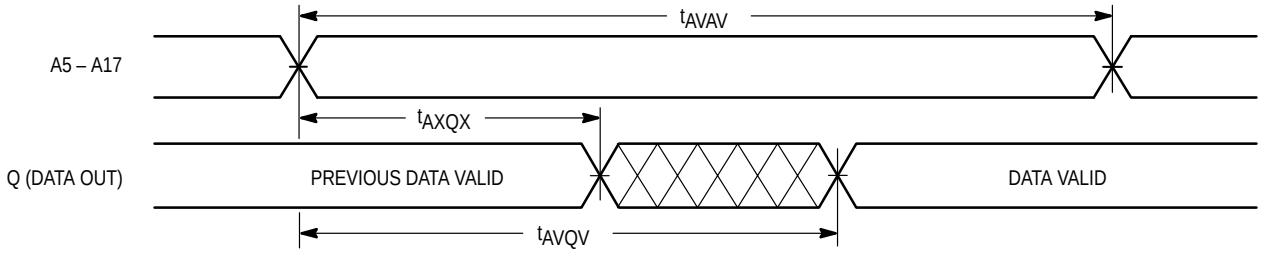
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 and 5)

Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time	t_{AVQV}	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	3, 4

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{COE}$ = V_{IL}).

TAG RAM READ CYCLE (See Note 5)

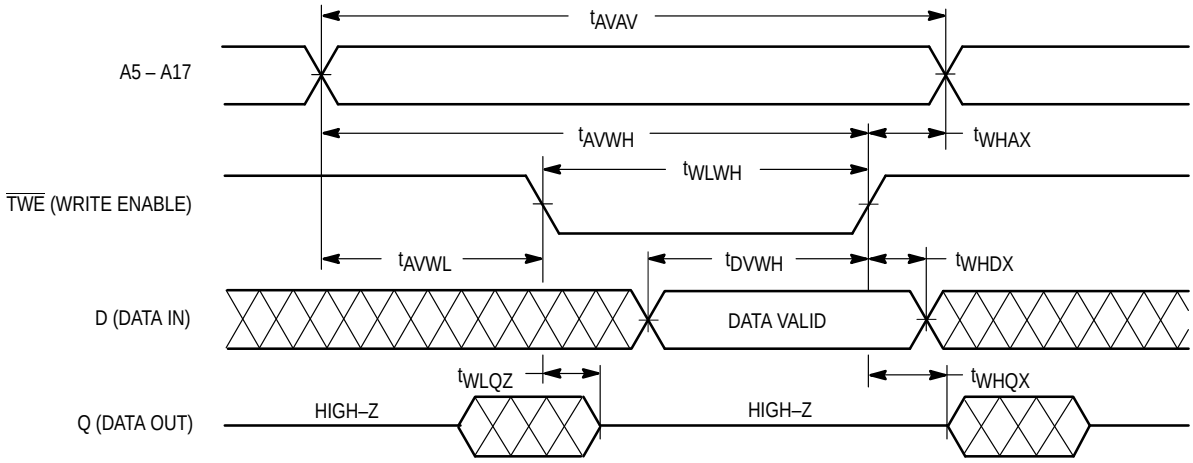


TAG RAM WRITE CYCLE (See Notes 1 and 2)

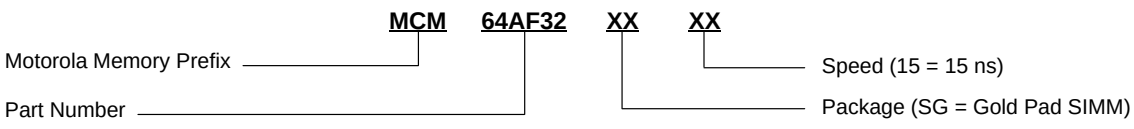
Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	4	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ is low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



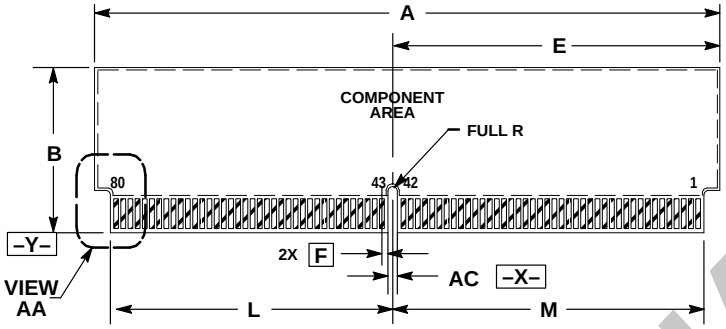
ORDERING INFORMATION
(Order by Full Part Number)



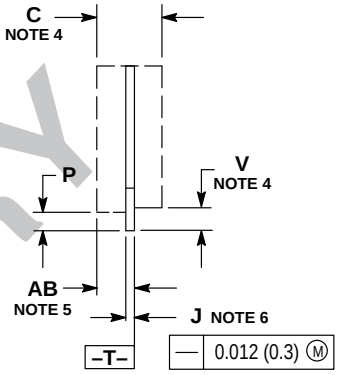
Full Part Number — MCM64AF32SG15

PACKAGE DIMENSIONS

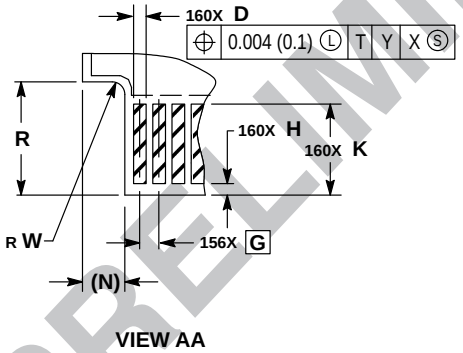
CARD EDGE MODULE
160–LEAD
CASE TBD



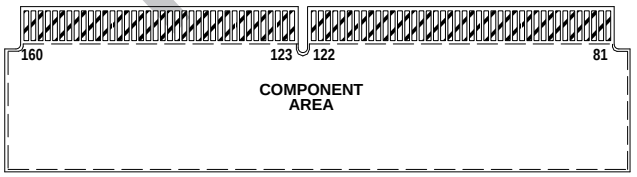
FRONT VIEW



SIDE VIEW



VIEW AA



BACK VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.290	1.310	32.77	33.27
C	—	0.454	—	11.53
D	0.033	0.037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.030	—	0.51
J	0.055	0.069	1.40	1.75
K	0.210	—	5.33	—
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.125	—	3.18	—
R	0.285	0.305	7.24	7.75
V	0.157	—	3.99	—
W	0.040	0.060	1.02	1.52
AB	—	0.262	—	6.66
AC	0.072	0.076	1.83	1.93

Literature Distribution Centers:
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JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.