MCM67D709

128K x 9 Bit Synchronous Dual I/O Fast Static RAM

The MCM67D709 is a 1,179,648 bit synchronous static random access memory organized as 131,072 words of 9 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 128K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers and two sets of output latches. This device has increased output drive capability supported by multiple power pins.

Asynchronous inputs include the processor output enable ($\overline{POE}$) and the system output enable ($\overline{SOE}$).

The address inputs (A0 – A16) are synchronous and are registered on the falling edge of clock (K). Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of clock (K). Writes to the RAM are self–timed.

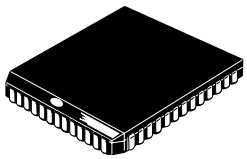
All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three–state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

The MCM67D709's dual I/Os can be used in x9 separate I/O applications. Common I/Os PDQ0 – 7, PDQP and SDQ0 – 7, SDQP can be treated as either inputs (D) or outputs (Q) depending on the state of the control pins. In order to dedicate PDQ0 – 7, PDQP as data (D) inputs and SDQ0 – 7, SDQP as outputs (Q), tie $\overline{SIE}$ and $\overline{POE}$ high. $\overline{SOE}$ becomes the asynchronous $\overline{G}$ for the outputs. $\overline{PIE}$ will need to track $\overline{W}$ for proper write/read operations.

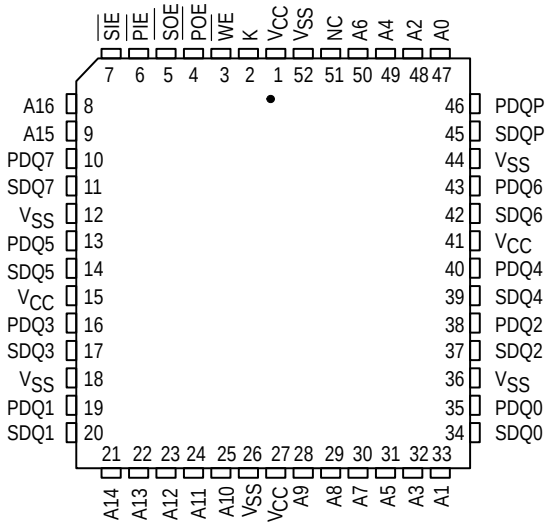
This device is ideally suited for pipelined systems and systems with multiple data buses and multi–processing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 5% Power Supply
- 88110/88410 Compatibility: –16/60 MHz, –20/50 MHz
- Self–Timed Write Cycles
- Clock Controlled Output Latches
- Address and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52 Lead PLCC Package
- Can be used as Separate I/O x9 SRAM



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENTS



PIN NAMES	
A0 – A16	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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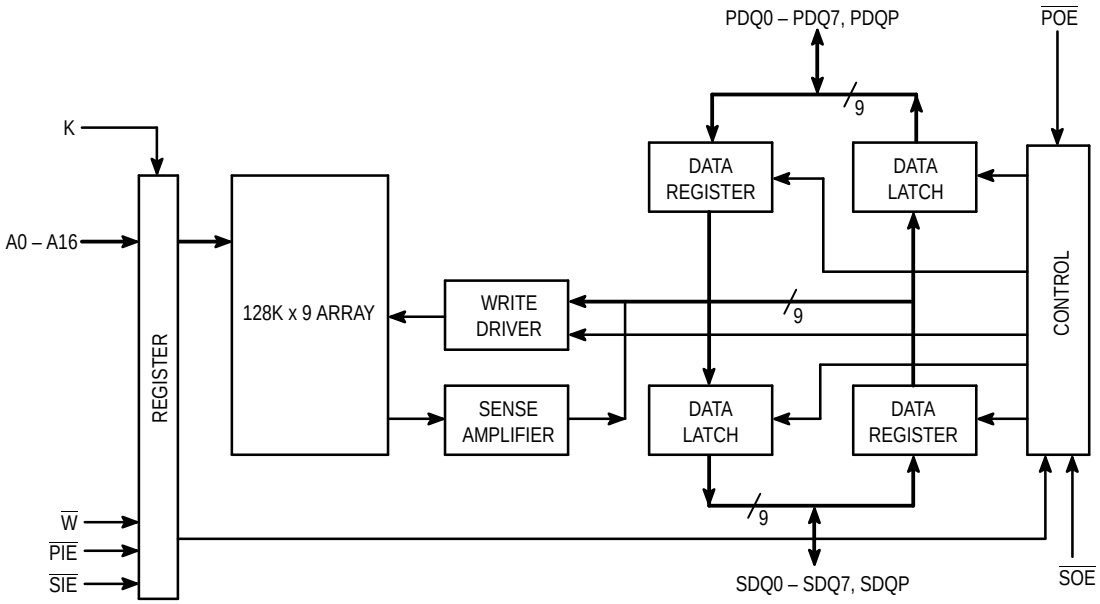
BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High–Z	3
1	1	1	1	0	Read	Copy Back	High–Z	Data Out	3
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	3
1	X	X	1	1	Read	NOP	High–Z	High–Z	
X	0	0	X	X	N/A	NOP	High–Z	High–Z	2, 4
0	0	1	1	1	Write	Processor Write Hit	Data In	High–Z	2, 5
0	1	0	1	1	Write	Allocate	High–Z	Data In	2, 5
0	0	1	1	0	Write	Write Through	Data In	Stream Data	2, 6
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	2, 6
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	2, 6
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	2, 6
0	1	1	X	X	N/A	NOP	High–Z	High–Z	4
X	0	1	0	0	N/A	Invalid	Data In	Stream	2, 7
X	0	1	0	1	N/A	Invalid	Data In	High–Z	2, 7
X	1	0	0	0	N/A	Invalid	Stream	Data In	2, 7
X	1	0	1	0	N/A	Invalid	High–Z	Data In	2, 7

NOTES:

1. A ‘0’ represents an input voltage ≤ V_{IL} and a ‘1’ represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAMs behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don’t care, and the corresponding outputs are High–Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. No RAM cycle is performed.
5. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
6. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
7. Data contention will occur.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM67D709–16: t_{KHKH} = 16 ns MCM67D709–20: t_{KHKH} = 20 ns	I_{CCA}	 — —	 280 260	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	5	6	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Measurement Timing Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	Processor Frequency: 60 MHz MCM67D709–16 Min	60 MHz MCM67D709–16 Max	50 MHz MCM67D709–20 Min	50 MHz MCM67D709–20 Max	Unit	Notes
Read Cycle Time Clock High to Clock High	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock High to Output Valid	t_{KHQV}	—	6	—	7.5	ns	3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	0	—	0	—	ns	
Output Hold from Clock High	t_{KHQX2}	2	—	3	—	ns	3, 4
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WHKH}	2		2			
$\overline{PIE}$	t_{PIEHKH}	2		2			
$\overline{SIE}$	t_{SIEHKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	6	0	8	ns	4
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	2	—	5	—	ns	4
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	4
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. K must be at a high level for outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

AC SPEC LOADS

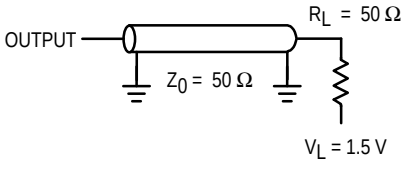


Figure 1A

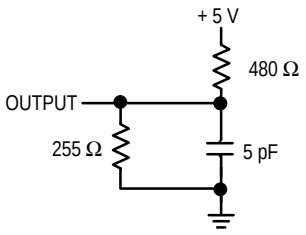
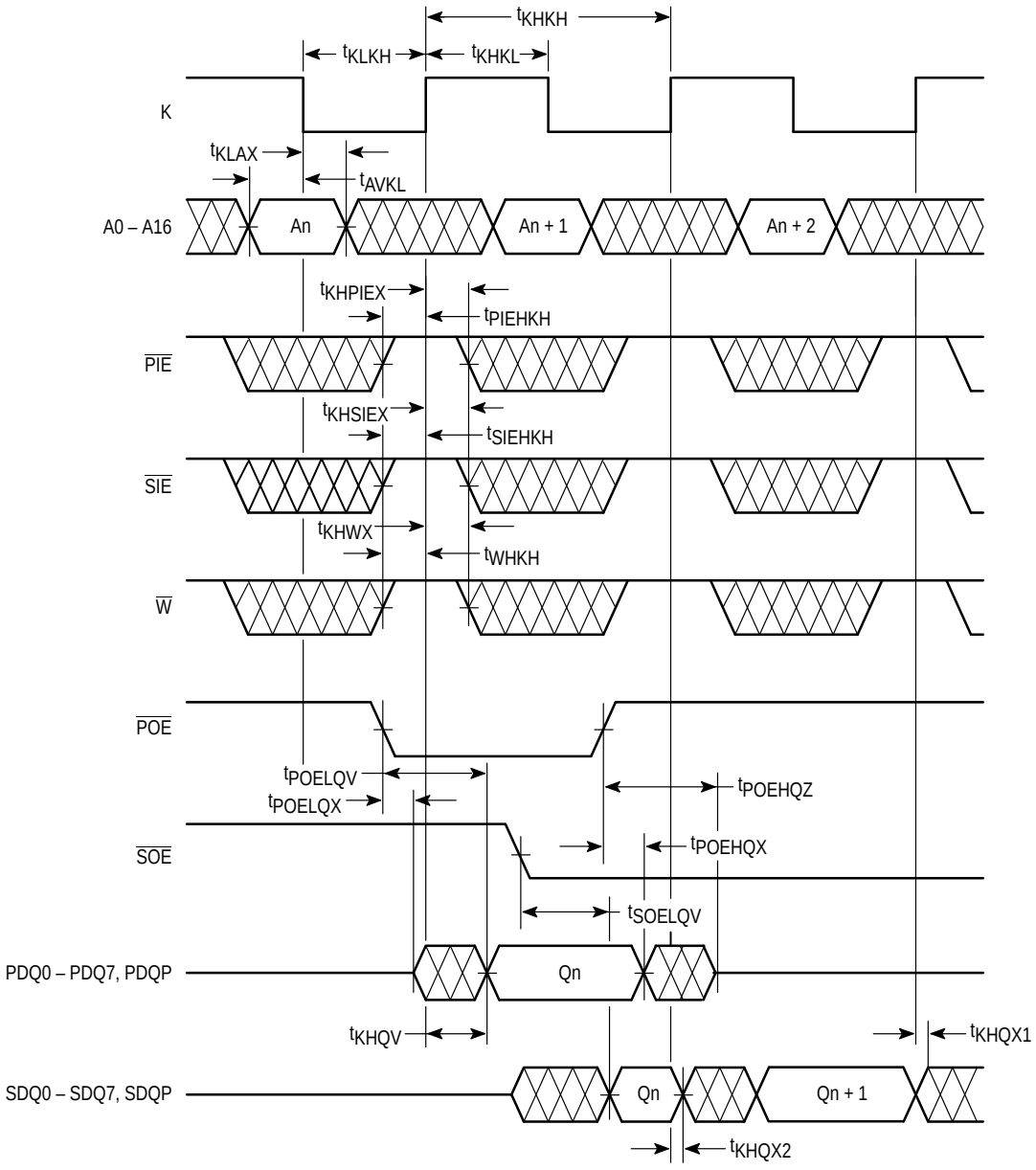


Figure 1B

READ CYCLE (See Note)

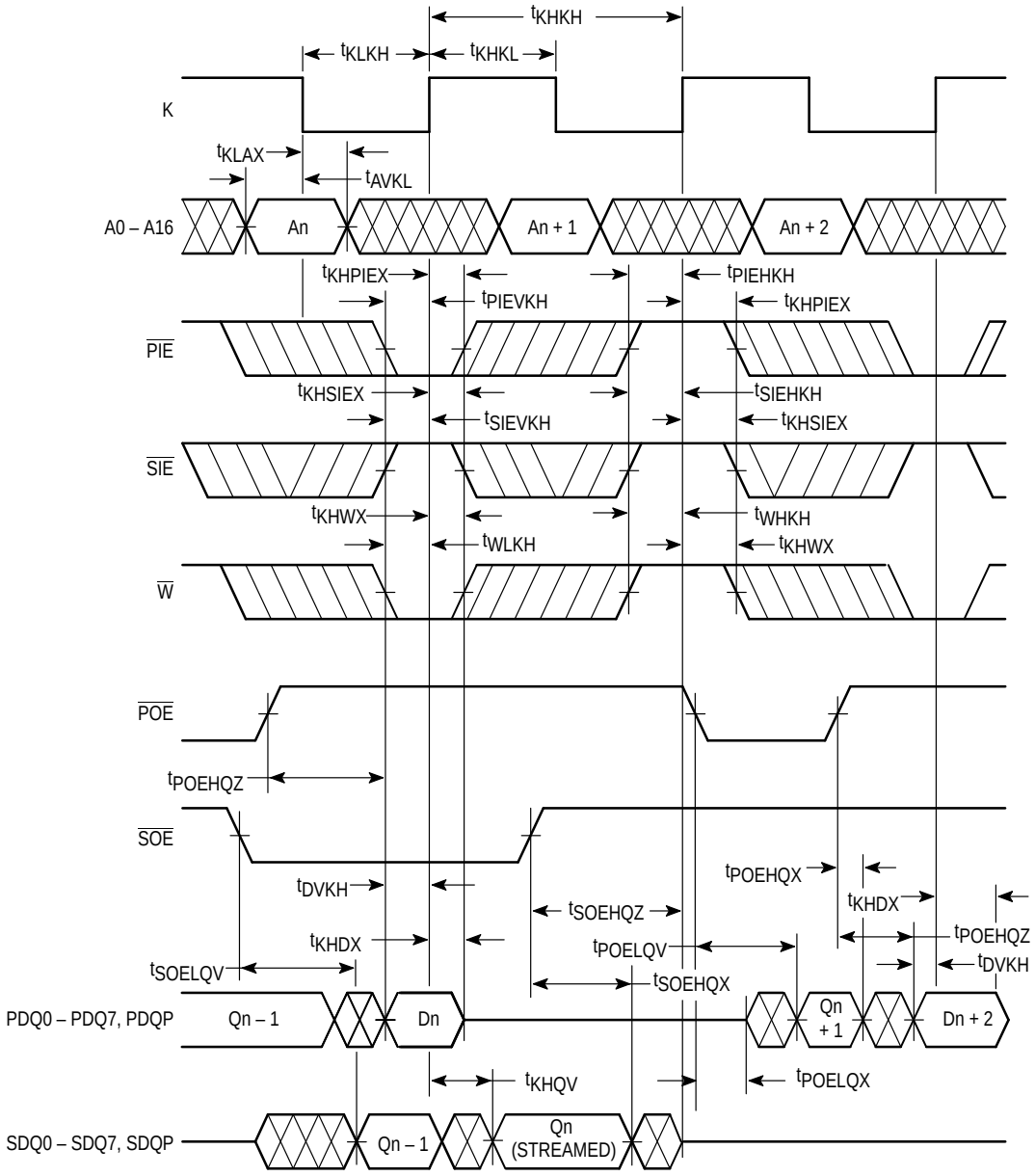


WRITE THROUGH – READ – WRITE (See Note 1)

Parameter	Symbol	Processor Frequency: 60 MHz MCM67D709–16 Min	60 MHz MCM67D709–16 Max	50 MHz MCM67D709–20 Min	50 MHz MCM67D709–20 Max	Unit	Notes
Write Cycle Times	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock High to Output High–Z ($\overline{W}$ = V_{IL} and $\overline{SIE}$ = $\overline{PIE}$ = V_{IH})	t_{KHQZ}	—	8	—	8	ns	3, 4
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WLKH}	2		2			
$\overline{PIE}$	t_{PIEVKH}	2		2			
$\overline{SIE}$	t_{SIEVKH}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}	2		2			
Write with Streaming ($\overline{PIE}$ = $\overline{SOE}$ = V_{IL} or $\overline{SIE}$ = $\overline{POE}$ = V_{IL}) Clock High to Output Valid	t_{KHQV}	—	5	—	7	ns	5
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	6	0	8	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	2	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A write is performed with $\overline{W}$ = V_{IL} for the specified setup and hold times and either $\overline{PIE}$ = V_{IL} or $\overline{SIE}$ = V_{IL}. If both $\overline{PIE}$ = V_{IL} and $\overline{SIE}$ = V_{IL} or $\overline{PIE}$ = V_{IH} and $\overline{SIE}$ = V_{IH}, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE

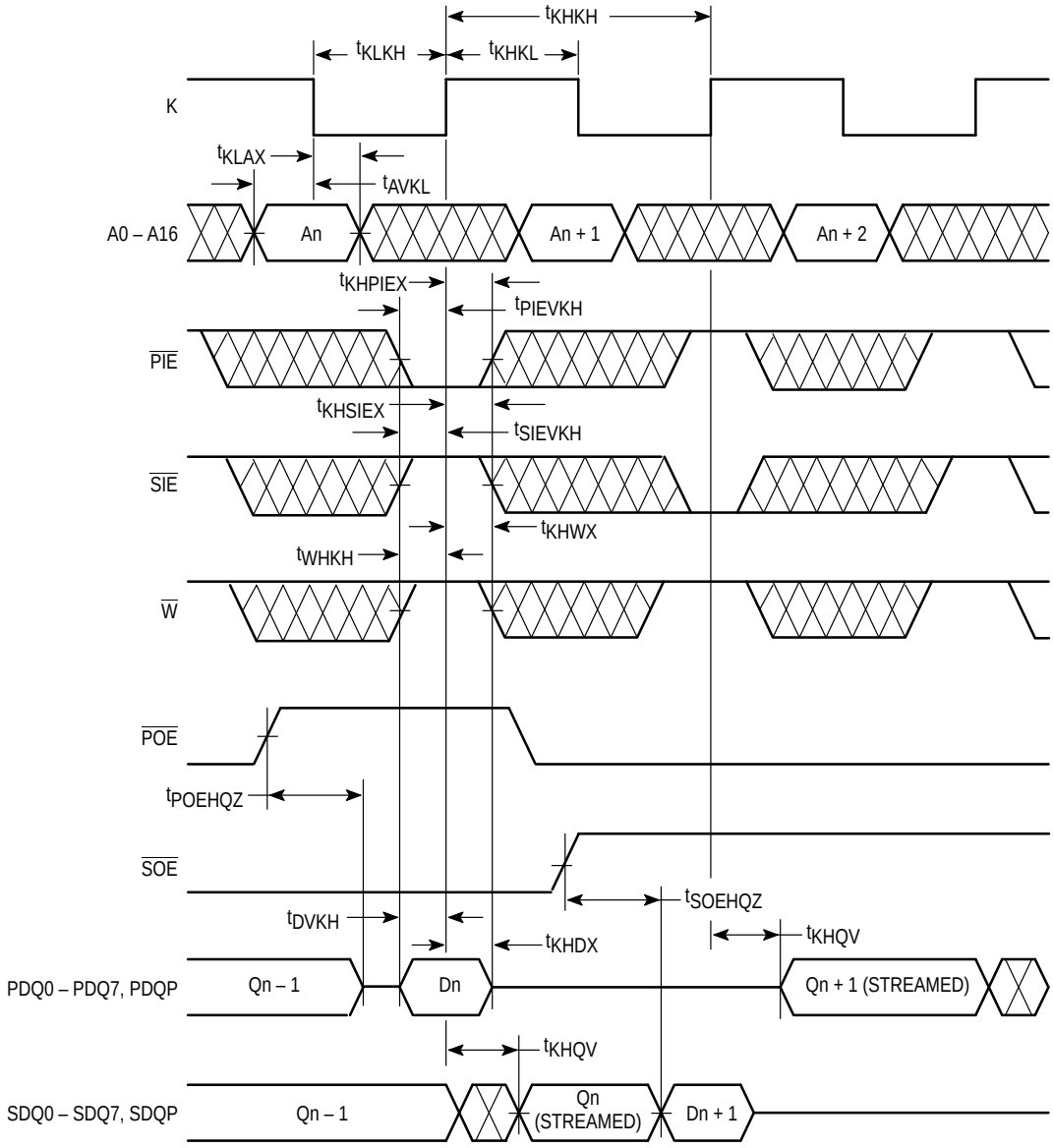


STREAM CYCLE (See Note 1)

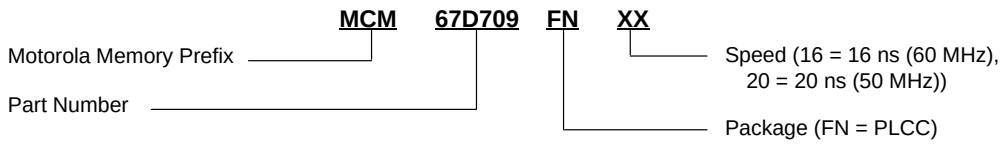
Processor Frequency		60 MHz		50 MHz			
		MCM67D709–16		MCM67D709–20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Stream Cycle Time	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	6	—	7	ns	
Setup Times: A $\overline{W}$ $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	 t_{AVKL} t_{WHKH} t_{PIEVKH} t_{SIEVKH} t_{DVKH}	 2 2 2 2 2	—	 2 2 2 2 2	—	ns	
Hold Times: A $\overline{W}$ $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	 t_{KLAX} t_{KHWX} t_{KHPIEX} t_{KHSIEX} t_{KHDX}	 2 2 2 2 2	—	 2 2 2 2 2	—	ns	
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	6	0	8	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, for a given device.

STREAM CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67D709FN16 MCM67D709FN20

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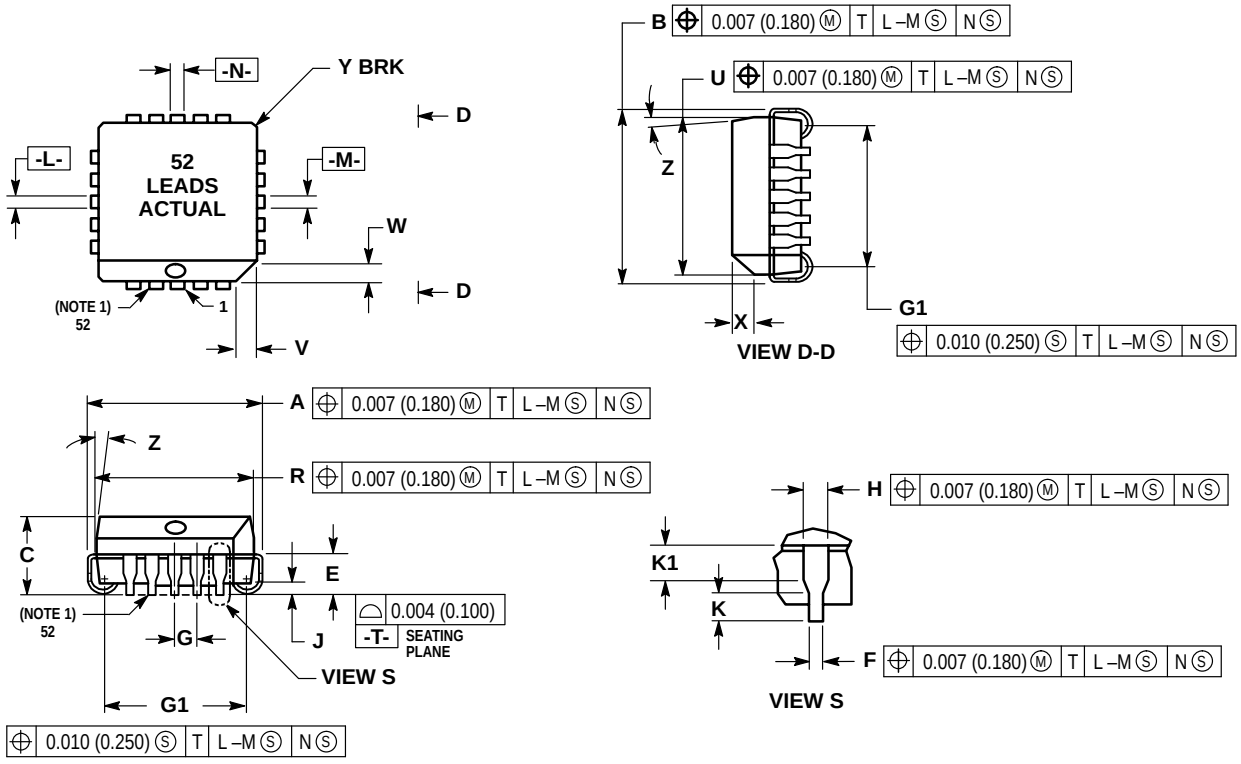
PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02



NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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