

# Advance Information

## 1M x 8 Bit

### Fast Static RAM Module

The MCM8A10 is an 8M bit static random access memory module organized as 1,048,576 words of 8 bits. The module is offered in a 72-lead single in-line memory module (SIMM). Eight MCM6227B fast static RAMs, packaged in 28-lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6227B is organized as 1,048,576 words of 1 bit. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM8A10 is equipped with a chip enable (E) and eight separate write enable (W0 – W7) inputs, allowing for greater system flexibility.

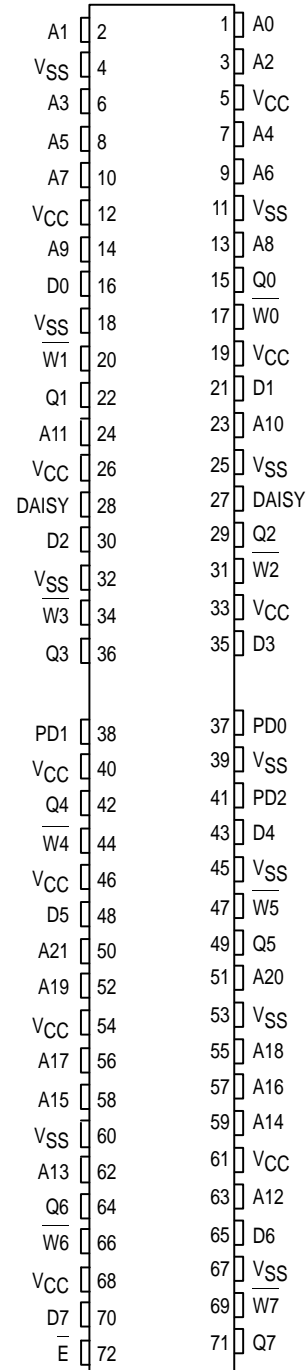
- Single 5 V ± 5% Power Supply
- Fast Access Times: 15 ns
- Three-State Outputs
- Fully TTL Compatible
- High Board Density SIMM Package
- Bit Operation: Eight Separate Write Enables, One for Each Bit
- High Quality Six-Layer FR4 PWB with Separate Internal Power and Ground Planes

PIN NAMES	
A0 – A19	Address Inputs
W0 – W7	Write Enables
E	Chip Enable
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
PD0 – PD2	Package Density
DAISY	Pins Single Net
VCC	+ 5 V Power Supply
VSS	Ground

For proper operation of the device, VSS must be connected to ground.

## MCM8A10

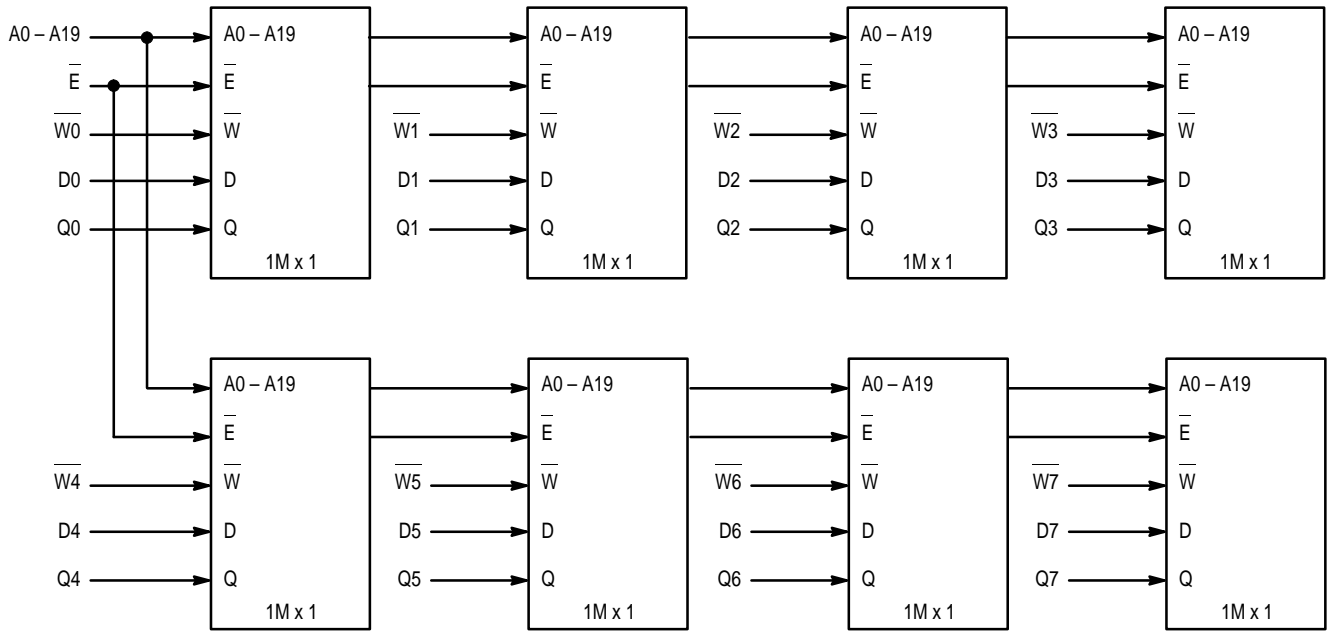
### PIN ASSIGNMENT TOP VIEW 72-LEAD SIMM – CASE TBD



This document contains information on a new product. Specifications and information herein are subject to change without notice.

10/30/96

**FUNCTIONAL BLOCK DIAGRAM  
1M x 8 MEMORY MODULE**



PD0 — Open  
 PD1 —  $V_{SS}$   
 PD2 — Open

## TRUTH TABLE

E	W	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	Read	D <sub>out</sub>	Read	I <sub>CCA</sub>
L	L	Write	High-Z	Write	I <sub>CCA</sub>

NOTE: H = High, L = Low, X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to 7.0	V
Voltage Relative to V <sub>SS</sub> for Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Output Current	I <sub>out</sub>	± 20	mA
Power Dissipation	P <sub>D</sub>	8.8	W
Temperature Under Bias	T <sub>bias</sub>	-10 to +85	°C
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 5%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.75	5.25	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.5*	0.8	V

\* V<sub>IL</sub> (min) = -0.5 V dc; V<sub>IL</sub> (min) = -2.0 V ac (pulse width ≤ 20 ns).

\*\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V ac (pulse width ≤ 20 ns).

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(I)</sub>	—	± 1	μA
Output Leakage Current (E = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(O)</sub>	—	± 1	μA
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>CC</sub> = max)	I <sub>CCA</sub>	—	920	mA
AC Standby Current (V <sub>CC</sub> = max, E = V <sub>IH</sub> , f ≤ f <sub>max</sub> )	I <sub>SB1</sub>	—	320	mA
CMOS Standby Current (E ≥ V <sub>CC</sub> - 0.2 V, V <sub>in</sub> ≤ V <sub>SS</sub> + 0.2 V or ≥ V <sub>CC</sub> - 0.2 V, V <sub>CC</sub> = max, f = 0 MHz)	I <sub>SB2</sub>	—	40	mA
Output Low Voltage (I <sub>OL</sub> = +8.0 mA)	V <sub>OL</sub>	—	0.4	V
Output High Voltage (I <sub>OH</sub> = -4.0 mA)	V <sub>OH</sub>	2.4	—	V

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, T<sub>A</sub> = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit	
Input Capacitance	Address Inputs E W	C <sub>in</sub>	42	58	pF
			50	74	
			10	13	
Input and Output Capacitance	D, Q	C <sub>in</sub> , C <sub>out</sub>	10	13	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V	Output Timing Measurement Reference Level ..... 1.5 V
Input Rise/Fall Time ..... 2 ns	Output Load ..... See Figure 1a
Input Timing Measurement Reference Level ..... 1.5 V	

### READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Read Cycle Time	$t_{AVAV}$	15	—	ns	2, 3
Address Access Time	$t_{AVQV}$	—	15	ns	
Enable Access Time	$t_{ELQV}$	—	15	ns	4
Output Hold from Address Change	$t_{AXQX}$	5	—	ns	
Enable Low to Output Active	$t_{ELQX}$	5	—	ns	5, 6, 7
Enable High to Output High-Z	$t_{EHQZ}$	0	6	ns	5, 6, 7

#### NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with E going low.
5. At any given voltage and temperature,  $t_{EHQZ}$  max is less than  $t_{ELQX}$  min, both for a given device and from device to device.
6. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ( $E \leq V_{IL}$ ).

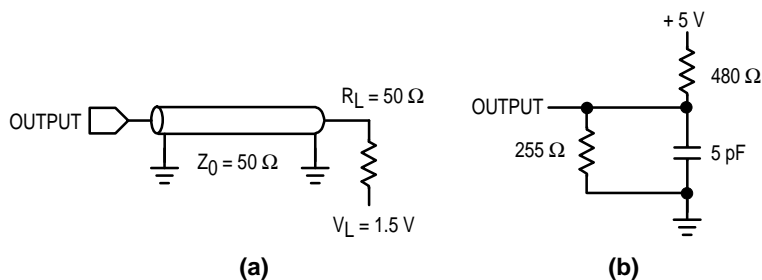
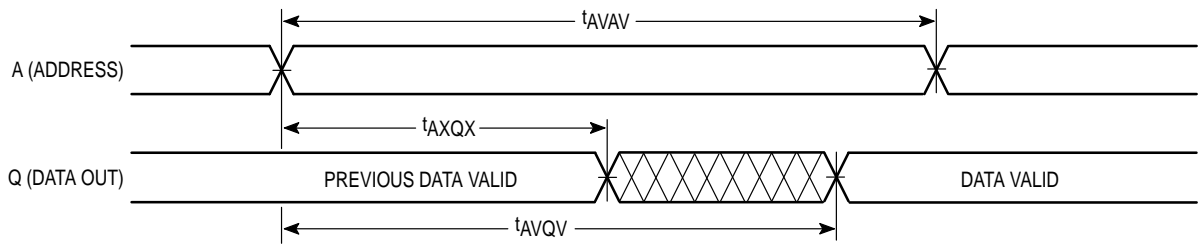


Figure 1. AC Test Loads

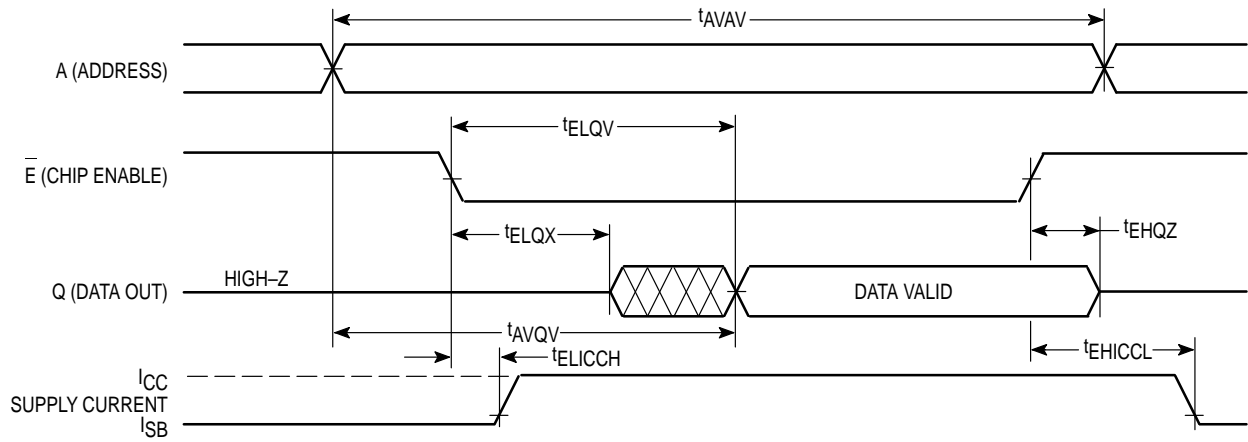
### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Notes 1, 2, and 8)



**READ CYCLE 2** (See Note 4)



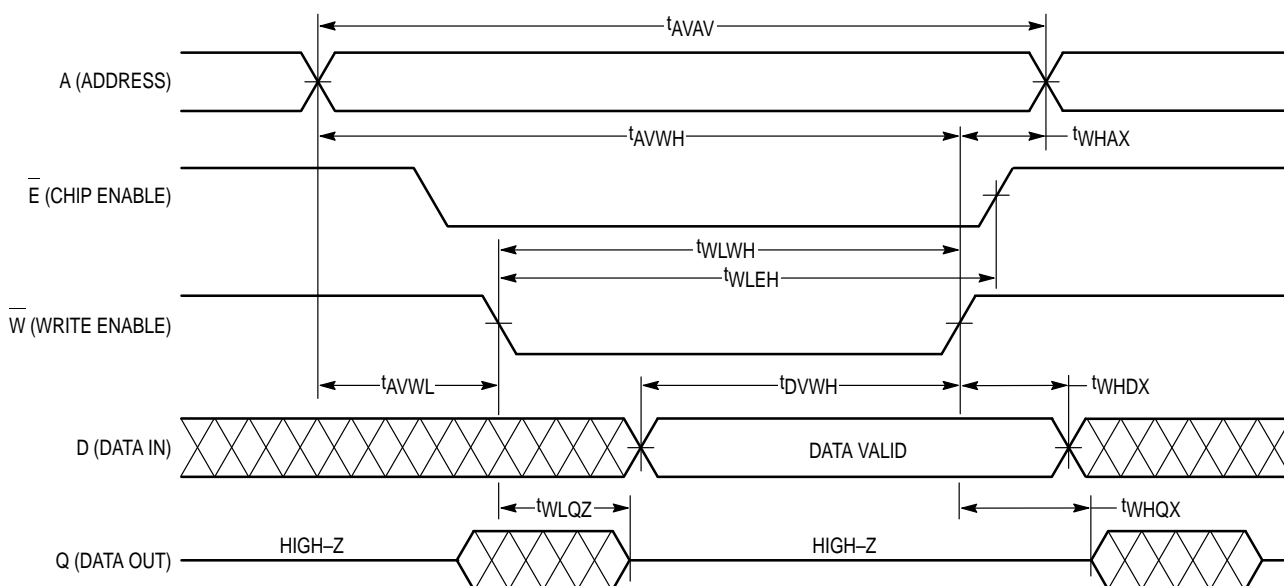
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	ns	3
Address Setup Time	$t_{AVWL}$	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	12	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	12	—	ns	
Data Valid to End of Write	$t_{DVWH}$	7	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	6	ns	4, 5, 6
Write High to Output Active	$t_{WHQX}$	5	—	ns	4, 5, 6
Write Recovery Time	$t_{WHAX}$	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

**WRITE CYCLE 1** ( $\overline{W}$  Controlled See Notes 1 and 2)



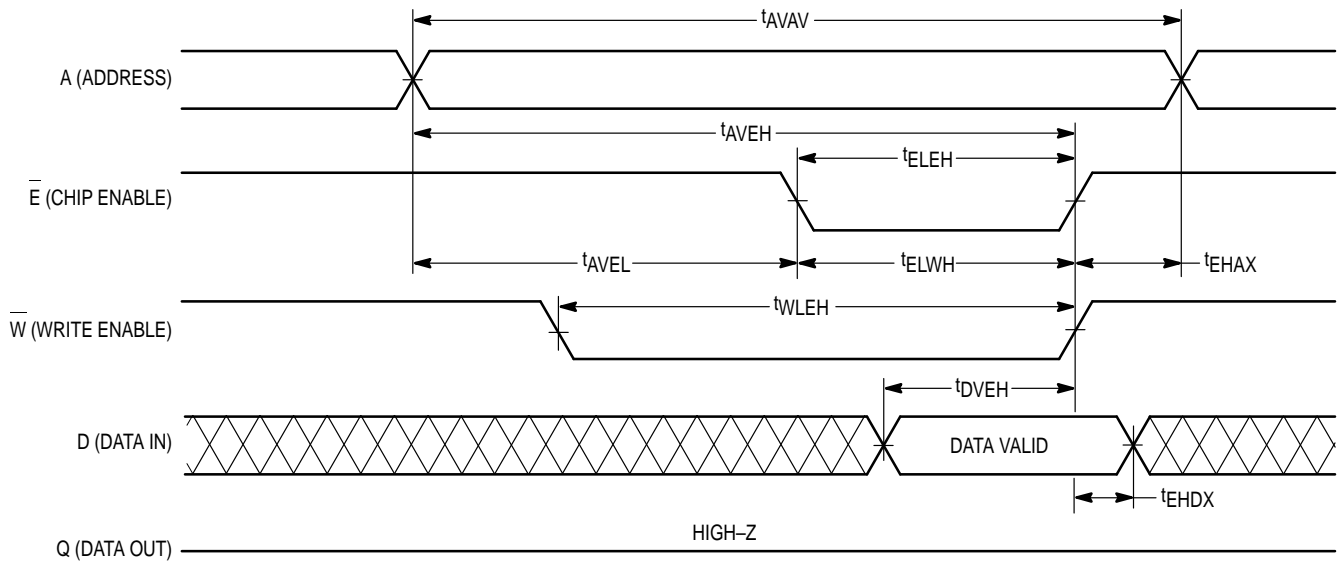
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	ns	3
Address Setup Time	$t_{AVEL}$	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	12	—	ns	
Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	10	—	ns	4, 5
Write Pulse Width	$t_{WLEH}$	12	—	ns	
Data Valid to End of Write	$t_{DVEH}$	7	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	ns	

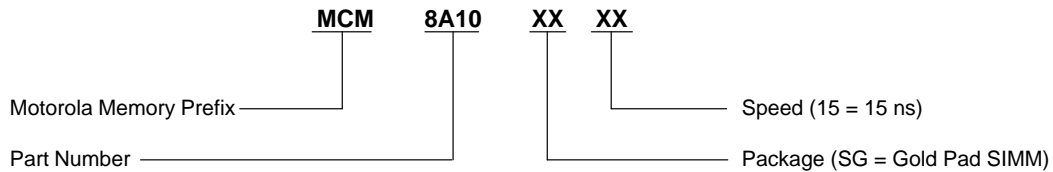
NOTES:

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
5. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance state.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled See Notes 1 and 2)



**ORDERING INFORMATION**  
(Order by Full Part Number)




Full Part Number — MCM8A10SG15

## PACKAGE DIMENSIONS

72-LEAD SIMM

CASE TBD

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MCM8A10/D

