

**8/16-bit Data Bus**  
**Static RAM Card**

Connector Type

**Two-piece 68-pin**

- MF365A-LYCATXX**
- MF3129-LYCATXX**
- MF3257-LYCATXX**
- MF3513-LYCATXX**
- MF31M1-LYCATXX**
- MF32M1-LYCATXX**
- MF34M1-LYCATXX**

**1. DESCRIPTION**

Mitsubishi's Static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm×54mm×3.3mm). The cards use a 8/16 bit data-bus.

Available in 64KB, 128KB, 256KB, 512KB, 1 MB, 2 MB and 4 MB capacities, Mitsubishi's SRAM cards conform to the PC Card Standard. Mitsubishi achieved high density memory, while maintaining credit size by using a thin small outline packaging technology (TSOP). The TSOP surpasses conventional memory card chip-on-board packaging technology where larger, surface-mount devices result in a tradeoff between card size and optimum memory density. The TSOP, with external leads spaced on 20-mil centers, is over four times smaller than standard equivalent pin count surface-mount packages. This allows up to 8 memory ICs (plus interface circuitry) to be mounted in a card that in only 3.3mm thick.

**4. PRODUCT LIST**

Type name	Item	Memory capacity	Data Bus width(bits)	Attribute memory	Auxiliary battery
MF365A-LYCATXX		64KB	8/16	NO	NO
MF3129-LYCATXX		128KB			
MF3257-LYCATXX		256KB			
MF3513-LYCATXX		512KB			
MF31M1-LYCATXX		1MB			
MF32M1-LYCATXX		2MB			
MF34M1-LYCATXX		4MB			

**2. FEATURES**

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size
- Electrostatic discharge protection to 15kV
- Buffered interface
- Write protect switch
- 68pin

**3. APPLICATIONS**

- Office automation
- Computers
- Telecommunications
- Data Communication
- Industrial
- Consumer



## 5. SUMMARY

MF3XXX-LYCATXX series is the Static RAM cards which has 8/16 bit changeable data-bus width. The card has a replaceable lithium battery to maintain data in memory. When the card is not use or the supply voltage drops, the battery will automatically maintain data in memory.

## 6. FUNCTIONAL DESCRIPTION

The function of the card is determined by the combination of the following five control signals, REG#, CE1#, CE2#, OE#, WE#; active low signals. (Please refer to section 10 FUNCTION TABLE on page 5)

### (1)COMMON MEMORY FUNCTION

When REG# signal is high level, the common memory area is selected.

#### (a)READ MODE

To read, WE# is set high level and CE1# or CE2# is set low level and the memory address is applied at inputs A0-A21(4MB). Setting OE# low level executes the reading with output at data-bus. It is available to make the following functions according to the combination of CE1# and CE2#.

When CE1# is set low level and CE2# is set high level, the card operates as an 8 bit data-bus width card. The data can be dealt with lower data-bus(D0-D7).

When both CE1# and CE2# are set low level, the card operates as a 16 bit data-bus width card.

At this mode LSB of address-bus (A0) is ignored.

In addition odd byte can be accessed through upper data-bus(D8-D15) when CE1# is set high level and CE2# is set low level. This mode is useful when handling only odd bytes in the 16 bit data-bus interface system (A0 is ignored).

When both CE1# and CE2# are set high level, the card becomes a standby mode where the card consumes low power and the data-bus is placed in high impedance state (above functions of CE1# and CE2# are the same as in the following modes).

When both OE# and WE# are set high level, the card becomes a output disable mode and the data-bus is placed in high impedance state.

#### (b)WRITE MODE

To write, the memory address is first applied at inputs A0-A21(4MB) and the data is applied at output pins. Setting CE1# or CE2# low level, WE# low level and OE# high level executes the writing.

### (2)ATTRIBUTE MEMORY FUNCTION

When REG# is set low level, the attribute memory area is selected. MF3XXX-LYCATXX series have no attribute memory, but outputs FFh on the lower data-bus(D0-D7) when the following conditions are applied

(a)setting CE1# low, CE2# high, OE# low, WE# high and A0 low

(b)setting CE1# low, CE2# low, OE# low and WE# high

## 7. WRITE PROTECT MODE

When the write protect switch is switched on, this card goes into a write protect mode that can read but not write data. In this mode, WP pin becomes "H" level.

At the shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin indicates "L" level).

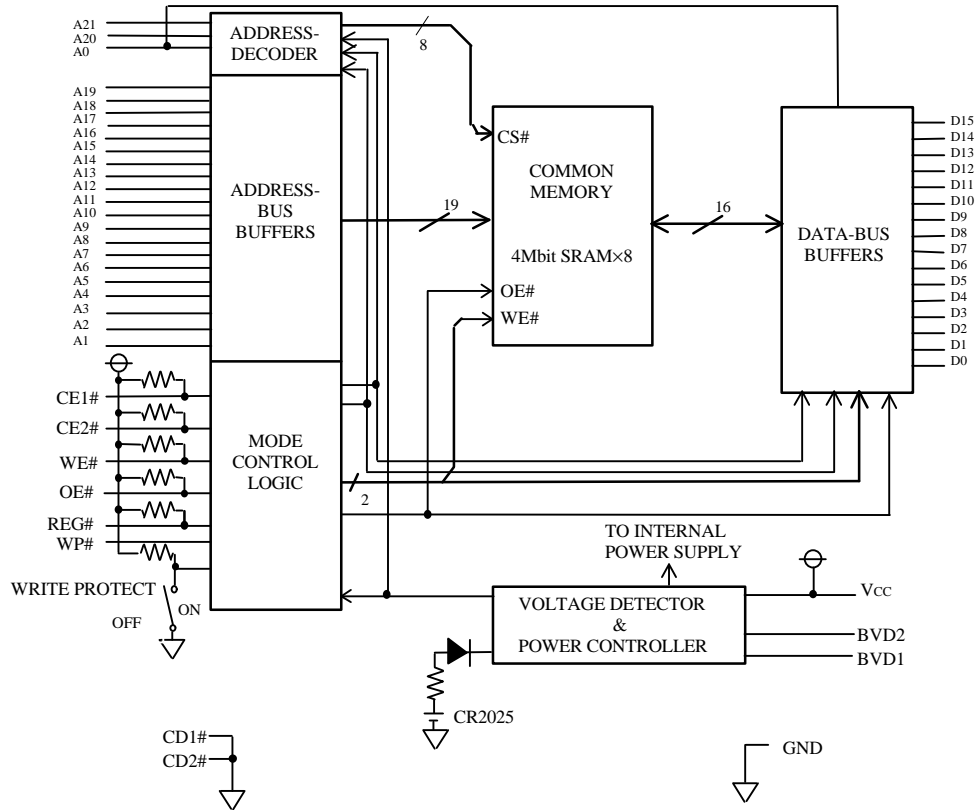


8. PIN ASSIGNMENTS

Pin No.	Symbol	Function	Pin No.	Symbol	Function	
1	GND	Ground	35	GND	Ground	
2	D3	} Data I/O	36	CD1#	Card detect 1	
3	D4		37	D11	} Data I/O	
4	D5		38	D12		
5	D6		39	D13		
6	D7		40	D14		
7	CE1#	Card enable 1	41	D15		} Card enable 2
8	A10	Address input	42	CE2#		
9	OE#	Output enable	43	NC	} No connection	
10	A11	} Address input	44	NC		
11	A9		45	NC		
12	A8		46	A17	} Address input	
13	A13		47	A18		A17 (NC for ≤ 128KB types)
14	A14	48	A19	A18 (NC for ≤ 256KB types)		
15	WE#	Write enable	49	A20		A19 (NC for ≤ 512KB types)
16	NC	No connection	50	A21		A20 (NC for ≤ 1MB type)
17	VCC	Power supply voltage	51	VCC	A21 (NC for ≤ 2MB type)	
18	NC	No connection	52	NC	Power supply voltage	
19	A16	} Address input	53	NC	} No connection	
20	A15		A16 (NC for 64KB type)	54		NC
21	A12		55	NC		
22	A7		56	NC		
23	A6		57	NC		
24	A5		58	NC		
25	A4		59	NC		
26	A3		60	NC		
27	A2		61	REG#		Attribute memory select
28	A1		62	BVD2		Battery voltage detect 2
29	A0	63	BVD1	Battery voltage detect 1		
30	D0	} Data I/O	64	D8	} Data I/O	
31	D1		65	D9		
32	D2		66	D10		
33	WP	Write protect	67	CD2#		Card detect 2
34	GND	Ground	68	GND	Ground	



9. BLOCK DIAGRAM (4MB) (MF34M1-LYCATXX)



10. FUNCTION TABLE

Mode	REG#	CE1#	CE2#	OE#	WE#	A0	I/O (D15~D8)	I/O (D7~D0)	Icc
Standby	X	H	H	X	X	X	High-impedance	High-impedance	standby
Read A (16bit) common	H	L	L	L	H	X	Odd Byte Data out	Even Byte Data out	Active
Write A (16bit) common	H	L	L	H	L	X	Odd Byte Data in	Even Byte Data in	Active
Read B (8bit) common	H	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	H	L	H	L	H	H	High-impedance	Odd Byte Data out	Active
Write B (8bit) common	H	L	H	H	L	L	High-impedance	Even Byte Data in	Active
	H	L	H	H	L	H	High-impedance	Odd Byte Data in	Active
Read C (8bit) common	H	H	L	L	H	X	Odd Byte Data out	High-impedance	Active
Write C (8bit) common	H	H	L	H	L	X	Odd Byte Data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16bit) attribute	L	L	L	L	H	X	Data out (unknown)	Data out (FFh)	Active
Read B (8bit) attribute	L	L	H	L	H	L	High-impedance	Data out (FFh)	Active
	L	L	H	L	H	H	High-impedance	Data out (unknown)	Active
Read C (8bit) attribute	L	H	L	L	H	X	Data out (unknown)	High-impedance	Active

Note 1 : H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=V<sub>IH</sub> or V<sub>IL</sub>

11. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-0.3~6.0	V
V <sub>I</sub>	Input voltage		-0.3~V <sub>cc</sub> +0.3	V
V <sub>O</sub>	Output voltage		0~V <sub>cc</sub>	V
T <sub>opr1</sub>	Operating temperature 1	Read, Write Operation	0~60	°C
T <sub>opr2</sub>	Operating temperature 2	Data retention	0~60	°C
T <sub>stg</sub>	Storage temperature	Excludes data retention	-20~70	°C

12. RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>cc</sub>	V <sub>cc</sub> Supply voltage	4.50	5.0	5.25	V
GND	System ground		0		V
V <sub>IH</sub>	High input voltage	3.5		V <sub>cc</sub>	V
V <sub>IL</sub>	Low input voltage	0		0.8	V



STATIC RAM CARDS

13. ELECTRICAL CHARACTERISTICS (Ta=0~55°C, Vcc=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit	
				Min.	Typ.	Max.		
VOH	High output voltage	IOH= -1.0mA		2.4			V	
VOL	Low output voltage	IOL=2mA				0.4	V	
IiH	High input current	Vi=Vcc V				10	µA	
IiL	Low input current	Vi=0V	CE1#, CE2#, WE#, OE#, REG# Other inputs	-10		-70 -10	µA	
IOZH	High output current in off state	CE1#=CE2#=VIH or OE#=VIH WE#=VIH, Vo=Vcc				10	µA	
IOZL	Low output current in off state	CE1#=CE2#=VIH or OE#=VIH WE#=VIH, Vo=0V				-10	µA	
Icc 1 • 1	Active supply current 1	CE1#=CE2#=VIL, Other inputs= VIH or VIL Outputs=open	64KB~	16bit			170	mA
			512KB	8bit			115	
			1MB~	16bit			230	
			4MB	8bit			155	
Icc 1 • 2	Active supply current 2	CE1#=CE2# ≤ 0.2V Other inputs ≤ 0.2V or ≥ Vcc-0.2V Outputs=open	64KB~	16bit			160	mA
			512KB	8bit			110	
			1MB~	16bit			220	
			4MB	8bit			150	
Icc 2 • 1	Standby supply current 1	CE1#=CE2#=VIH Other inputs=VIH or VIL	64KB~4MB				10	mA
Icc 2 • 2	Standby supply current 2	CE1#=CE2# ≥ Vcc-0.2V Other inputs ≤ 0.2V or ≥ Vcc-0.2V	64KB~512KB			0.15	0.45	mA
			1MB~4MB			0.30	0.65	
VBDET1	Battery detect reference voltage	Vcc=5V, Ta=25°C		2.27	2.37	2.47	V	
VBDET2	Battery detect reference voltage	Vcc=5V, Ta=25°C		2.55	2.65	2.75	V	

Note 2 : Currents flowing into the card are taken as positive (unsigned).

3 : Typical values are measured at Vcc=5V, Ta=25°C.

14. CAPACITANCE

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
CI	Input capacitance	Vi=GND, vi=25mVrms f=1MHz, Ta=25°C				30	pF
CO	Output Capacitance	Vo=GND, vo=25mVrms f=1MHz, Ta=25°C				20	pF

Note 4 : These parameters are not 100% tested.

**15. SWITCHING CHARACTERISTICS**

**Read Cycle** (Ta=0~55°C, Vcc=4.5~5.25V, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcR	Read cycle time	150		ns
ta(A)	Address access time		150	ns
ta(CE)	Card enable access time		150	ns
ta(OE)	Output enable access time		75	ns
tdis(CE)	Output disable time (from CE#)		75	ns
tdis(OE)	Output disable time (from OE#)		75	ns
ten(CE)	Output enable time (from CE#)	5		ns
ten(OE)	Output enable time (from OE#)	5		ns
tv(A)	Data valid time (after address change)	0		ns

**16. TIMING REQUIREMENTS**

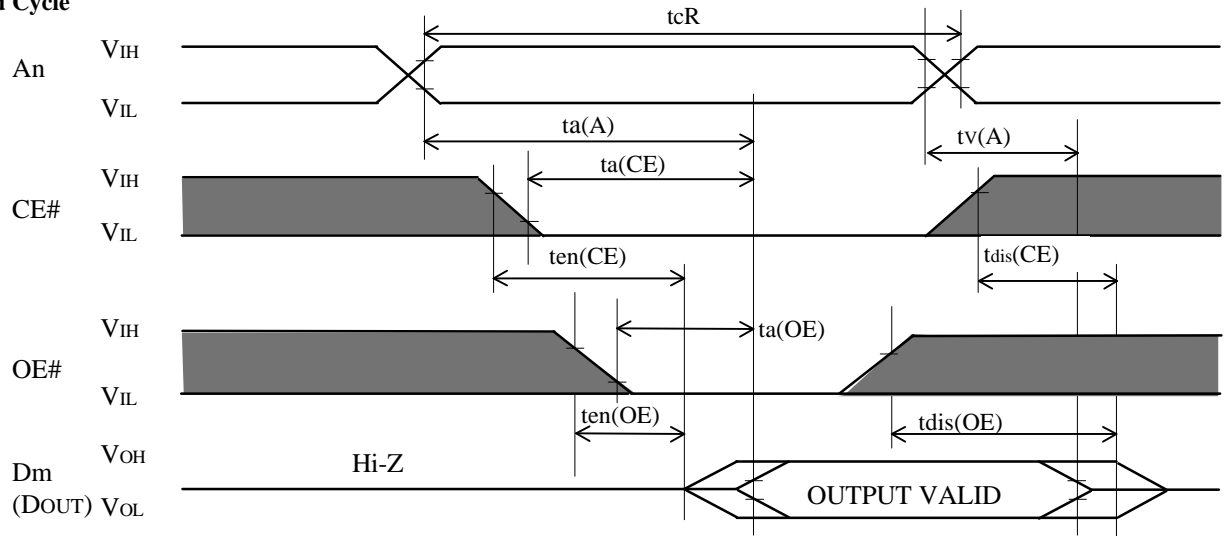
**Write Cycle** (Ta=0~55°C, Vcc=4.5~5.25V, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcW	Write cycle time	150		ns
tw(WE)	Write pulse width	80		ns
tsu(A)	Address set up time	20		ns
tsu(A-WEH)	Address set up time with respect to WE# high	100		ns
tsu(CE-WEH)	Card enable set up time with respect to WE# high	100		ns
t(D-WEH)	Data set up time with respect to WE# high	50		ns
th(D)	Data hold time	20		ns
trec(WE)	Write recovery time	20		ns
tdis(WE)	Output disable time (from WE#)		75	ns
tdis(OE)	Output disable time (from OE#)		75	ns
ten(WE)	Output enable time (from WE#)	5		ns
ten(OE)	Output enable time (from OE#)	5		ns
tsu(OE-WE)	OE# set up time with respect to WE# low	10		ns
th(OE-WE)	OE# hold time with respect to WE# high	10		ns



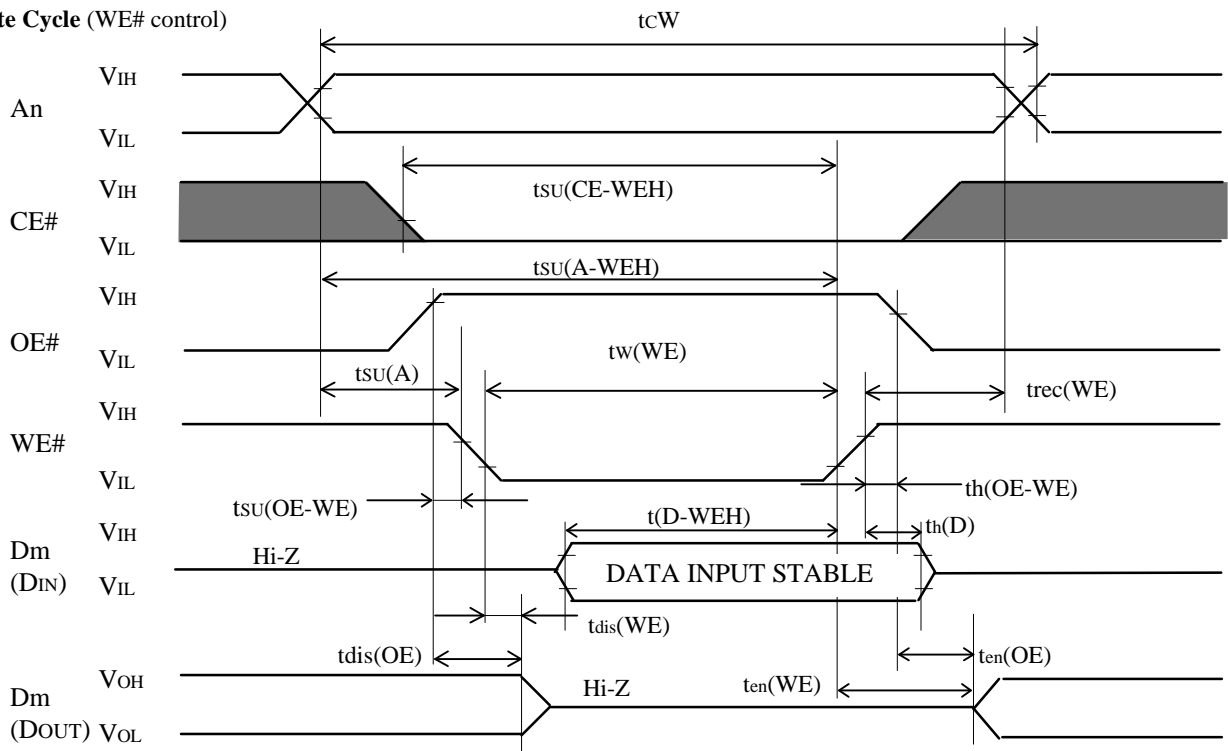
**TIMING DIAGRAM**

**Read Cycle**



WE#="H" level  
REG#="H" level

**Write Cycle (WE# control)**

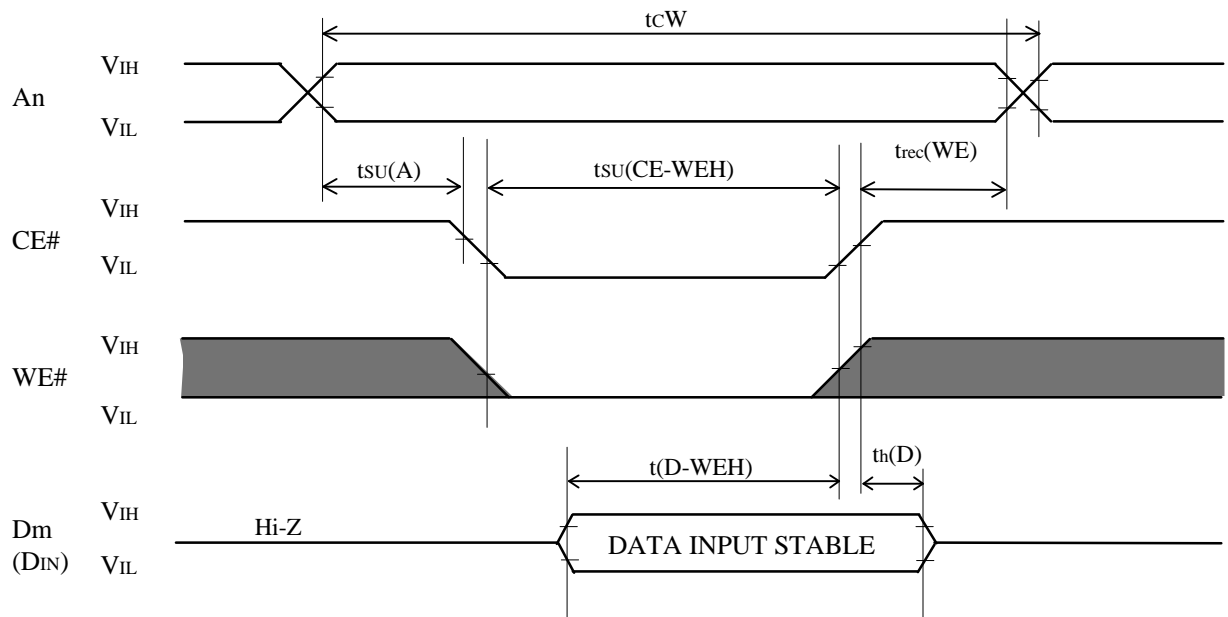


REG#="H" level





Write Cycle (CE# control)



OE#="H" level  
REG#="H" level

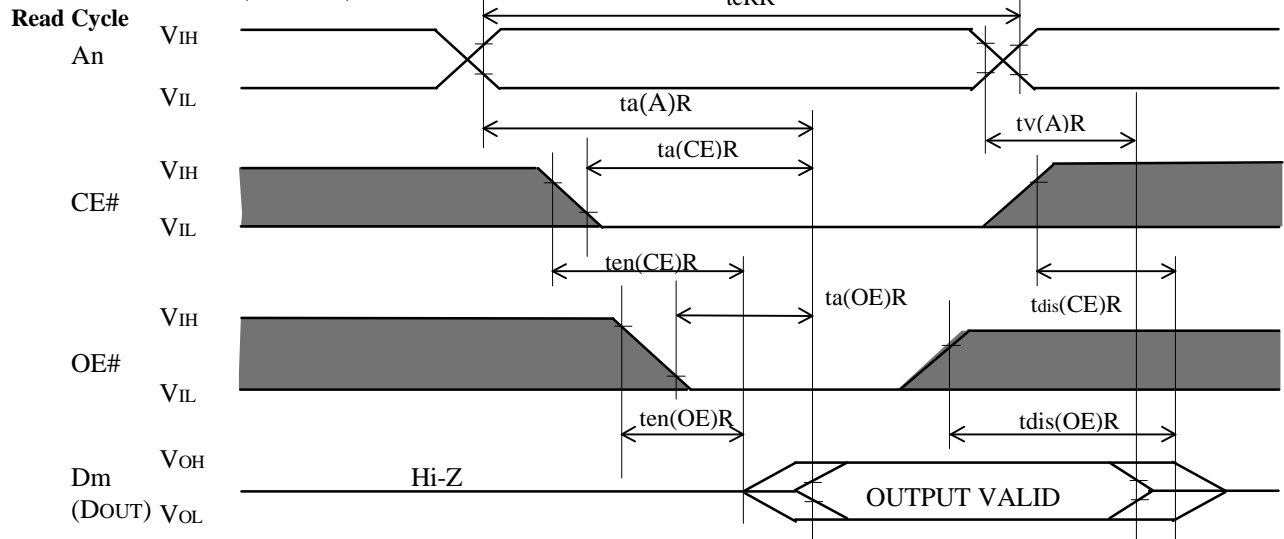
17. SWITCHING CHARACTERISTICS (Attribute)

Read Cycle (Ta=0~55°C, Vcc=4.5~5.25V, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcRR	Read cycle time	300		ns
ta(A)R	Address access time		300	ns
ta(CE)R	Card enable access time		300	ns
ta(OE)R	Output enable access time		150	ns
tdis(CE)R	Output disable time (from CE#)		100	ns
tdis(OE)R	Output disable time (from OE#)		100	ns
ten(CE)R	Output enable time (from CE#)	5		ns
ten(OE)R	Output enable time (from OE#)	5		ns
tV(A)R	Data valid time after address change	0		ns



**TIMING DIAGRAM (Attribute)**



WE#="H" level  
REG#="L" level

Note 5 : Test Conditions

Input pulse levels :  $V_{IL}=0.4V$ ,  $V_{IH}=4.0V$

Input pulse rise, fall time :  $t_r=t_f=10ns$

Reference voltage


Input :  $V_{IL}=0.8V$ ,  $V_{IH}=3.5V$

Output :  $V_{OL}=0.8V$ ,  $V_{OH}=3.0V$

( $t_{en}$  and  $t_{dis}$  are measured when output voltage is  $\pm 500mV$  from steady state.)

Load :  $100pF + 1\ TTL\ gate$

$5pF + 1\ TTL\ gate$  (at  $t_{en}$  and  $t_{dis}$  measuring)

6 :  Indicates the don't care input

7 : Writing is executed in overlap of  $CE\#$  and  $WE\#$  are "L" level. (only for Common Memory)

8 : Don't apply inverted phase signal externally when  $Dm$  pin is in output mode.

9 :  $CE\#$  is indicated as follows:

Read A/Write A :  $CE\#=CE1\#=-CE2\#$

Read B/Write B :  $CE\#=-CE1\#$ ,  $CE2\#="H"$  level

Read C/Write C :  $CE\#=-CE2\#$ ,  $CE1\#="H"$  level



**18. ELECTRICAL CHARACTERISTICS**

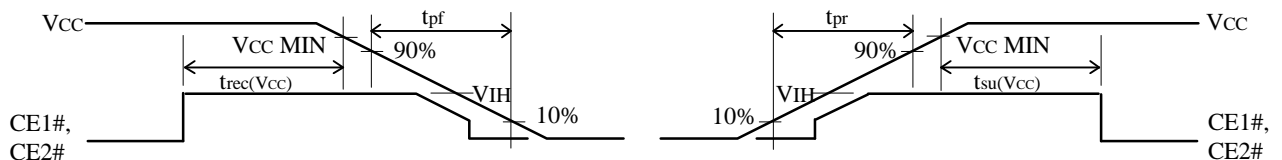
**BATTERY BACKUP** (Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V <sub>BATT</sub>	Back-up enable battery voltage	All pins open	2.6			V	
V <sub>i</sub> (CE)	Card enable voltage	3.5V ≤ V <sub>CC</sub> ≤ 5.25V	3.5			V	
		0V ≤ V <sub>CC</sub> < 3.5V	V <sub>cc</sub> -0.1	V <sub>cc</sub>	V <sub>cc</sub> +0.1		
I <sub>cc</sub> (Bup)	Battery back-up supply current	All pins open, V <sub>BATT</sub> =3V, Ta=25°C	64KB			3	μA
			128KB			3	
			256KB			3	
			512KB			5	
			1MB			3	
			2MB			5	
			4MB			9	
	Battery back-up supply current	All pins open, V <sub>BATT</sub> =3V	64KB			30	μA
			128KB			30	
			256KB			30	
			512KB			50	
			1MB			30	
			2MB			50	
			4MB			90	

**19. TIMING REQUIREMENTS** (Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			
		Min.	Typ.	Max.	
T <sub>pr</sub>	Power supply rise time	0.1		300	ms
t <sub>pf</sub>	Power supply fall time	3		300	ms
t <sub>su</sub> (V <sub>cc</sub> )	Setup time at power on	20			ms
t <sub>rec</sub> (V <sub>cc</sub> )	Recovery time at power off	1000			ns

**CARD INSERTION/REMOVAL TIMING DIAGRAM**



**20. BATTERY SPECIFICATIONS**

Please use the following coin type lithium battery.  
 Type of main battery; CR2025 or equivalents

**20.1 BATTERY LIFE EXPECTANCY**

The calculated main battery's life expectancies are as follows.

Card Type	main battery's life (when the card is left continuously)
MF365A-LYCATXX	5.9years
MF3129-LYCATXX	5.9years
MF3257-LYCATXX	5.9years
MF3513-LYCATXX	3.6years
MF31M1-LYCATXX	5.9years
MF32M1-LYCATXX	3.6years
MF34M1-LYCATXX	2.0years

Conditions; Temperature : 25°C Humidity : 60%RH

**21. CONNECTOR**

The number of card insertion and removal are as follows.

Office environment      10000 times min. at speed of 10 cycles/min.  
 Harsh environment      5000 times min. at speed of 10 cycles/min.

**22. CARD WEIGHT**      about 30g

**23. UL CLASS OF MAIN CARD PARTS**

(1) MAIN FRAME      UL94V-0  
 (2) PCB      UL94V-0  
 (3) PLASTIC PART OF CONNECTOR      UL94V-0

**24. THE BATTERY VOLTAGE DETECT SIGNALS (BVD1,2)**

BVD1	BVD2	Comment
H	H	Battery operational
H	L	Battery operational, but battery should be replaced
L	L	Battery and data integrity is not kept

Note10. The battery voltage detect signals indicate the present state of the battery.  
 They do not guarantee the data retention.

**25. CONCERNING THE SECURITY OF DATA**

There is always the possibility that a soft-error (this malfunction is not permanent hence it is called soft and the data can be restored by rewriting) may occur with semiconductor products.

When keeping the important data within an IC card, remember to give due consideration to safety when making your circuit designs, with appropriate measures such as

- (1) Keeping multiple copies of the data.
- (2) Addition of ECC or CRC by software or hardware.

**⚠ Warning ( if card with battery / card with auxiliary battery )**

- (1) Do not charge, short, disassemble, deform, heat, or throw the batteries into fire, as they may ignite, overheat, rupture or explode.
- (2) Place the batteries out of the reach of children. If somebody swallows them, they should see a doctor immediately.
- (3) When discarding or storing the batteries, wrap them individually with cellophane tape or other nonconductive material. If they are positioned in contact with any other metals or batteries, they may explode, rupture or leak electrolyte solution.

**⚠ Caution**

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**Keep safety first in your circuit designs!**

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