

**35-45GHz Single Side Band Mixer  
Self biased**

*Preliminary*

**GaAs Monolithic Microwave IC**

**Description**

The MFC\_PO10892 is a multifunction chip (MFC) which integrates a self biased LO buffer amplifier and a sub-harmonically balanced diode mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion.

It is designed for a wide range of applications, typically commercial communication systems for broadband local access. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a P-HEMT process, 0.25µm gate length. It is available in chip form.

**Main Features**

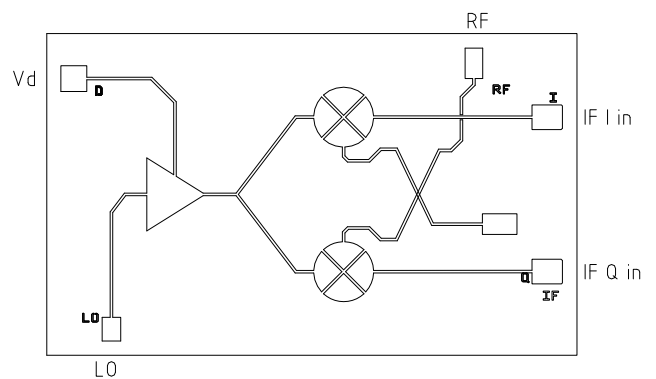
- Broadband performances : 35-45GHz
- 11dB conversion Loss
- 15dBc image rejection
- +10dBm LO input power
- +0dBm input power (1dB gain comp.)
- Power consumption 60mA@4V
- Chip size : 2.06 x 1.25 x 0.10 mm

**Main Characteristics**

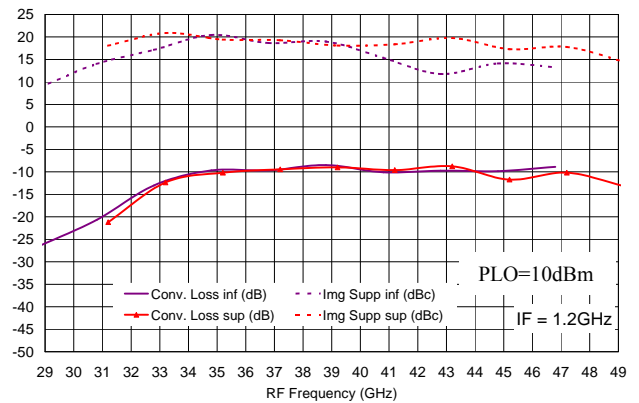
Tamb. = 25°C

	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	35		45	GHz
F <sub>LO</sub>	LO frequency range	16		24	GHz
F <sub>IF</sub>	IF frequency range	DC		3	GHz
L <sub>c</sub>	Conversion Loss		11		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !



Up converter in Infradyne & supradyn mode



## Electrical Characteristics for Broadband Operation

T<sub>amb</sub> = +25°C*Preliminary*

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>LO</sub>	LO frequency range	16		24	GHz
F <sub>IF</sub>	IF frequency range	DC		3	GHz
L <sub>c</sub>	Conversion Loss		11		dB
P <sub>LO</sub>	LO Input power		+10		dBm
2xLO Leak	2xLO Leakage (for P <sub>LO</sub> =+10dBm)		-35	-	dBm
Img Rej	Image Rejection (1)		15		dBc
P1dB	Input power at 1dB compression		+0		dBm
LO Match	LO VSWR*		2.0:1		
RF Match	RF VSWR*		2.0:1		
IF Match	IF VSWR*		2.0:1		
V <sub>d</sub>	Drain bias supply		4		V
I <sub>d</sub>	Bias current		60		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

\* A bonding wire of typically 0.1 to 0.15 nH will improve the accesses matching.

## Absolute Maximum Ratings

T<sub>amb</sub> = 25°C (1)

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	4.5	V
I <sub>d</sub>	Drain bias current	90	mA
P <sub>LO</sub>	Maximum LO input power	15	dBm
T <sub>a</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +125	°C

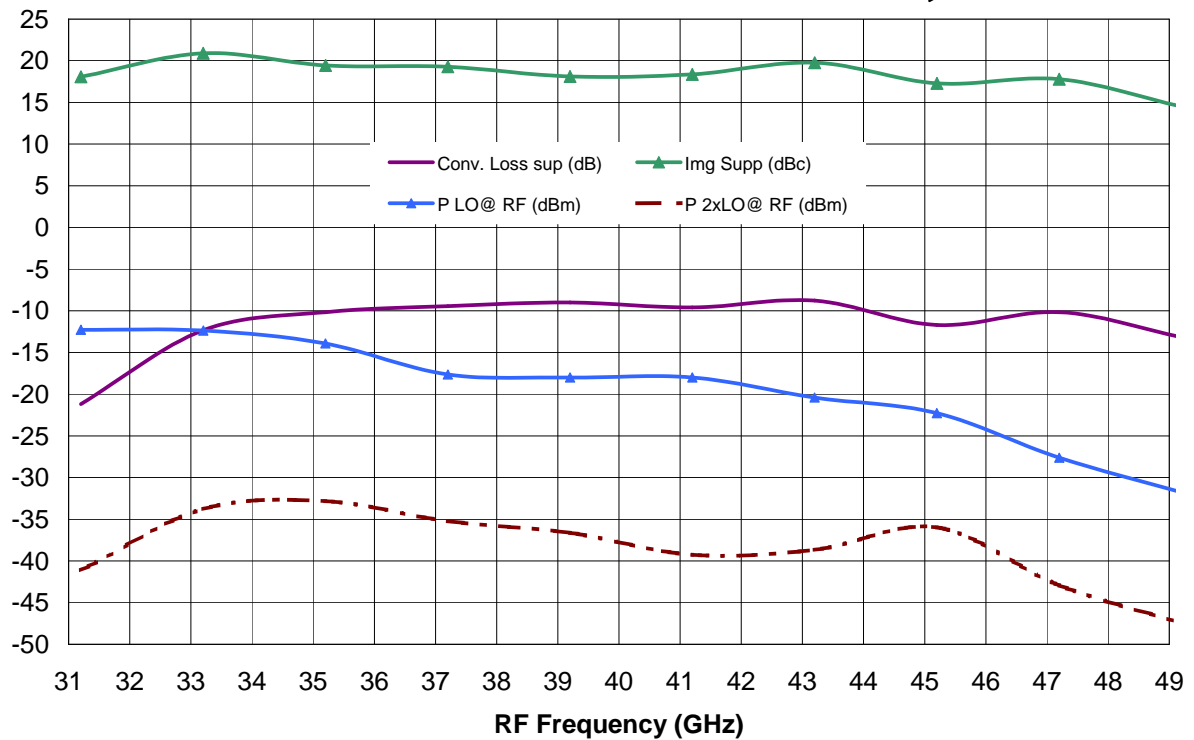
(1) Operation of this device above any one of these parameters may cause permanent damage.

## Typical on wafer measurement

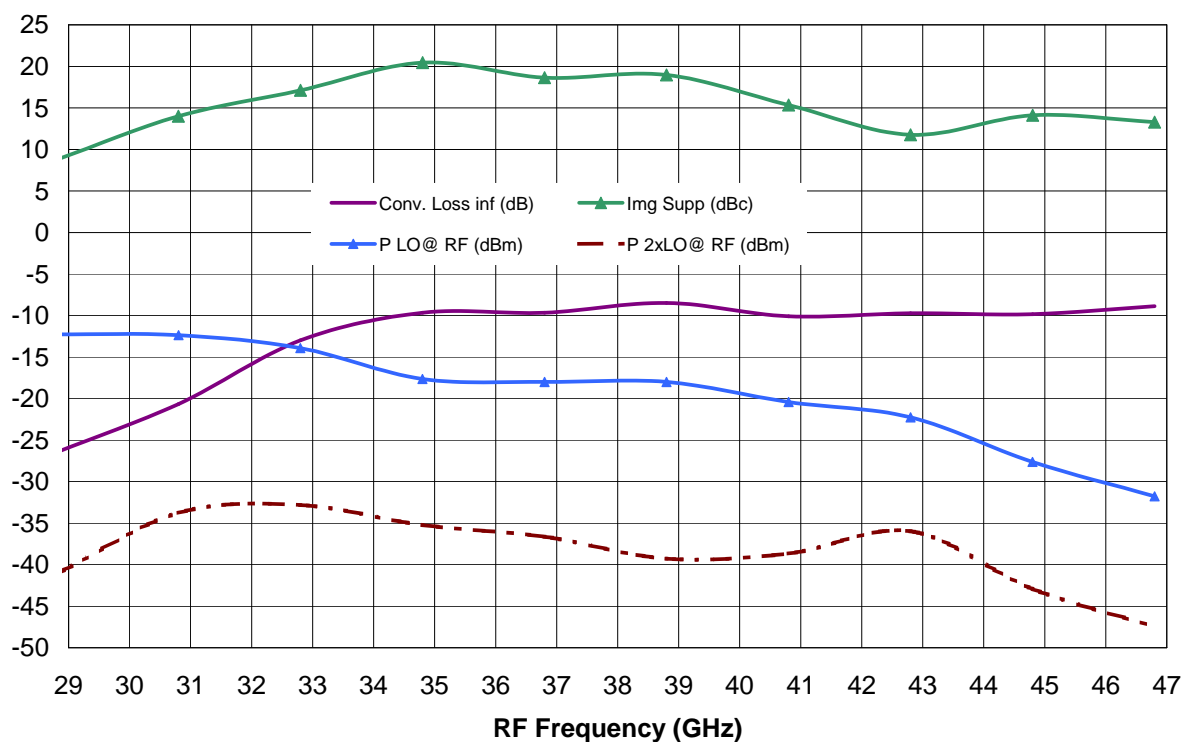
Tamb= 25°C, Vd=4V, Id=60mA, Freq IF=1.2GHz, P\_LO=10 dBm

*Preliminary*

### Up Converter in Supradyne mode

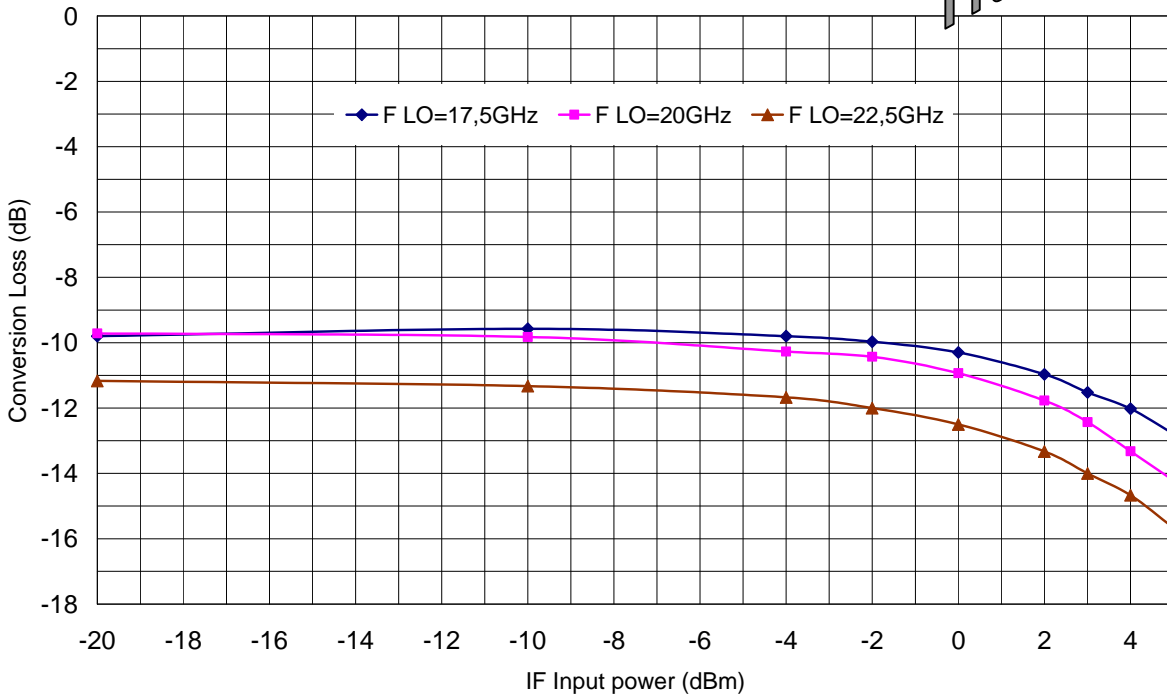


### Up Converter in Infradyne mode

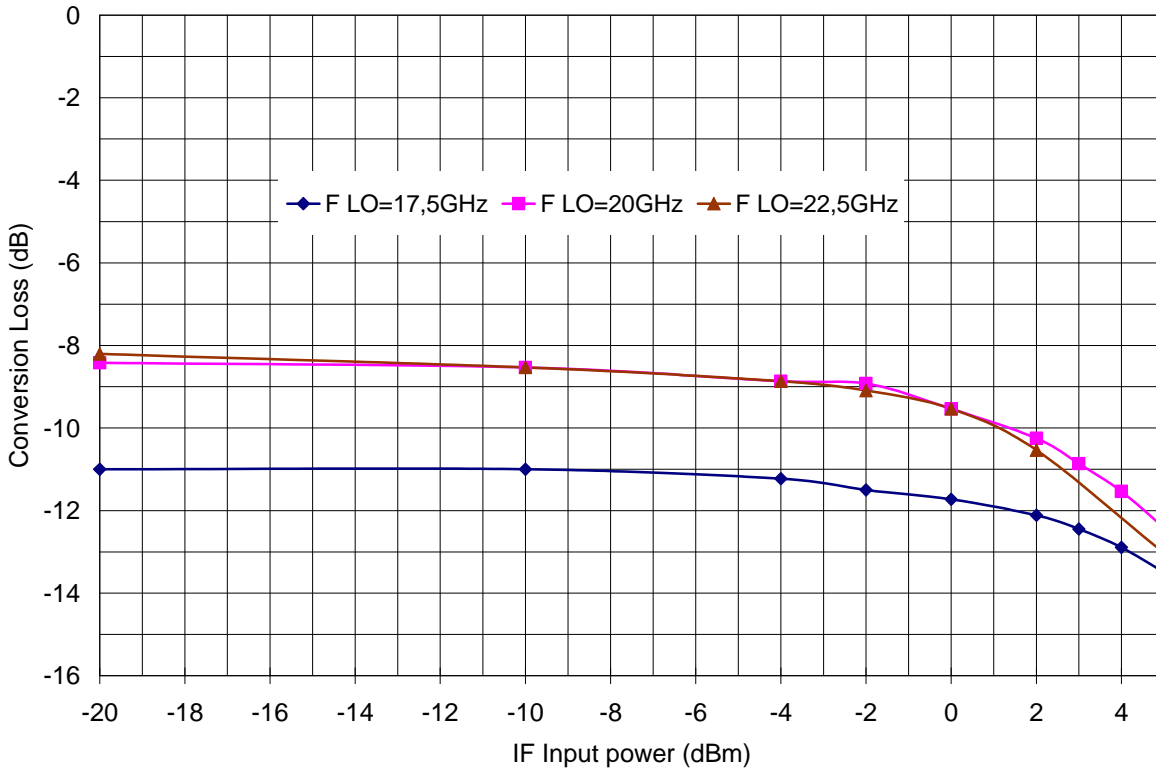


Preliminary

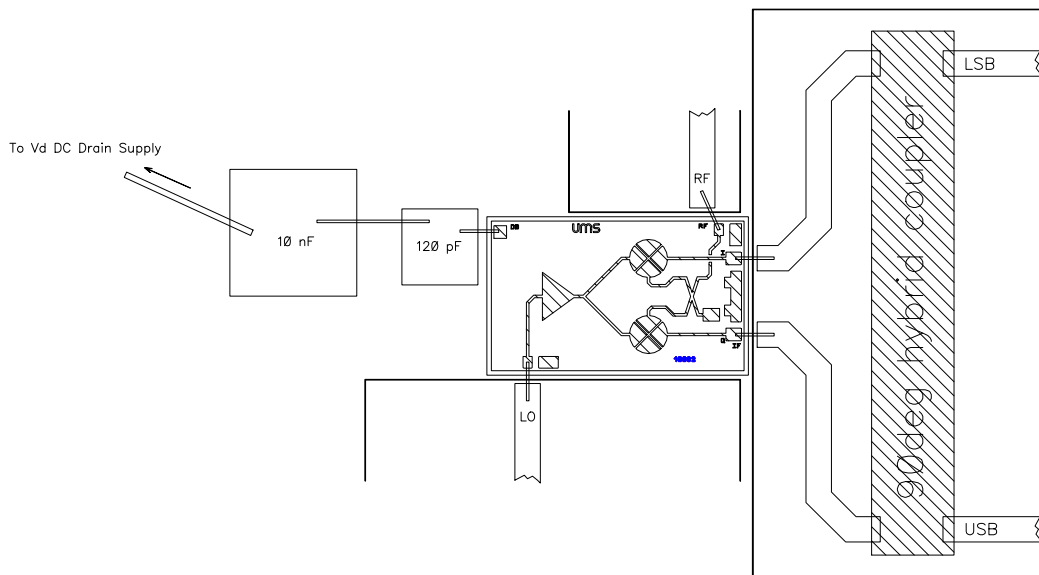
Up Converter compression in Supradyne mode



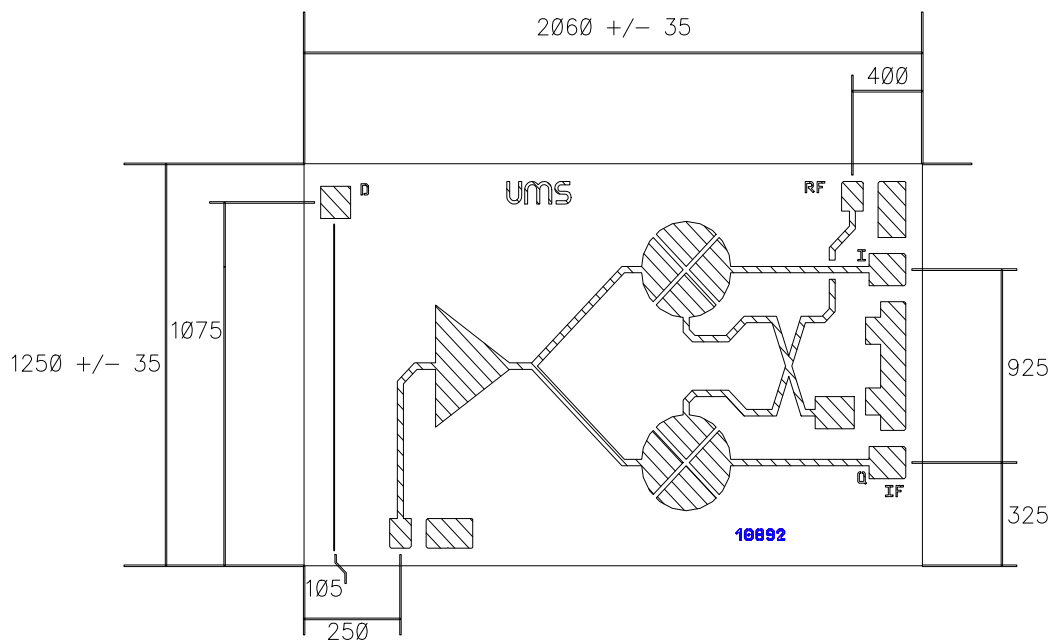
Up Converter compression in Infradyne mode



## Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



### Chip Mechanical Data and Pin references

( Chip thickness : 100µm. All dimensions are in micrometers )

*Preliminary*

## Ordering Information

Chip form: MFC-PO10892-99F/00

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