MH89770

T1/ESF Framer & Interface

Preliminary Information

ISSUE 2 March 1995

Features

- Complete interface to a bidirectional T1 link
- D3/D4 or ESF framing and SLC-96 compatible
- Two frame elastic buffer with jitter tolerance improved to 156UI
- Insertion and detection of A, B, C, D bits Signalling freeze, optional debounce
- Selectable B8ZS, jammed bit (ZCS) or no zero code suppression
- Yellow and blue alarm signal capabilities
- Bipolar violation count, F_T error count, CRC error count
- Frame and superframe sync. signals, Tx and Rx
- Per channel, overall, and remote loop around
- 8 kHz synchronization output
- Digital phase detector between T1 line and ST-BUS
- ST-BUS compatible
- Pin compatible with the MH89760BN/BS
- Inductorless clock recovery
- Loss of Signal (LOS) indication
- Available in standard, narrow and surface mount formats

Ordering Information

MH89770N	40 Pin DIL Hybrid 0.8" row pitch
MH89770S	40 Pin Surface Mount Hybrid

0°C to 70°C

Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links

Description

The MH89770 is a complete T1 interface solution, meeting the Extended Super Frame (ESF), D3/D4 and SLC-96 formats. The MH89770 interfaces to the DS1 1.544 Mbit/sec digital trunk and has the capability of meeting ACCUNET®[1] T1.5 wander tolerance (138 UI).

The MH89770 is a pin-compatible enhancement of the MH89760B.

1. ACCUNET® T1.5 is a registered trademark of AT & T.

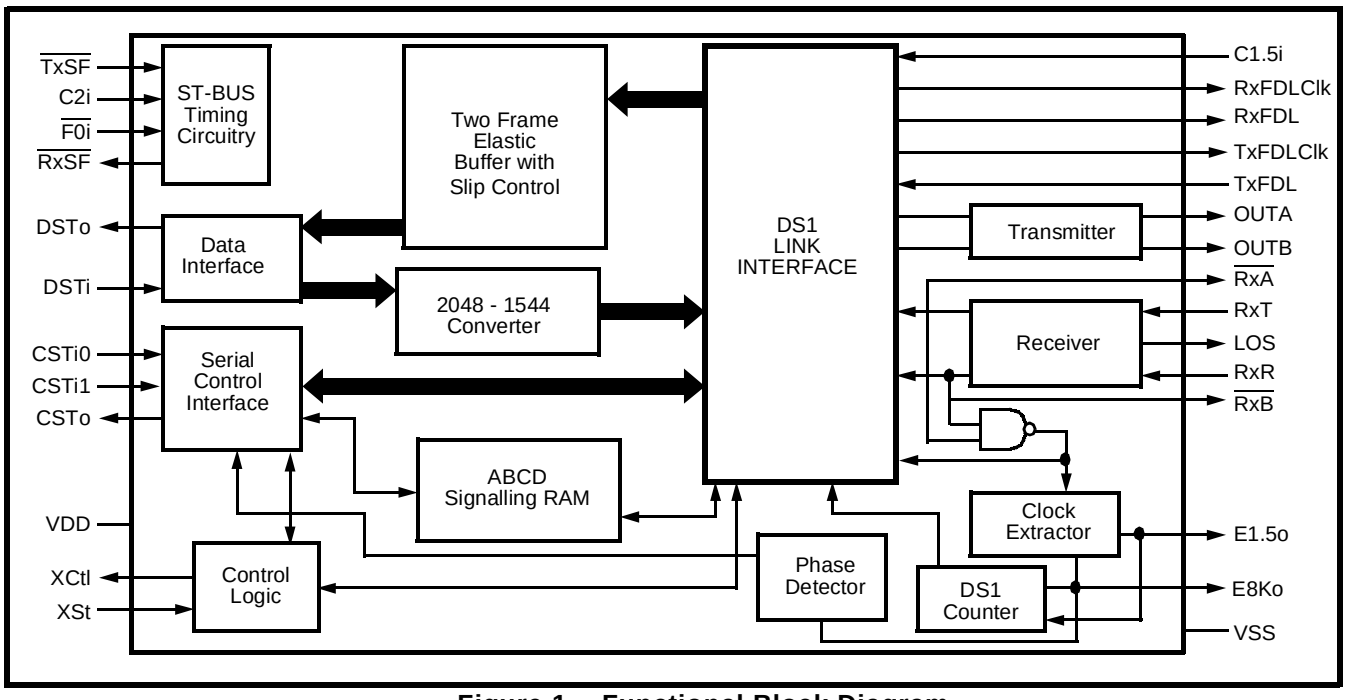


Figure 1 - Functional Block Diagram

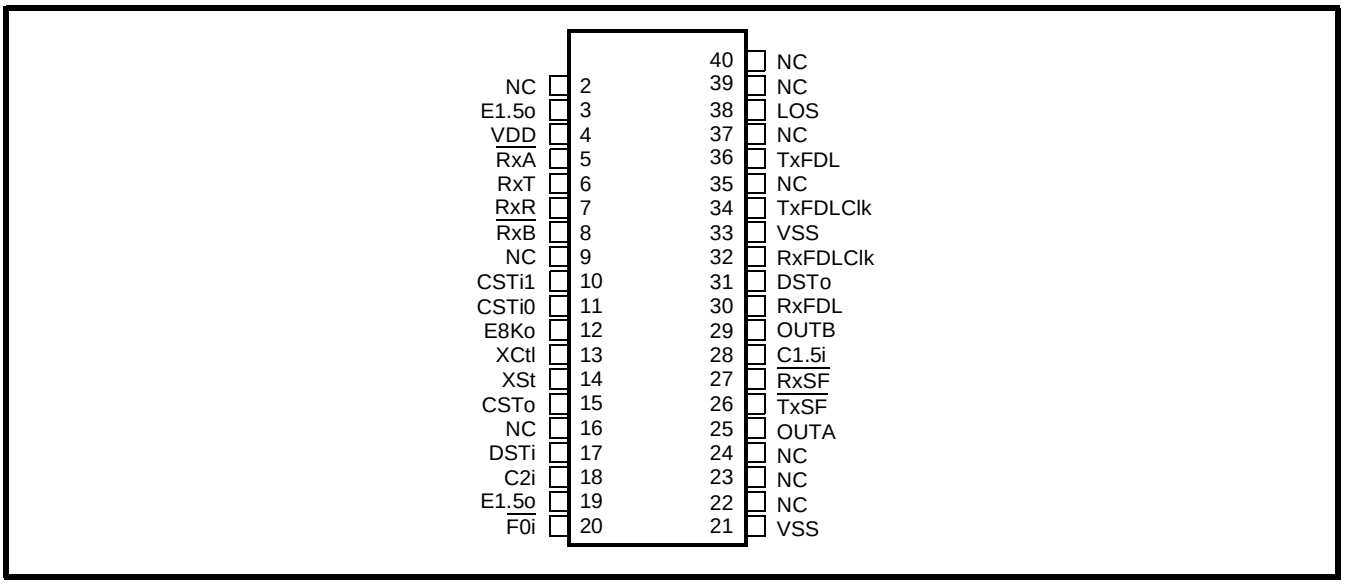


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
2	NC	**No Connection.**
3	E1.5o	**1.544 MHz Extracted Clock (Output):** This clock is extracted by the device from the received DS1 signal. It is used internally to clock in data received at RxT and RxR.
4	V_{DD}	**System Power Supply**. +5V.
5	$\overline{\text{RxA}}$	**Received A (Output):** The bipolar DS1 signal received by the device at RxR and RxT is converted to a unipolar format and output at this pin.
6 7	RxT RxR	**Receive Tip and Ring Inputs:** Bipolar split phase inputs designed to be connected directly to the input transformer. Impedance to ground is approximately 1kΩ. Impedance between pins=430Ω.
8	$\overline{\text{RxB}}$	**Received B (Output):** The bipolar DS1 signal received by the device at RxR and RxT is converted to a unipolar format and output at this pin.
9	NC	**No Connection.**
10	CSTi1	**Control ST-BUS Input #1:** A 2048 kbit/s serial control stream which carries 24 per-channel control words.
11	CSTi0	**Control ST-BUS Input #0:** A 2048 kbit/s serial control stream that contains 24 per channel control words and two master control words.
12	E8Ko	**8 kHz Extracted Clock (Output):** This is an 8 kHz output generated by dividing the extracted 1.544 MHz clock by 193 and aligning it with the received DS1 frame. The 8 kHz signal can be used for synchronizing system clocks to the extracted 1.544 MHz clock. When digital loopback is enabled, the 8kHz is derived from C1.5.
13	XCtl	**External Control (Output):** This is an uncommitted external output pin which is set or reset via bit 3 in Master Control Word 1 on CSTi0. The state of XCtl is updated once per frame.
14	XSt	**External Status (Schmitt Trigger Input):** The state of this pin is sampled once per frame and the status is reported in bit 5 of Master Status Word 2 on CSTo.
15	CSTo	**Control ST-BUS Output:** This is a 2048 kbit/s serial control stream which provides the 24 per-channel status words, and two master status words.
16	NC	**No Connection.**

Pin Description (Continued)

Pin #	Name	Description
17	DSTi	**Data ST-BUS Input:** This pin accepts a 2048 kbit/s serial stream which contains the 24 PCM or data channels to be transmitted on the T1 trunk.
18	C2i	**2.048 MHz System Clock (Input):** This is the master clock for the ST-BUS section of the chip. All data on the ST-BUS is clocked in on the falling edge of C2i and out on the rising edge.
19	E1.5o	**1.544 MHz Extracted Clock (Output):** Internally connected to Pin 3.
20	$\overline{F0i}$	**Frame Pulse Input:** This is the frame synchronization signal which defines the beginning of the 32 channel ST-BUS frame.
21	V_{SS}	**System ground.**
22-24	NC	**No Connection.**
25	OUTA	**Output A (Open Collector Output):** This is the output of the DS1 transmitter circuit. It is suitable for use with an external pulse transformer to generate the transmit bipolar line signal.
26	$\overline{TxSF}$	**Transmit Superframe Pulse Input:** A low pulse applied at this pin will determine the start of the next transmit superframe as illustrated in Figure 20. The device will free run if this pin is held high.
27	$\overline{RxSF}$	**Received Superframe Pulse Output:** A pulse output on this pin indicates that the next frame of data on the ST-BUS is from frame 1 of the received superframe. The period is 12 frames long in D3/D4 modes and 24 frames in ESF mode. Active only when device is synchronized to received DS1 signal.
28	C1.5i	**1.544 MHz Clock Input**: The rising edge of this clock is used to output data on OUTA, OUTB. C1.5i must be phase-locked to the C2i system clock.
29	OUTB	**Output B (Open Collector Output):** This is the output of the DS1 transmitter circuit. It is suitable for use with an external pulse transformer to generate the transmit bipolar line signal.
30	RxFDL	**Received Facility Data Link (Output):** A 4 kbit/s serial output stream that is demultiplexed from the FDL bits in ESF mode, or the received F_S bit pattern when in SLC96 mode. It is clocked out on the rising edge of RxFDLClk.
31	DSTo	**Data ST-BUS Output:** A 2048 kbit/s serial output stream which contains the 24 PCM or data channels received from the DS1 line.
32	RxFDLClk	**Receive Facility Data Link Clock Output:** A 4 kHz clock used to output FDL information on RxFDL. Data is clocked out on the rising edge of the clock.
33	V_{SS}	**No Connection.**
34	TxFDLClk	**Transmit Facility Data Link Clock Output:** A 4 kHz clock used to input FDL information on TxFDL. Data is clocked in on the rising edge of the clock.
35	NC	**No Connection.**
36	TxFDL	**Transmit Facility Data Link (Input)**: A 4 kbit/s serial input stream that is muxed into the FDL bits in the ESF mode, or the F_S pattern when in SLC96 mode. It is clocked in on the rising edge of TxFDLClk.
37	NC	**No Connection.**
38	LOS	**Loss of Signal (Output):** This pin goes high when 128 contiguous ZEROs are received on the RxT and RxR inputs. When LOS is high, $\overline{RxA}$ and $\overline{RxB}$ are forced high. LOS is reset when 48 ones are received in a two T1-frame period.
39	NC	**No Connection.**
40	NC	**No Connection.**

DSTi	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL TRANSMITTED

DSTo	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL RECEIVED

CSTi0	0 PCCW1	1 PCCW1	2 PCCW1	3 X	4 PCCW1	5 PCCW1	6 PCCW1	7 X	8 PCCW1	9 PCCW1	10 PCCW1	11 X	12 PCCW1	13 PCCW1	14 PCCW1	15 MCW1	16 PCCW1	17 PCCW1	18 PCCW1	19 X	20 PCCW1	21 PCCW1	22 PCCW1	23 X	24 PCCW1	25 PCCW1	26 PCCW1	27 X	28 PCCW1	29 PCCW1	30 PCCW1	31 MCW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW=Per Channel Control Word, MCW1/2=Master Control Word 1/2

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTi1	0 PCCW2	1 PCCW2	2 PCCW2	3 X	4 PCCW2	5 PCCW2	6 PCCW2	7 X	8 PCCW2	9 PCCW2	10 PCCW2	11 X	12 PCCW2	13 PCCW2	14 PCCW2	15 X	16 PCCW2	17 PCCW2	18 PCCW2	19 X	20 PCCW2	21 PCCW2	22 PCCW2	23 X	24 PCCW2	25 PCCW2	26 PCCW2	27 X	28 PCCW2	29 PCCW2	30 PCCW2	31 X
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW=Per Channel Control Word

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTo	0 PCSW	1 PCSW	2 PCSW	3 PSW	4 PCSW	5 PCSW	6 PCSW	7 X	8 PCSW	9 PCSW	10 PCSW	11 X	12 PCSW	13 PCSW	14 PCSW	15 MSW1	16 PCSW	17 PCSW	18 PCSW	19 X	20 PCSW	21 PCSW	22 PCSW	23 X	24 PCSW	25 PCSW	26 PCSW	27 X	28 PCSW	29 PCSW	30 PCSW	31 MSW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCSW=Per Channel Status Word, PSW=Phase Status Word, MSW=Master Status Word

ST-BUS VERSUS DS1 CHANNEL STATUS

X = UNUSED

Figure 3 - ST-BUS Channel Allocations

Functional Description

The MH89770 is a thick film hybrid solution for a T1 interface. All of the formatting and signalling insertion and detection is done by the device. Various programmable options in the device include: ESF, D3/D4 or SLC-96 mode, common channel or robbed bit signalling, zero code suppression, alarms, and local and remote loopback. The MH89770 also has built in bipolar line drivers and receivers and a clock extraction circuit.

All data and control information is communicated to the MH89770 via 2048 kbit/s serial streams conforming to Mitel's ST-BUS format.

The ST-BUS is a TDM serial bus that operates at 2048 kbits/s. The serial streams are divided into 125 µsec frames that are made up of 32 8-bit channels. A serial stream that is made up of these 32 8 bit channels is known as an ST-BUS stream, and one of these 64 kbit/s channels is known as an ST-BUS channel.

The system side of the MH89770 is made up of ST-BUS inputs and outputs, i.e., control inputs and outputs (CSTi/o) and data inputs and outputs (DSTi/o). These signals are functionally represented in Figure 32. The DS1 line side of the device is made up of split phase inputs (RxT, RxR) and outputs (OUTA, OUTB) which can be connected to line coupling transformers. Functional transmit and receive timing is shown in Figures 33 and 34.

Data for transmission on the DS1 line is clocked serially into the device at the DSTi pin. The DSTi pin accepts a 32 channel time division multiplexed ST-BUS stream. Data is clocked in with the falling edge of the C2i clock. ST-BUS frame boundaries are defined by the frame pulse applied at the $\overline{\text{F0i}}$ pin. Only 24 of the available 32 channels on the ST-BUS serial stream are actually transmitted on the DS1 side. The unused 8 channels are ignored by the device.

Data received from the DS1 line is clocked out of the device in a similar manner at the DSTo pin. Data is clocked out on the rising edge of the C2i clock. Only 24 of the 32 channels output by the device contain the information from the DS1 line. The DSTo pin is, however, actively driven during the unused channel timeslots. Figure 3 shows the correspondence between the DS1 channels and the ST-BUS channels.

All control and monitoring of the device is accomplished through two ST-BUS serial control inputs and one serial control output. Control ST-BUS input number 0 (CSTi0) accepts an ST-BUS serial stream which contains the 24 per channel control words and two master control words. The per channel control words relate directly to the 24 information channels output on the DS1 side. The master control words affect operation of the whole device. Control ST-BUS input number 1 (CSTi1) accepts an ST-BUS stream containing the A, B, C and D signalling bits. The relationship between the CSTi channels and the controlled DS0 channels is shown in Figure 3. Status and signalling information is received from the device via the control ST-BUS output (CSTo). This serial output stream contains two master status words, 24 per channel status words and one Phase Status Word. Figure 3 shows the correspondence between the received DS1 channels and the status words. Detailed information on the operation of the control interface is presented below.

Programmable Features

The main features in the device are programmed through two master control words which occupy channels 15 and 31 in Control ST-BUS input stream number 0 (CSTi0). These two eight bit words are used to:

- Select the different operating modes of the device ESF, D3/D4 or SLC-96.
- Activate the features that are needed in a certain application; common channel signalling, zero code suppression, signalling debounce, etc.
- Turn on in service alarms, diagnostic loop arounds, and the external control function

Tables 1 and 2 contain a complete explanation of the function of the different bits in Master Control Words 1 and 2.

Major Operating Modes

The major operating modes of the device are enabled by bits 2 and 4 of Master Control Word 2. The Extended Superframe (ESF) mode is enabled when bit 4 is set high. Bit 2 has no effect in this mode. The ESF mode enables the transmission of the S bit pattern shown in Table 3. This includes the frame/superframe pattern, the CRC-6, and the Facility Data Link (FDL). The device generates the frame/multiframe pattern and calculates the CRC for each superframe. The data clocked into the device on the TxFDL pin is incorporated into the FDL. ESF mode will also insert A, B, C and D signalling bits into the 24 frame multiframe. The DS1 frame begins after

Bit	Name	Description
7	**Debounce**	When set the received A, B, C and D signalling bits are reported directly in the per channel status words output at CSTo. When clear, the signalling bits are debounced for 6 to 9 ms before they are placed on CSTo.
6	**TSPZCS**	**Transparent Zero Code Suppression.** When this bit is set, no zero code suppression is implemented.
5	**B8ZS**	**Binary Eight Zero Suppression.** When this bit is set, B8ZS zero code suppression is enabled. When clear, bit 7 in data channels containing all zeros is forced high before being transmitted on the DS1 side. This bit is inactive if the TSPZCS bit is set.
4	**8kHSel**	**8 kHz Output Select.** When set, the E8Ko pin is held high. When clear, the E8Ko generates an 8 kHz output derived from the extracted 1.544 MHz clock or C1.5i clock (see Pin Description for E8Ko).
3	**XCtl**	**External Control Pin.** When set, the XCtl pin is held high. When clear, XCtl is held low.
2	**ESFYLW**	**ESF Yellow Alarm.** Valid only in ESF mode. When set, a sequence of eight 1's followed by eight 0's is sent in the FDL bit positions. When clear, the FDL bit contains data input at the TxFDL pin.
1	**Robbed bit**	When this bit is set, robbed bit signalling is disabled on all DS0 transmit channels. When clear, A, B, C and D signalling bits are inserted into bit position 8 of all DS0 channels in every 6th frame.
0	**YLALR**	**Yellow Alarm.** When set, bit 2 of all DS0 channels is set low. When clear, bit 2 operates normally.

Table 1. Master Control Word 1 (Channel 15, CSTi0)

Bit	Name	Description
7	**RMLOOP**	**Remote Loopback.** When set, the data received at RxR and RxT is looped back to OUTB and OUTA respectively. The data is clocked into the device with the extracted 1.544 MHz clock. The device still monitors the received data and outputs it at DSTo. The device operates normally when the bit is clear.
6	**DGLOOP**	**Digital Loopback.** When set, the data input on DSTi is looped around to DSTo. The normal received data on RxR and RxT is ignored. However, the data input at DSTi is still transmitted on OUTA and OUTB. The device frames up on the looped data using the C1.5i clock.
5	**ALL1'S**	**All One's Alarm.** When set, the chip transmits an unframed all 1's signal on OUTA and OUTB.
4	**ESF/D4**	**ESF/D4 Select.** When set, the device is in ESF mode. When clear, the device is in D3/D4 mode.
3	**ReFR**	**Reframe.** If set for at least one frame and then cleared, the chip will begin to search for a new frame position. Only the change from high to low will cause a reframe, not a continuous low level.
2	**SLC-96**	**SLC-96 Mode Select.** The chip is in SLC-96 mode when this bit is set. This enables input and output of the F_S bit pattern using the same pins as the facility data link in ESF mode. The chip will use the same framing algorithm as D3/D4 mode. The user must insert the valid F_S bits in 2 out of 6 superframes to allow the receiver to find superframe sync, and the transmitter to insert A and B bits in every 6th frame. The SLC-96 FDL completely replaces the F_S pattern in the outgoing S bit position. Inactive in ESF mode.
1	**CRC/MIMIC**	In ESF mode, when set, the chip disregards the CRC calculation during synchronization. When clear, the device will check for a correct CRC before going into synchronization. In D3/D4 mode, when set, the device will synchronize on the first correct S-bit pattern detected. When this bit is clear, the device will not synchronize if it has detected more than one candidate for the frame alignment pattern (i.e., a mimic).
0	**Maint.**	**Maintenance Mode.** When set, the device will declare itself out-of-sync if 4 out of 12 consecutive F_T bits are in error. When clear, the out-of-sync threshold is 2 errors in 4 F_T bits. In this mode, four consecutive bits following an errored F_T bit are examined.

Table 2. Master Control Word 2 (Channel 31, CSTi0)

approximately 25 periods of the C1.5i clock from the F0i frame pulse.

Frame #	FPS	FDL	CRC	Signalling †
1		X		
2			CB1	
3		X		
4	0			
5		X		
6			CB2	A
7		X		
8	0			
9		X		
10			CB3	
11		X		
12	1			B
13		X		
14			CB4	
15		X		
16	0			
17		X		
18			CB5	C
19		X		
20	1			
21		X		
22			CB6	
23		X		
24	1			D

Table 3. ESF Frame Pattern

† These signalling bits are only valid if the robbed bit signalling is active.

‡

During synchronization the receiver locks on to the incoming frame, calculates the CRC and compares it to the CRC received in the next multiframe. The device will not declare itself to be in synchronization unless a valid framing pattern in the S-bit is detected and a correct CRC is received. The CRC check in this case provides protection against false framing. The CRC check can be turned off by setting bit 1 in Master Control Word 2.

The device can be forced to resynchronize itself. If Bit 3 in Master Control Word 2 is set for one frame and then subsequently reset, the device will start to search for a new frame position. The decision to reframe is made by the user's system processor on the basis of the status conditions detected in the received master status words. This may include consideration of the number of errors in the received CRC in conjunction with an indication of the presence of a mimic. When the device attains synchronization the mimic bit in Master Status Word 1 is set if the device found another possible candidate when it was searching for the framing pattern.

Note that the device will resynchronize automatically if the errors in the terminal framing pattern (F_T or FPS) exceed the threshold set with bit 0 in Master Control Word 2.

Frame #	F_T	F_S	Signalling †
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

Table 4. D3/D4 Framer

† These signalling bits are only valid if the robbed bit signalling is active.

Standard D3/D4 framing is enabled when bit 4 of Master Control Word 2 is reset (logic 0). In this mode the device searches for and inserts the framing pattern shown in Table 4. This mode only supports AB bit signalling, and does not contain a CRC check.

The CRC/MIMIC bit in Master Control Word 2, when set high, allows the device to synchronize in the presence of a mimic. If this bit is reset, the device will not synchronize in the presence of a mimic. (Also refer to section on Framing Algorithm.)

In the D3/D4 mode the device can also be made compatible with SLC-96 by setting bit two of Master Control Word 2. This allows the user to insert and extract the signalling framing pattern on the DS1 bit stream using the FDL input and output pins. The user must format this 4 kbits of information externally to meet all of the requirements of the SLC-96 specification (see Table 5). The device multiplexes and demultiplexes this information into the proper position. This mode of operation can also be used for any other application that uses all or part of the signalling framing pattern. As long as the serial stream clocked into the TxFDL contains two proper sets of consecutive synchronization bits (as shown in Table 5 for frames 1 to 24), the device will be able to insert and extract the A, B signalling bits. The $\overline{\text{TxSF}}$ pin should be held high in this mode. Superframe boundaries cannot be defined by a pulse on this input. The $\overline{\text{RxSF}}$ output functions normally and indicates the superframe boundaries based on the synchronization pattern in the F_S received bit position.

Frame #	F_T	F_S†	Notes	Frame #	F_T	F_S†	Notes
1	1		Resynchronization Data Bits	37	1		X = Concentrator Field Bits
2		0		38		X	
3	0			39	0		
4		0		40		X	
5	1			41	1		
6		0		42		X	
7	0			43	0		
8		1		44		X	
9	1			45	1		
10		1		46		X	
11	0			47	0		S = Spoiler Bits
12		1		48		S	
13	1			49	1		
14		0		50		S	
15	0			51	0		
16		0		52		S	
17	1			53	1		
18		0		54		C	C = Maintenance Field Bits
19	0			55	0		
20		1		56		C	
21	1			57	1		
22		1		58		C	
23	0			59	0		A = Alarm Field Bits
24		1		60		A	
25	1		X =Concentrator Field Bits	61	1		
26		X		62		A	
27	0			63	0		L = Line Switch Field Bits
28		X		64		L	
29	1			65	1		
30		X		66		L	
31	0			67	0		
32		X		68		L	
33	1			69	1		
34		X		70		L	
35	0			71	0		S = Spoiler Bits
36		X		72		S	

Table 5. SLC-96 Framing Pattern

† Note: The FS pattern has to be supplied by the user.

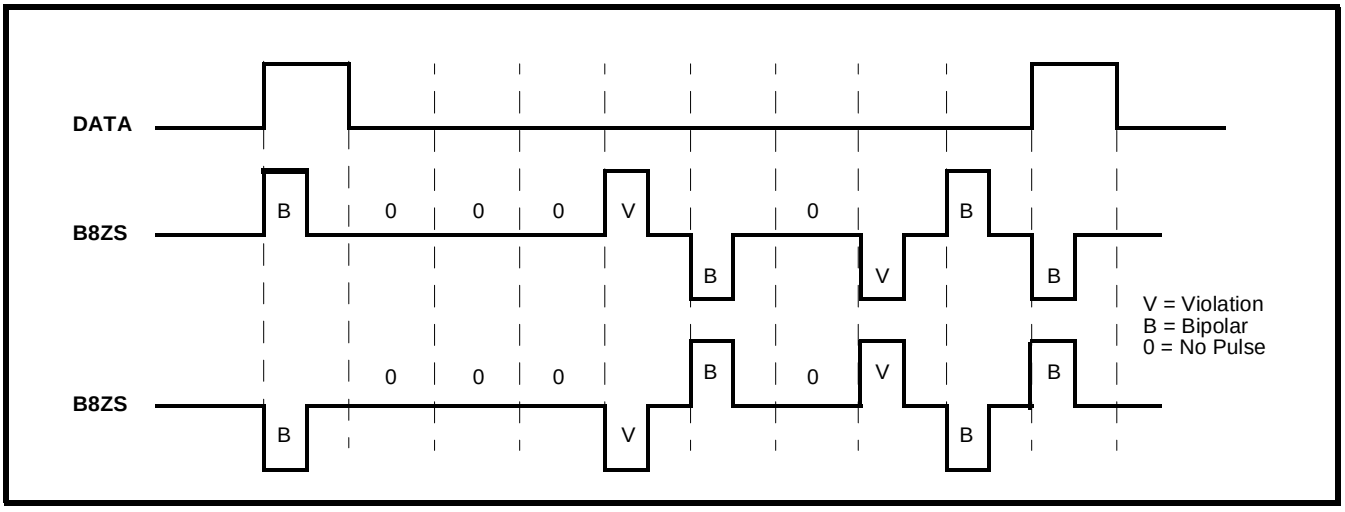


Figure 4 - B8ZS Output Coding

Zero Code Suppression

The combination of bits 5 and 6 in Master Control Word 1 allow one of three zero code suppression schemes to be selected. The three choices are: none, binary 8 zero suppression (B8ZS), or jammed bit (bit 7 forced high). No zero code suppression allows the device to interface with systems that have already applied some form of zero code suppression to the data input on DSTi. B8ZS zero code suppression replaces all strings of 8 zeros with a known bit pattern and a specific pattern of bipolar violations. This bit pattern and violation pattern is shown in Figure 4. The receiver monitors the received bit pattern and the bipolar violation pattern and replaces all matching strings with 8 zeros.

Loopback Modes

Remote and digital loopback modes are enabled by bits 6 and 7 in Master Control Word 2. These modes can be used for diagnostics in locating the source of a fault condition. Remote loop around loops back data received at RxR and RxT back out on OUTA and OUTB, thus effectively sending the received DS1 data back to the far end unaltered so that the transmission line can be tested. The received signal with the appropriate received channels on the DS1 side made available in the proper format at DSTo.

The digital loop around mode diverts the data received at DSTi back out the DSTo pin. Data received on DSTi is, however, still transmitted out via OUTA and OUTB. This loop back mode can be used to test the near end interface equipment when there is no transmission line or when there is a suspected failure of the line.

The all ones transmit alarm (also known as the blue alarm or the keep alive signal) can be activated in conjunction with the digital loop around so that the transmission line sends an all 1's signal while the normal data is looped back locally.

The MH89770 also has a per channel loopback mode. See Table 6 and the following section for more information.

Per Channel Control Features

In addition to the two master control words in CSTi0 there are also 24 Per Channel Control Words. These control words only affect individual DS0 channels. The correspondence between the channels on CSTi0 and the affected DS0 channel is shown in Fig. 3. Each control word has three bits that enable robbed bit signalling, DS0 channel loopback and inversion of the DS0 channel. A full description of each of the bits is provided in Table 6.

Transmit Signalling Bits

Control ST-BUS input number 1 (CSTi1) contains 24 additional per channel control words. These 24 ST-BUS channels contain the A, B, C and D signalling bits that the device uses at transmit time. The position of these 24 per channel control words in the ST-BUS is shown in Figure 3 and the position of the ABCD signalling bits is shown in Table 7. Even though the device only inserts the signalling

Bit	Name	Description
7-3	IC	**Internal Connections.** Must be kept at 0 for normal operation.
2	Polarity	When set, the applicable channel is not inverted on the transmit or the receive side of the device. When clear, all the bits within the applicable channel are inverted both on transmit and receive side.
1	Loop	**Per Channel Loopback.** When set, the received DS0 channel is replaced with the transmitted DS0 channel. Only one DS0 channel may be looped back in this manner at a time. The transmitted DS0 channel remains unaffected. When clear the transmit and receive DS0 sections operate normally.
0	Data	**Data Channel Enable.** When set, robbed bit signalling for the applicable channel is disabled. When clear, every 6th DS1 frame is available for robbed bit signalling. This feature is enabled only if bit 1 in Master Control Word is low.

Table 6. Per Channel Control Word 1 Input at CSTi0

Bit	Name	Description
7-4	Unused	Keep at 0 for normal operation
3 2 1-0	A B C, D	These are the 4 signalling bits inserted in the appropriate channels of the DS1 stream being output from the chip, when in ESF mode. In D3/D4 modes where there are only two signalling bits, the values of C and D are ignored.

Table 7. Per Channel Control Word 2 Input at CSTi1

Bit	Name	Description
7	YLALR	**Yellow Alarm Indication.** This bit is set when the chip is receiving a 0 in bit position 2 of every DS0 channel.
6	MIMIC	This bit is set if the frame search algorithm found more than one possible frame candidate when it went into frame synchronization.
5	ERR	**Terminal Framing Bit Error.** The state of this bit changes every time the chip detects 4 errors in the F_T or FPS bit pattern. The bit will not change state more than once every 96ms.
4	ESFYLW	**ESF Yellow Alarm.** This bit is set when the device has observed a sequence of eight one's and eight 0's in the FDL bit positions.
3	$\overline{\text{MFSYNC}}$	**Multiframe Synchronization.** This bit is cleared when D3/D4 multiframe synchronization has been achieved. Applicable only in D3/D4 and SLC-96 modes of operation.
2	BPV	**Bipolar Violation Count.** The state of this bit changes every time the device counts 256 bipolar violations.
1	SLIP	**Slip Indication.** This bit changes state every time the elastic buffer in the device performs a controlled slip.
0	$\overline{\text{SYN}}$	**Synchronization.** This bit is set when the device has not achieved synchronization. The bit is clear when the device has synchronized to the received DS1 data stream.

Table 8. Master Status Word 1 (Channel 15, CSTo)

Bit	Name	Description
7	BlAlm	**Blue Alarm.** This bit is set if the receiver has detected two frames of 1's and an out of frame condition. It is reset by any 250 microsecond interval that contains a zero.
6	FrCnt	**Frame Count.** This is the ninth and most significant bit of the "Phase Status Word" (see Table 10). If the phase status word is incrementing, this bit will toggle when the phase reading exceeds channel 31, bit 7. If the phase word is decrementing, then this bit will toggle when the reading goes below channel 0, bit 0.
5	XSt	**External Status.** This bit reflects the state of the external status pin (XSt). The state of the XSt pin is sampled once per frame.
4-3	BPVCnt	**Bipolar Violation Count.** These two bits change state every 128 and every 64 bipolar violations, respectively.
2-0	CRCCNT	**CRC Error Count.** These three bits count received CRC errors. The counter will reset to zero when it reaches terminal count. Valid only in ESF mode.

Table 9. Master Status Word 2 (Channel 31, CSTo)

Bit	Name	Description
7-3	ChannelCnt	**Channel Count.** These five bits indicate the ST-BUS channel count between the ST-BUS frame pulse and the rising edge of E8Ko.
2-0	BitCnt	**Bit Count.** These three bits provide one bit resolution within the channel count described above.

Table 10. Phase Status Word (Channel 3, CSTo)

information in every 6th DS1 frame this information must be input every ST-BUS frame.

Robbed bit signalling can be disabled for all channels on the DS1 link by bit 1 of Master Control Word 1. It can also be disabled on a per channel basis by bit 0 in the Per Channel Control Word 1.

Operating Status Information

Status Information regarding the operation of the device is output serially via the Control ST-BUS output (CSTo). The CSTo serial stream contains Master Status Words 1 and 2, 24 Per Channel Status Words, and a Phase Status Word. The Master Status Words contain all of the information needed to determine the state of the interface and how well it is operating. The information provided includes frame and super frame synchronization, slip, bipolar

Bit	Name	Description
7-4	**Unused**	Unused Bits. Will be output as 0's.
3 **2** **1** **0**	**A** **B** **C** **D**	These are the 4 signalling bits as extracted from the received DS1 bit stream. The bits are debounced for 6 to 9 ms if the debounce feature is enabled via bit 7 in Master Control Word 1.

Table 11. Per Channel Status Word Output on CSTo

violation counter, alarms, CRC error count, F_T error count, synchronization pattern mimic and a phase status word. Tables 8 and 9 give a description of each of the bits in Master Status Words 1 and 2, and Table 10 gives a description of the Phase Status Word.

In addition, the MH89770 has a Loss of Signal (LOS) pin that is set High when 128 consecutive ZEROs are received. While LOS is set High, $\overline{RxA}$ and $\overline{RxB}$ are forced High. The LOS signal goes Low when a ONEs density on 12.5% of the bits (equivalent to 48 bits) occurs in a two DS1 frame period.

Alarm Detection

The device detects the yellow alarm for both D3/D4 frame format and ESF format. The D3/D4 yellow alarm will be activated if a '0' is received in bit position 2 of every DS0 channel for 600 msec. It will be released in 200 msec after the contents of the bit change. The alarm is detectable in the presence of errors on the line. The ESF yellow alarm will become active when the device has detected a string of eight 0's followed by eight 1's in the facility data link. It is not detectable in the presence of errors on the line. This means that the ESF yellow alarm will drop out for relatively short periods of time, so the system will have to integrate the ESF yellow alarm. The blue alarm signal, in Master Status Word 2, will also drop out if there are errors on the line.

Mimic Detection

The mimic bit in Master Status Word 1 will be set if, during synchronization, a frame alignment pattern (F_T or FPS bit pattern) was observed in more than one position, i.e., if more than one candidate for the frame synchronization position was observed. It will be reset when the device resynchronizes. The mimic bit, the terminal framing error bit and the CRC error counter can be used separately or together to decide if the receiver should be forced to reframe.

Bipolar Violation Counter

The Bipolar Violation bit in Master Status Word 1 will toggle after 256 violations have been detected in the received signal. It has a maximum refresh time of 96 ms. This means that the bit can not change state faster than once every 96 ms. For example, if there are 256 violations in 80 ms the BPV bit will not change state until 96 ms. Any more errors in that extra 16 ms are not counted. If there are 256 errors in 200 ms then the BPV bit will change state after 200 ms. In practical terms this puts an upper limit on the error rate that can be calculated from the BPV information, but this rate (1.7×10^{-3}) is well above any normal operating condition.

Bits 4 and 3 also provide bipolar violations infor-mation. Bit 4 will change state after 128 violations. Bit 3 changes state after 64 bipolar violations. These bits are refreshed independently and are not subject to the 96 ms refresh rate described above.

DS1/ST-BUS Phase Difference

An indication of the phase difference between the ST-BUS and the DS1 frame can be ascertained from the information provided by the eight bit Phase Status Word and the Frame Count bit. Channel three on CSTo contains the Phase Status Word. Bits 7-3 in this word indicate the number of ST-BUS channels between the ST-BUS frame pulse and the rising edge of the E8Ko signal. The remaining three bits provide one bit resolution within the channel count indicated by bits 7-3. The frame count bit in Master Status Word 2 is the ninth and most significant bit of the phase status word. It will toggle when the phase status word increments above channel 31, bit 7 or decrements below channel 0, bit 0. The E8Ko signal has a specific relationship with received DS1 frame. The rising edge of E8Ko occurs during bit 2, channel 17 of the received DS1 frame. The Phase Status Word in conjunction with the frame count bit, can be used to monitor the phase relationship between the received DS1 frame and the local ST-BUS frame.

The local 2.048 MHz ST-BUS clock must be phase-locked to the 1.544 MHz clock extracted from the received data. When the two clocks are not phase-locked, the input data rate on the DS1 side will differ from the output data rate on the ST-BUS side. If the average input data rate is higher than the

average output data rate, the channel count and bit count in the phase status word will be seen to decrease over time, indicating that the E8Ko rising edge, and therefore the DS1 frame boundary is moving with respect to the ST-BUS frame pulse. Conversely, a lower average input data rate will result in an increase in the phase reading.

In an application where it is necessary to minimize jitter transfer from the received clock to the local system clock, a phase lock loop with a relatively large time constant can be implemented using information provided by the phase status word. In such a system, the local 2.048 MHz clock is derived from a precision VCO. Frequency corrections are made on the basis of the average trend observed in the phase status word. For example, if the channel count in the phase status word is seen to increase over time, the feedback applied to the VCO is used to decrease the system clock frequency until a reversal in the trend is observed.

The elastic buffer in the MT8977 permits the device to handle 26 ST-BUS channels or 156 UI of jitter/ wander (see description of elastic buffer in the next section). In order to prevent slips from occurring, the frequency corrections would have to be implemented such that the deviation in the phase status word is limited to 26 channels peak-to-peak. It is possible to use a more sophisticated protocol, which would center the elastic buffer and permit more jitter/wander to be handled. However, for most applications, including ACCUNET® T1.5 (138 UI), the 156 UI of jitter/wander tolerance is acceptable.

Received Signalling Bits

The A, B, C and D signalling bits are output from the device in the 24 Per Channel Status Words. Their location in the serial steam output at CSTo is shown in Figure 3 and the bit positions are shown in Table 11. The internal debouncing of the signalling bits can be turned on or off by Master Control Word 1. In ESF mode, A, B, C and D bits are valid. Even though the signalling bits are only received once every six frames the device stores the information so that it is available on the ST-BUS every frame. The ST-BUS will always contain the most recent signalling bits. The state of the signalling bits is frozen if synchronization is lost.

In D3/D4 mode, only the A and B bits are valid. The state of the signalling bits is frozen when terminal frame synchronization is lost. The freeze is disabled when the device regains terminal frame synchronization. The signalling bits may go through a random transition stage until the device attains multiframe synchronization.

Clock and Framing Signals

The MH89770 has a built in clock extraction circuit which creates a 1.544 MHz clock synchronized to the received DS1 signal. This clock is used internally by the MH89770 to clock in data received on RxT and RxR, and is also output at the E1.5o pin. The circuit has been designed to operate within the constraints imposed by the minimum 1's density requirements, typically specified for T1 networks (maximum of 15 consecutive 0's).

The extracted clock is internally divided by 193 and aligned with the received DS1 frame. The resulting 8 kHz signal is output at the E8Ko pin and can be used to phase lock the local system C2 and the transmit C1.5 clocks to the extracted clock.

The MH89770 requires three clock signals which have to be generated externally. The ST-BUS interface on the device requires a 2.048 MHz signal which is applied at the C2i pin and an 8 kHz framing signal applied at the $\overline{F0i}$ pin. The framing signal is used to delimit individual ST-BUS frames. Figure 19 illustrates the relationship between the C2i and $\overline{F0i}$ signals. The $\overline{F0i}$ signal can be derived from the 2.048 MHz C2 clock. The transmit side of the DS1 interface requires a 1.544 MHz clock applied at C1.5i. The C1.5 and C2 clocks must be phase locked. There must be 193 clock cycles of the C1.5 clock for every 256 cycles of the C2 clock in order for the 2.048 to 1.544 rate converter to function properly.

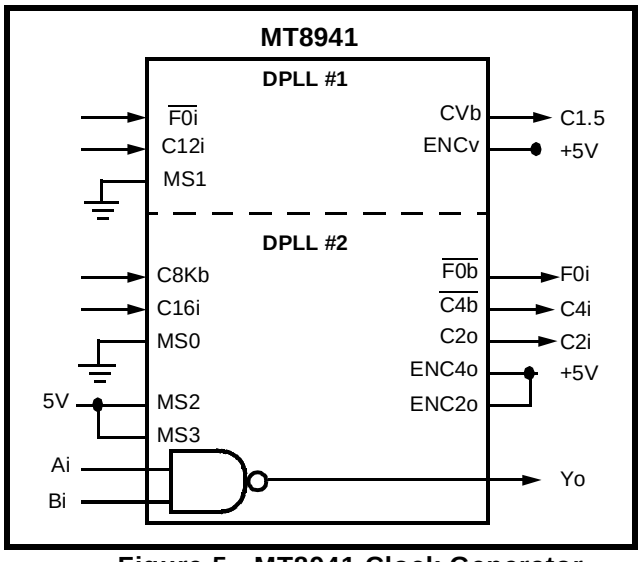
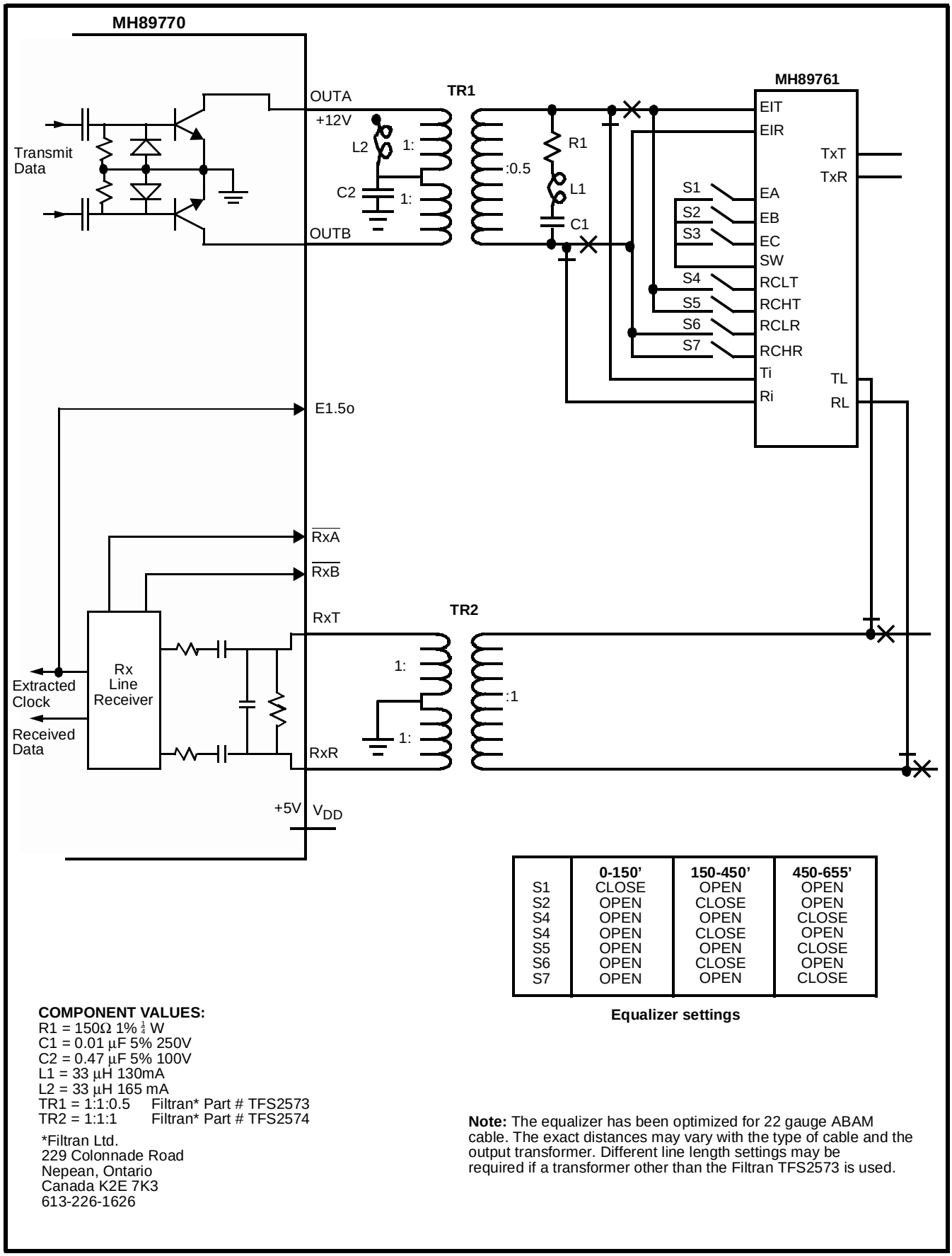


Figure 5 - MT8941 Clock Generator



	0-150'	150-450'	450-655'
S1	CLOSE	OPEN	OPEN
S2	OPEN	CLOSE	OPEN
S4	OPEN	OPEN	CLOSE
S4	OPEN	CLOSE	OPEN
S5	OPEN	OPEN	CLOSE
S6	OPEN	CLOSE	OPEN
S7	OPEN	OPEN	CLOSE

Equalizer settings

COMPONENT VALUES:
R1 = 150Ω 1% ¼ W
C1 = 0.01 µF 5% 250V
C2 = 0.47 µF 5% 100V
L1 = 33 µH 130mA
L2 = 33 µH 165 mA
TR1 = 1:1:0.5 Filtran* Part # TFS2573
TR2 = 1:1:1 Filtran* Part # TFS2574

*Filtran Ltd.
229 Colonnade Road
Nepean, Ontario
Canada K2E 7K3
613-226-1626

Note: The equalizer has been optimized for 22 gauge ABAM cable. The exact distances may vary with the type of cable and the output transformer. Different line length settings may be required if a transformer other than the Filtran TFS2573 is used.

Figure 6 - Input/Output Configuration

In synchronous operation the slave end of the link must have its C2 and C1.5 clocks phase locked to the extracted clock. In plesiochronous clocking applications where the master and slave end are operating under controlled slip conditions, phase locking to the extracted clock is generally not required.

Mitel's MT8941 Digital Phase Lock Loop (DPLL) can be used to generate all timing signals required by the MH89770. The MT8941 has two DPLLs built into the device. Figure 5 shows how DPLL #1 can be set up to generate the C1.5 clock phase locked to the F0i which in turn is derived from the same source as the C2 clock. Figure 5 also shows how DPLL #2 is set up to generate the ST-BUS clocks that are phase locked to the received data rate. If E8Ko from the MH89770 is connected to the C8Kb input on the MT8941, DPLL #2 in the device will generate the ST-BUS clocks that are phase locked to the T1 line.

DS1 Line Interface

Line Transmitter

The transmit line interface is made up of two open collector drivers (OUTA and OUTB) that can be coupled to the line with a center tapped pulse transformer (see Figure 6). A step function is applied to the transformer when either of the transistors is turned on. By operating in the transient portion of the inductance response, the secondary of the transformer produces an almost square pulse. The capacitor and inductor on the center tap of the transmit transformer shown in Figure 6 suppress transients in the 12 volt supply. The series RLC across the output of the transformer shape the pulse to meet the AT & T or CCITT pulse templates. A detailed transformer specification is presented in the applications section of this data sheet.

To complete the interfaces to the transmit line, a pre-equalizer and line impedance matching network is required. The pulse output at the transformer secondary must be pre-equalized to drive different lengths of cable. Mitel's MH89761 T1 Equalizer is configurable to provide pre-emphasis for 0-150, 150-450 and 450-655 foot lengths of 22 AWG transmission line. A separate 6dB pad is also provided on the MH89761 for use in implementing external looparound. Both circuits have input and output impedance of 100Ω. Figure 6 shows how the equalizer is connected in a typical application. (Refer to the MH89761 data sheet for more details.)

Line Receiver

The bipolar receiver inputs on the device, RxT and RxR, are intended to be coupled to the line through a center tapped pulse transformer as shown in Figure 6. The device presents a 400Ω impedance to the receive transformer to permit matching to 100Ω twisted pair cable. The signal detect threshold level of the receiver circuit is set at approximately 1.5V. There is no equalization of the received signal. The receiver circuit is designed to accurately decode a signal attenuated by a maximum of 3 dB from the digital crossconnect point. The MH89770 is not designed to directly accept a signal from the last network repeater. Interface to the public network generally requires a Channel Service Unit (CSU). The receiver decodes the bipolar signal into a split phase unipolar return to zero format. The two resulting unipolar signals are used for bipolar violation detection within the device and are also output at RxA and RxB. The input jitter tolerance of the MH89770 is shown in Figure 7.

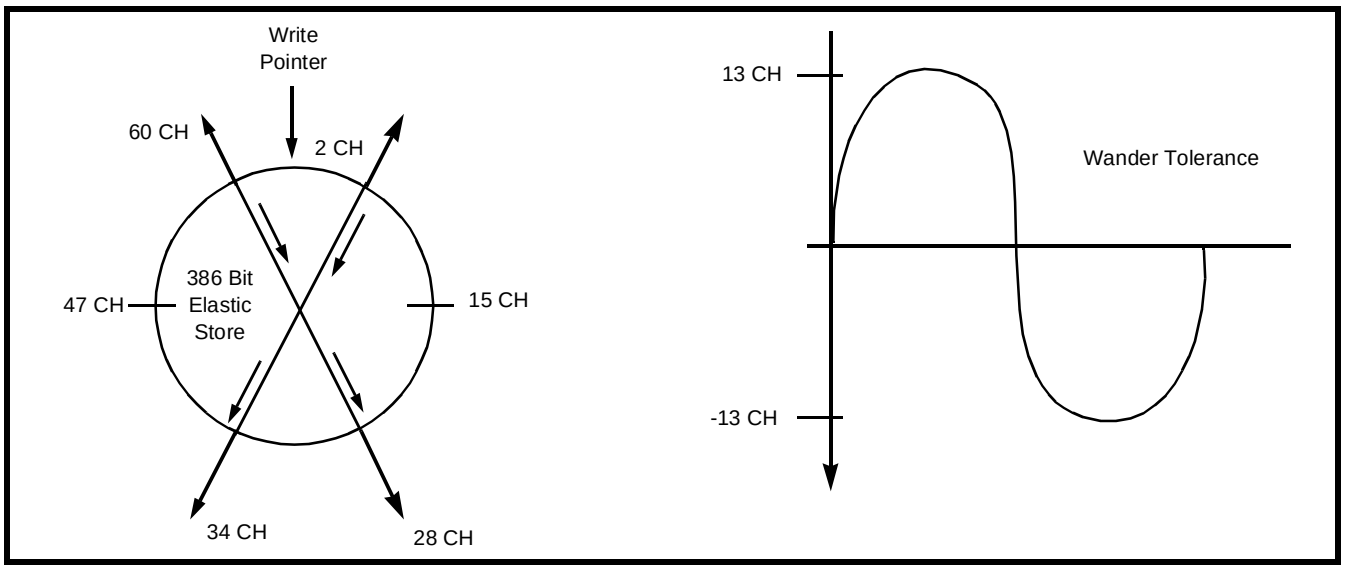


Figure 7 - Elastic Buffer Functional Diagram (156 UI Wander Tolerance)

Elastic Buffer

The MH89770 has a two frame elastic buffer which absorbs jitter in the received DS1 signal. The buffer is also used in the rate conversion between the 1.544 Mbit/s DS1 rate and the 2.048 Mbit/s ST-BUS data rate.

The received data is written into the elastic buffer with the extracted 1.544 MHz clock. The data is read out of the buffer on the ST-BUS side with the system 2.048 MHz clock. The maximum delay through the buffer is 1.875 ST-BUS frames or 60 ST-BUS channels, see Figure 7. The minimum delay required to avoid bus contention in the buffer memory is two ST-BUS channels.

Under normal operating conditions, the system C2i clock is phase locked to the extracted E1.5o clock using external circuitry. If the two clocks are not phase-locked, then the rate at which the data is being written into the device on the DS1 side may differ from the rate at which it is being read out on the ST-BUS side. The buffer circuit will perform a controlled slip if the throughput delay conditions described above are violated. For example, if the data on the DS1 side is being written in at a rate slower than what it is being read out on the ST-BUS side, the delay between the received DS1 write pointer and the ST-BUS read pointer will begin to decrease over time. When this delay approaches the minimum two channel threshold, the buffer will perform a controlled slip which will reset the internal ST-BUS read pointers so that there is exactly 34 channels delay between the two pointers. This will result in some ST-BUS channels containing information output in the previous frame. Repetition of up to one DS1 frame of information is possible.

Conversely, if the data on the DS1 side is being written into the buffer at a rate faster than it is being read out on the ST-BUS side, the delay between the DS1 frame and the ST-BUS frame will increase over time. A controlled slip will be performed when the throughput delay exceeds 60 ST-BUS channels. This slip will reset the internal ST-BUS counters so that there is a 28 channel delay between the DS1 write pointer and the ST-BUS read pointer, resulting in loss of up to one frame of received DS1 data.

Figure 7 illustrates the relationship between the read and write pointers of the receive elastic buffer. Measuring clockwise from the write pointer, if the read pointer comes within two channels of the writer pointer a frame slip will occur, which will put the read pointer 34 channels from the write pointer. Conversely, if the read pointer moves more than 60 channels from the write pointer, a slip will occur, which will put the read pointer 28 channels from the write pointer. This provides a worst case hysteresis of 13 ST-BUS channels peak (26 ST-BUS channels peak-to-peak). This can be translated into a low frequency jitter (wander) tolerance value, accounting for the DS1 to ST-BUS rate conversion, as follows:

$$(1.544/2.048) \times 26 \times 8 = 156 \text{ UI pp.}$$

There is no loss of frame sync, multiframe sync or any errors in the signalling bits when the device performs a slip. The information on the FDL pins in ESF or SLC-96 mode will, however, undergo slips at the same time.

Framing Algorithm

A state diagram of the framing algorithm is shown in Figure 8. The dotted lines show which feature can be switched in and out depending upon the operating mode of the device.

In ESF mode, the framer searches for the FPS bits. Once this pattern is detected and verified, bit 0 in Master Status Word 1 is cleared.

When the device is operating in the D3/D4 format, the framer searches for the F_T pattern, i.e., a repeating 1010... pattern in a specific bit position every alternate frame. It will synchronize to this pattern and declare valid terminal frame synchronization by clearing bit 0 in Master Status Word 1. The device will subsequently initiate a search for the F_S pattern to locate the signalling frames (see Figure 21). When a correct F_S pattern has been located, bit 3 in Master Status Word 1 is cleared indicating that the device has achieved multiframe synchronization.

Note: the device will remain in terminal frame synchronization even if no F_S pattern can be located.

In D3/D4 format, when the CRC/MIMIC bit in Master Control Word 1 is cleared, the device will not go into synchronization if more than one bit position in the frame has a repeating 1010.... pattern, i.e., if more than one candidate for the terminal framing position is located. The framer will continue to search until only one terminal framing pattern candidate is discovered. It is, therefore, possible that the device may not synchronize at all in the presence of PCM code sequences (e.g., sequences generated by some types of test signals) which contain mimics of the terminal framing pattern.

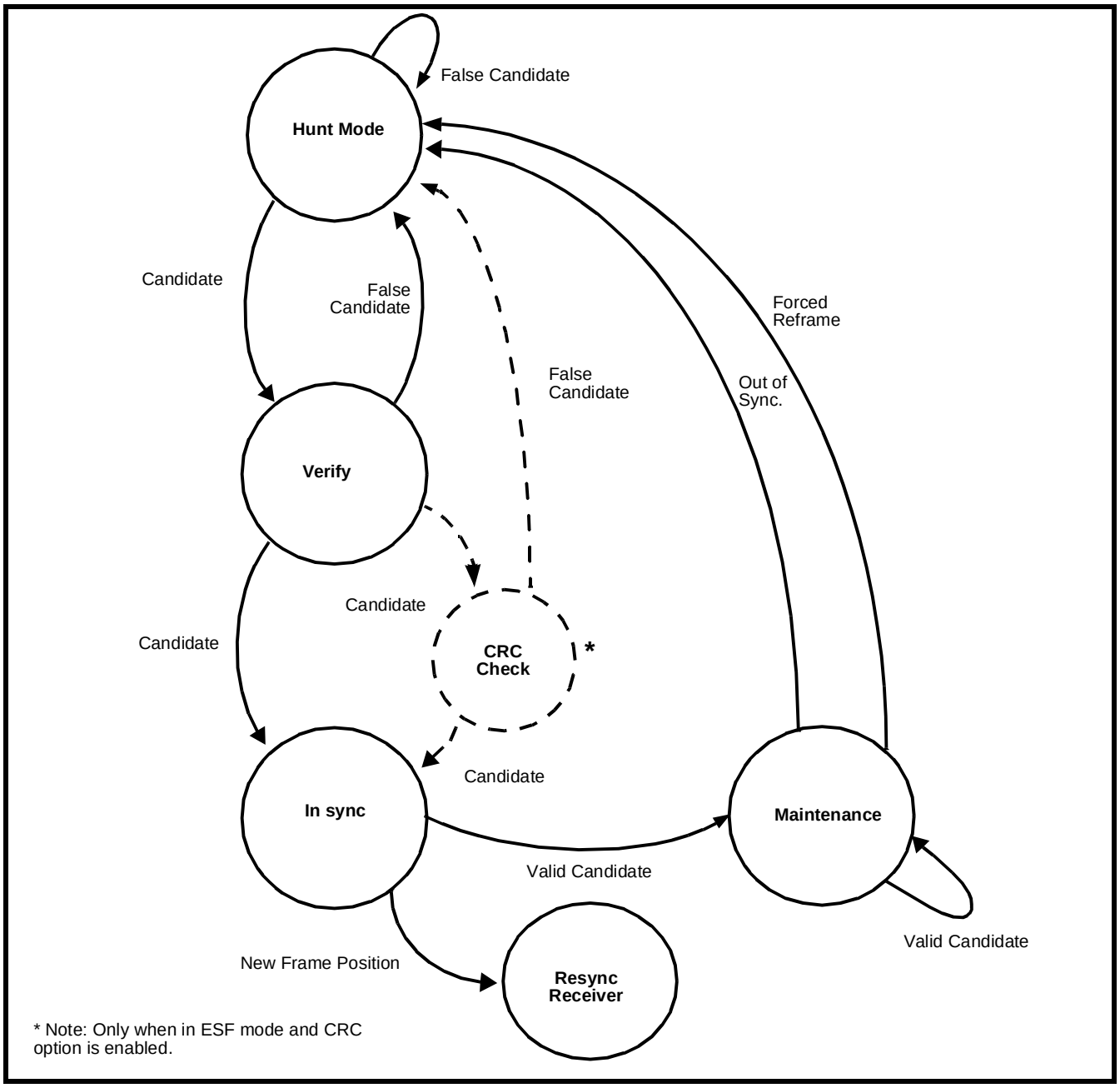


Figure 8 - Off-Line Framer State Diagram

Setting CRC/MIMIC bit high will force the framer to synchronize to the first terminal framing pattern detected. In standard D3/D4 applications, the user's system software should monitor the multiframe synchronization state indicated by bit 3 in Master Status Word 1. Failure of the device to achieve multiframe synchronization within 4.5ms of terminal frame synchronization, is an indication that the device has framed up to a terminal framing pattern mimic and should be forced to reframe.

One of the main features of the framer is that it performs its function "off line". That is, the framer repositions the receive circuit only when it has detected a valid frame position. When the framer exits maintenance mode the receive counters remain where they are until the framer has found a new frame position. This means that if the user forces a reframe when the device was really in the right place, there will not be any disturbance in the circuit because the framer has no effect on the receiver until it has found synchronization. The out of synchronization criterion can be controlled by bit 0 in Master Control Word 2. This bit changes the out of frame conditions for the maintenance state.

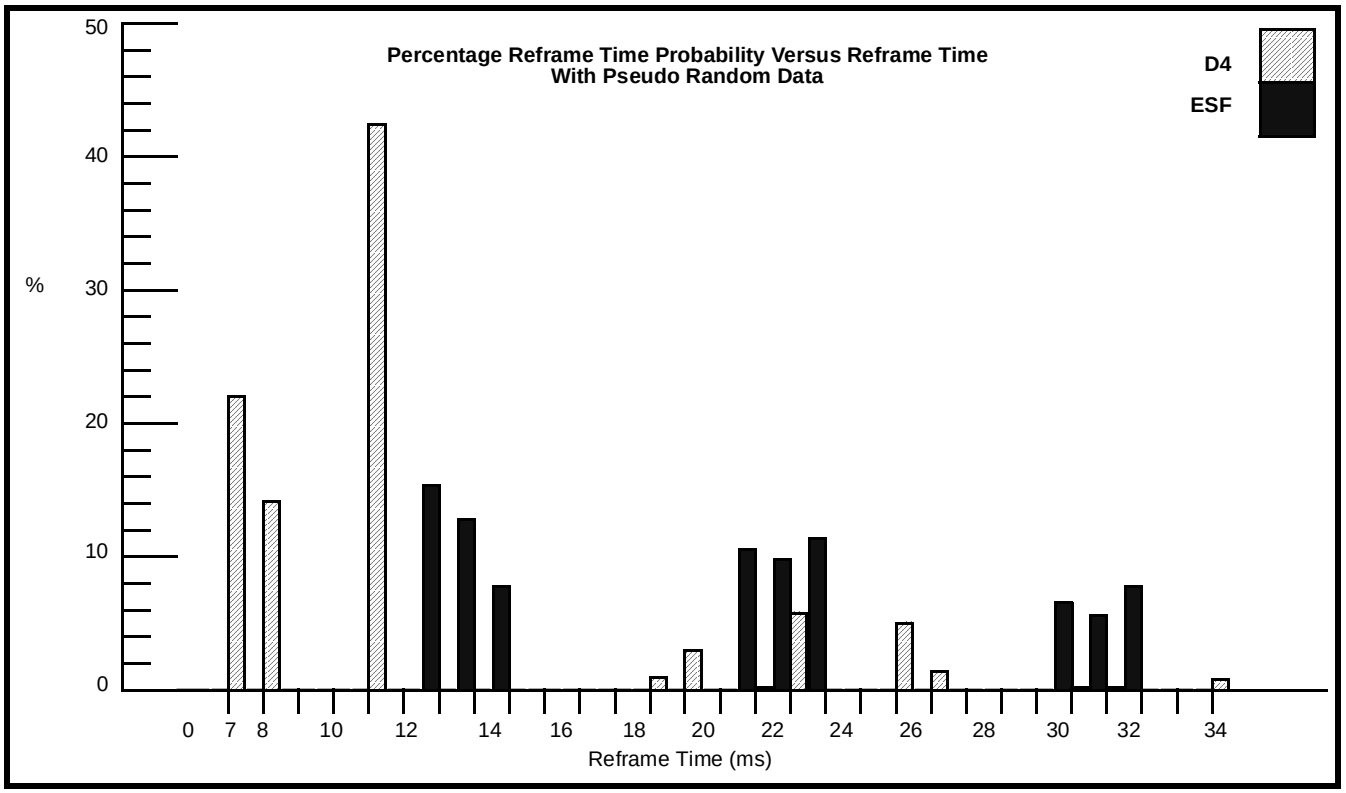


Figure 9 - Reframe Time

The out of sync threshold can be changed from 2 out of 4 errors in F_T (or FPS) to 4 out of 12 errors in FT (or FPS). The average reframe time is 24 ms for ESF mode, and 12ms for D3/D4 modes.

Figure 9 is a bar graph which shows the probability of achieving frame synchronization at a specific time. The chart shows the results for ESF mode with CRC check, and D3/D4 modes of operation. The average reframe time with random data is 24 ms for ESF, and 13 ms for D3/D4 modes. The probability of a reframe time of 35 ms or less is 88% for ESF mode, and 97% for D3/D4 modes. In ESF mode it is recommended that the CRC check be enabled unless the line has a high error rate. With the CRC check disabled the average reframe time is greater because the framer must also check for mimics.

Applications

1. Typical T1 Application

Figure 10 shows the external components that are required in a typical T1 application using the MH89770. The MT8980 is used to control and monitor the device as well as switch data to DSTi and DSTo (refer to Application Note MSAN-123 for more information on the operation of the MT8980). The MT8952, HDLC protocol controller, is shown in this application to illustrate how the data on the FDL could be used. The digital phase-locked loop, the MT8941, provides all the clocks necessary to make a functional interface. The 1.544 MHz clock extracted by the MH89770 is used to clock in data at RxT and RxR. It is also internally divided by 193 to obtain an 8 kHz clock which is output at E8Ko. The MT8941 uses this 8 kHz signal to provide a phase locked 2.048 MHz clock for the ST-BUS interface and a 1.544 MHz clock for the DS1 transmit side.

Note: the configurations shown in Figures 10 and 12 using the MT8941 may not meet specific jitter performance requirements. A more sophisticated PLL may be required for applications designed to meet specific standards. Please refer to the MT8941 data sheet for further details on its jitter performance.

The split phase unipolar signals output by the MT8977 at TxA and TxB are used by the line driver circuit to generate a bipolar AMI signal. The line driver is transformer coupled to an equalization circuit and the DS1 line. Equalization of the transmitted signal is required to meet AT & T specifications for crossconnect compatible equip-ment (see AT&T Technical Advisory #34). Specifica-tions for the input and output transformers are shown in Figure 11. On the receive side the bipolar line signal is converted into a unipolar format by the line receiver circuit. The resulting split phase signals are input at the $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ pins on the

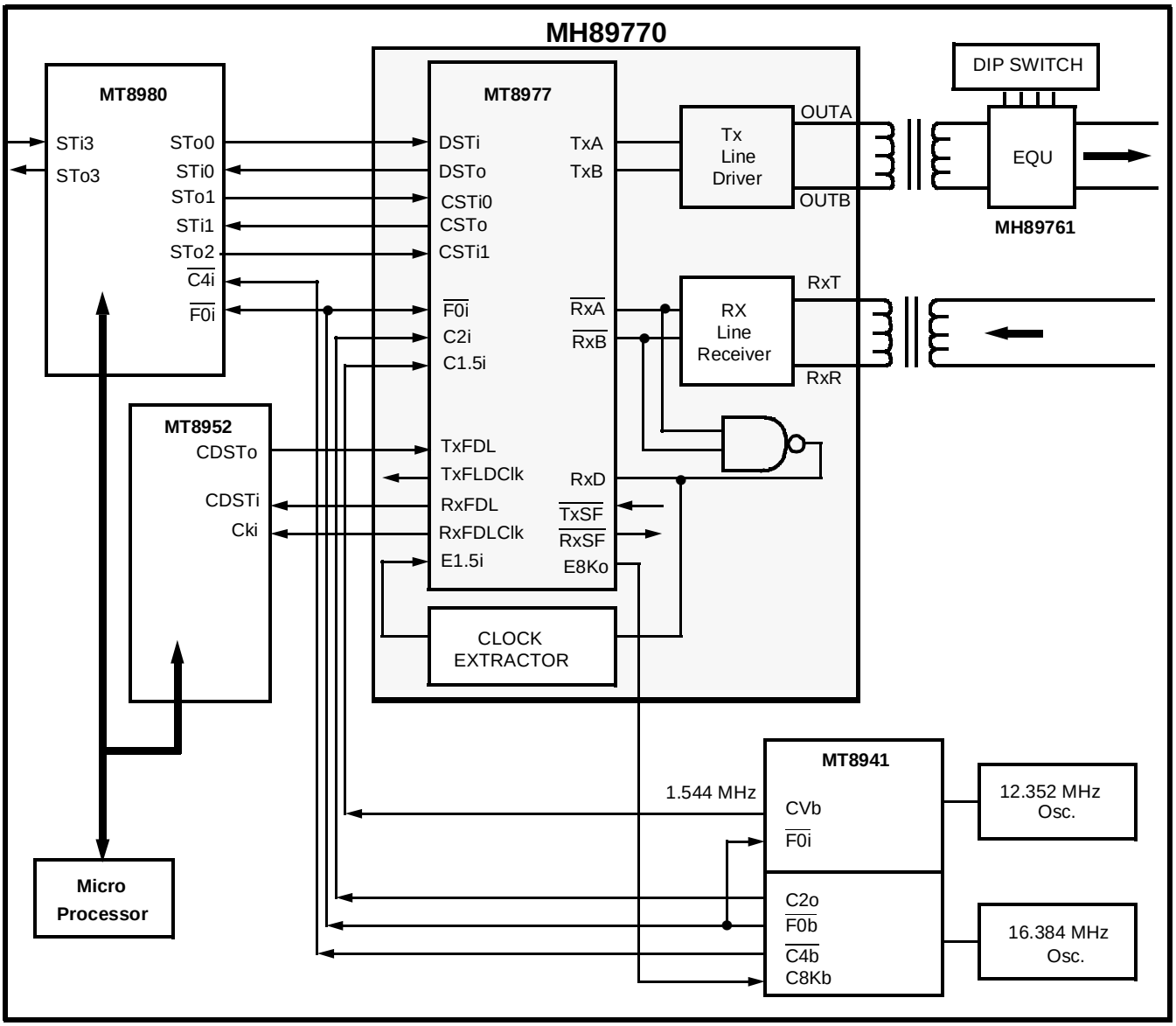
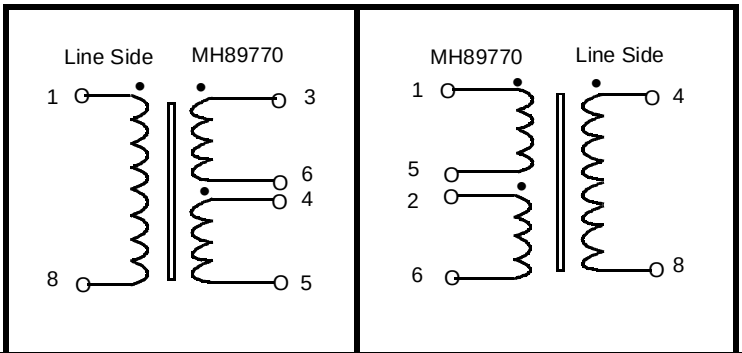


Figure 10 - Typical ESF Configuration



Parameter	Input Transformer	Output Transformer	Units
Line Impedance	100	100	Ω
Inductance	(1-8) >2.2	(4-8) 0.46	mH
Turns Ratio	(1-8):(3-6) 1:1 (1-8):(4-5) 1:1	(1-5):(4-8) 1.89:1 (2-6):(4-8) 1.89:1	
Isolation	1500	1500	V(rms)

Figure 11 - Typical Parameters of the Input and Output Transformers

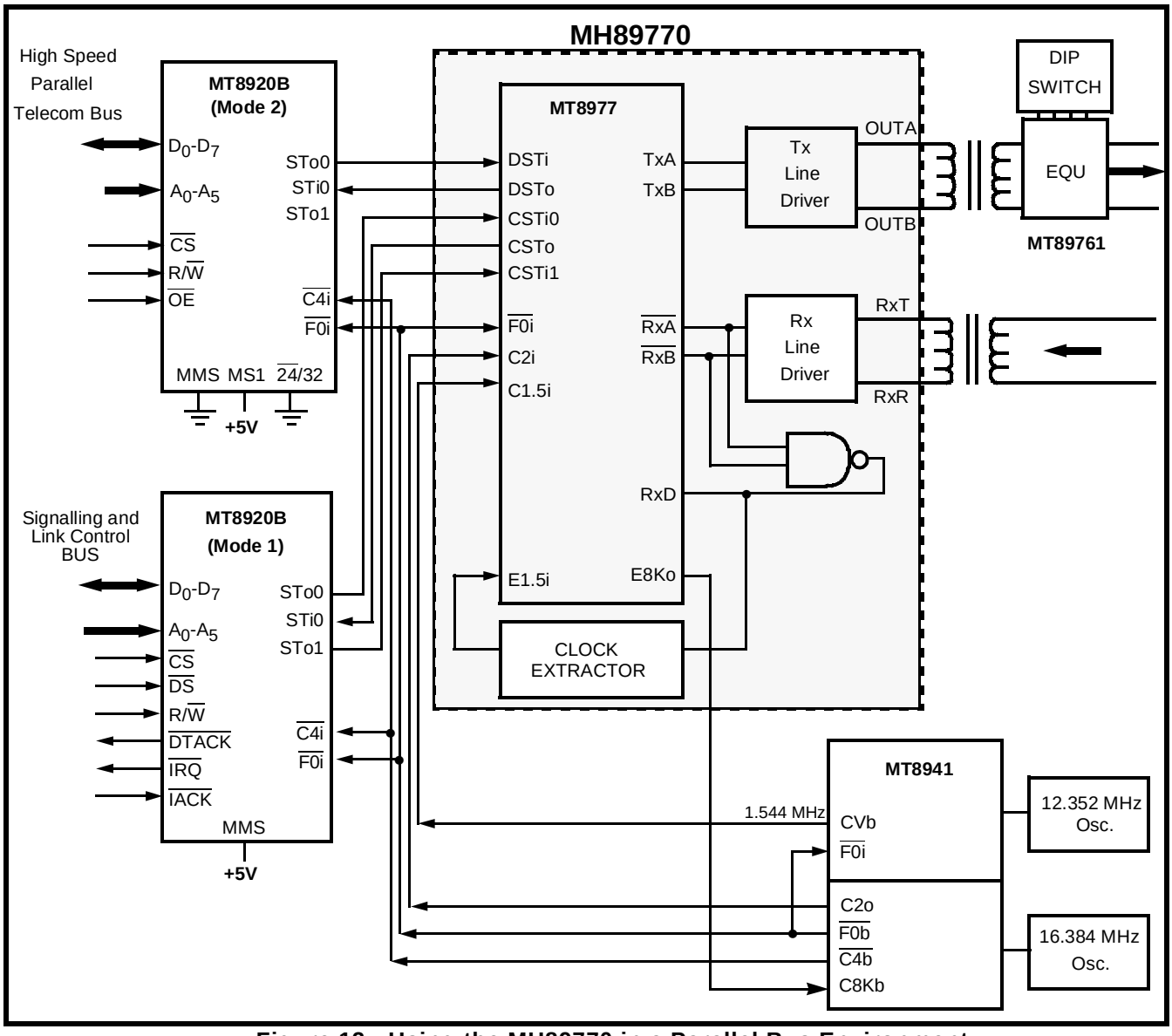


Figure 12 - Using the MH89770 in a Parallel Bus Environment

MT8976. The signals are combined to produce a composite return to zero signal which is clocked into the MT8976 at RxD.

2. Interfacing the MH89770 to a Parallel Bus

The MH89770 can be interfaced to a high speed parallel bus or to a microprocessor using MT8920B Parallel Access Circuit (STPA). Fig. 12 shows the MT8977 interfaced to a parallel bus structure using two STPA's operating in modes 1 and 2.

The first STPA operating in mode 2 (MMS=0, MS1=1, 24/32=0), routes data and/or voice information between the parallel telecom bus and the T1 or CEPT link via DSTi and DSTo. The second STPA, operating in mode 1 (MMS=1) provides access from the signalling and link control bus to the MH89770 status and control channels. All signalling and link functions may be controlled easily through the STPA transmit RAM's Tx0, Tx1, while status information is read at receive RAM Rx0. In addition, interrupts can be set up to notify the system in case of slips, loss of sync, alarms, violations, etc.

3. PCM/Voice Channel Bank

The D3/D4 channel bank is one of the most widely used pieces of equipment in the North American network today. The D3/D4 channel converts 24 analog telephone lines into the 24 channels of a T1 serial stream. The channel bank is the interface point between a digital switching or transmission system and the analog telephone loop. The industry is moving towards end-to-end digital connections (ISDN), but the analog channel bank will still be in use for many years to come.

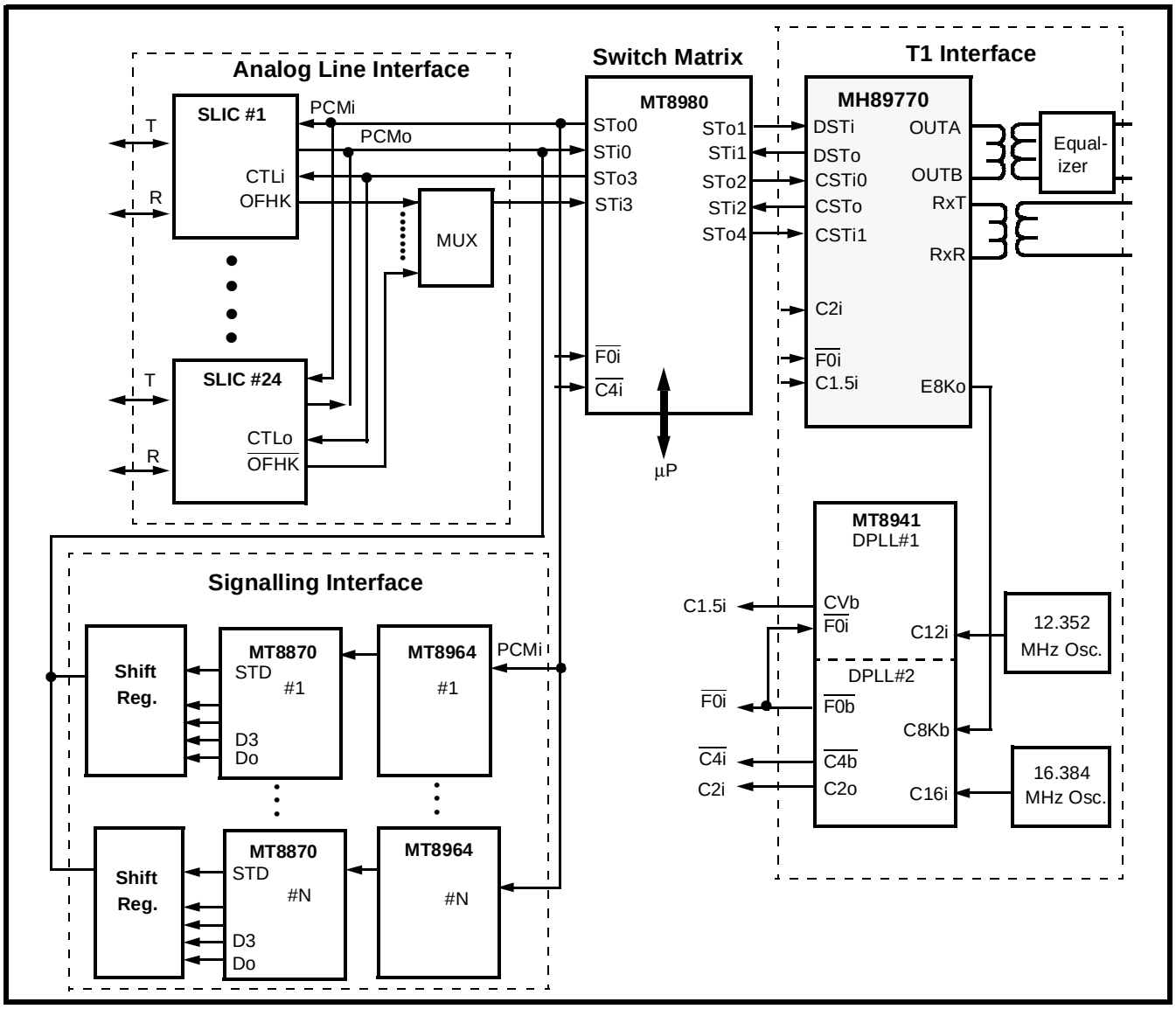


Figure 13 - PCM/Voice Data Channel Bank

Figure 13 shows a block diagram of a channel bank that has been divided into four sections, the analog line interface, signalling interface, switch matrix, and T1 interface. The subscriber line interface circuit (SLIC) provides interface to the telephone line, i.e., provides loop current and ringing voltage, and converts the analog voice signal into µ-Law PCM. The SLIC also detects the off-hook condition for conventional POTS (Plain Old Telephone Set) signalling.

Once the voice is encoded into digital format the switch matrix transfers the 24 consecutive channels that are received from the SLICs to the 24 valid channels used by the MH89770. The MH89770 formats and transmits this information on the T1 line.

Signalling information from the telephone sets can be routed straight through to the output T1 channel, or it can be routed to the DTMF receiver pool. This is easily accomplished by the MT8980 switch matrix once the SLIC has digitized the analog signal.

Channel banks must be able to operate in a loop timed mode so that they meet the clock synchronization requirements of a level four entity. Phase-locked loop #2 of the MT8941 generates the ST-BUS clocks that are synchronized to the extracted 8kHz clock, and phase-locked loop #1 generates the transmit T1 clock synchronized to the ST-BUS.

4. ISDN Voice/Data Channel Bank/Concentrator

The ISDN channel bank is a term that is used in this context to describe a system that performs the same logical function as the D3/D4 channel bank. That is, it concentrates the subscribers digital loop into the primary digital transmission scheme, the T1 trunk.

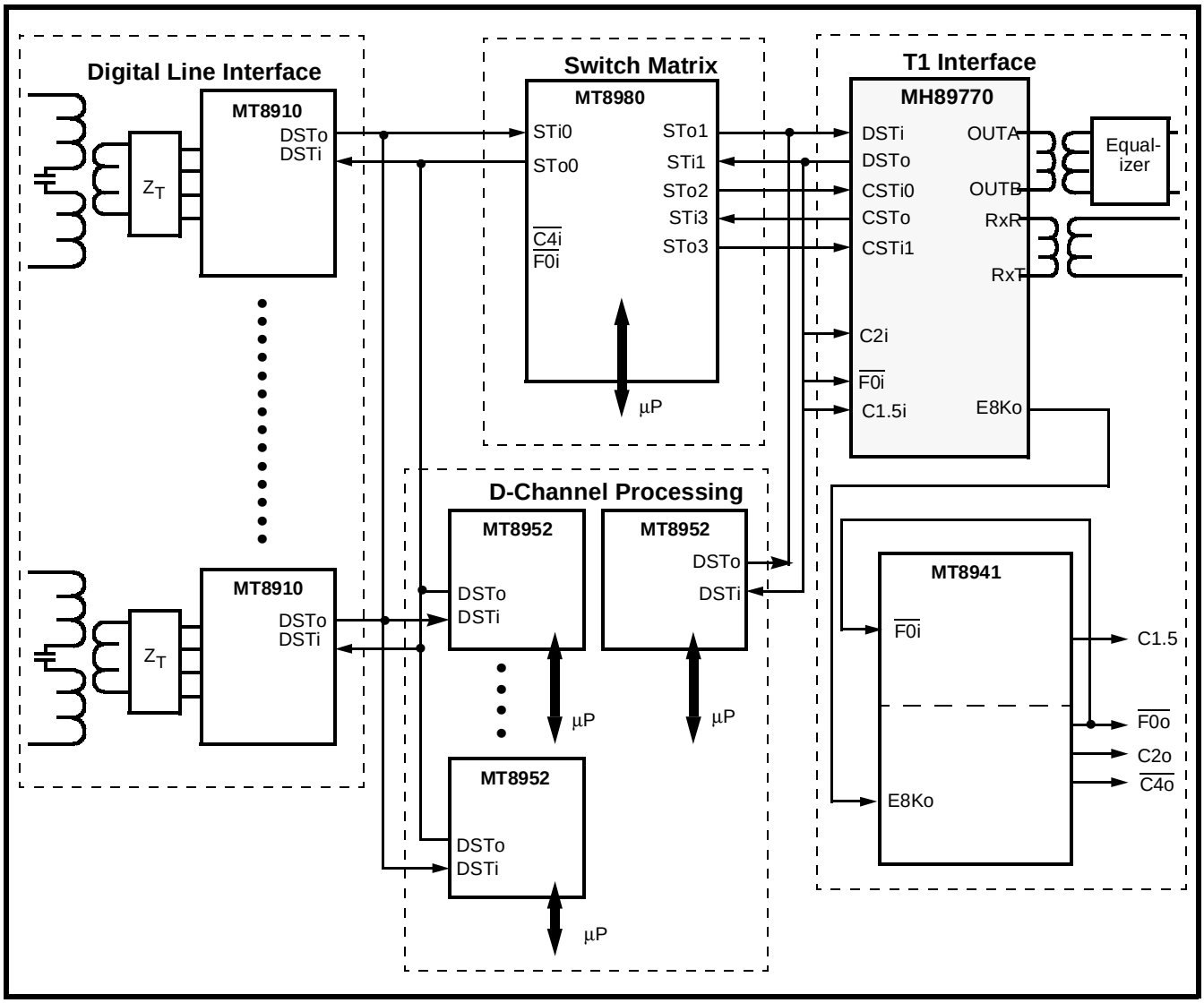


Figure 14 - ISDN Voice Data Channel Bank

The ISDN channel bank in Figure 14 is divided into four blocks, the digital line interface, the switch matrix, the D channel processing, and the T1 interface. Beginning with the digital line interface, the MT8910 provides 2B+D 160k bit bidirectional communication over single twisted pair wiring. The MT8910 converts the 160kbit line signal into ST-Bus format, where it can be manipulated by the MT8980 switch matrix. The data received from the MT8910 is then transferred to the D channel processor by the switch matrix. The D channel processor converts the 2B+D format used on the 160 kBit digital line into the 23B+D format used on the T1 Link.

To control and monitor the MT8910s and the T1 interface the switch matrix operates some of its input and output streams in message mode. This enables the system to control all of the functions of the MT8910s and the T1 interface through the Control ST-BUS points, (CSTi/o).

Clock synchronization is done by the MT8941. Phase-locked loop # 2 generates ST-BUS clocks that are synchronized to the extracted 8kHz output from the T1 interface. Phase-locked loop #1 generates the transmit T1 clock synchronized to the ST-BUS clocks, which are synchronized to the extracted T1 clock. This scheme will also allow the system to operate in a loop timed mode.

With appropriate multiplexing a single D channel processor can handle all 23 2B+D interfaces. If both B channels on all 24 lines are going to be used then it would be necessary to use two T1 trunk interfaces.

5. Digital Access Cross Connect System (DACS)

The Digital Access Cross Connect System (DACS) is a T1 switch with 127 T1 lines as input and output plus one T1 line that is reserved for test and maintenance purposes. A DACS is capable of switching any input channel on any T1 trunk to any output channel on any T1 trunk.

There are four main blocks in Figure 15, the T1 interfaces, the switch matrix, the control matrix, and the clock generator. The digital trunk interface is made up of the MH89770 plus the additional components required to interface to the transmission line. The MH89770 handles all of the required transmit and receive data formatting, and converts the 1.544 MHz serial stream into ST-BUS format so that it can be routed through the MT8980 synchronous switch matrix.

The switch matrix can be built so that the maximum throughput delay is 1 frame +2 channels. The switch matrix will not only route data channels to their destination, but it will also route the received signalling bits through to the destination channel. This is necessary because the receiving MH89770 decodes the T1 stream, and the transmitting MH89770 has to reconstruct the outgoing T1 stream. In other words, there is no multiframe integrity between received data and transmitted data. The total throughput delay is one frame plus ten ST-BUS channels for the MH89770 receiver, 2.5 ST-BUS channels for the MH89770 transmitter, and one frame plus two ST-BUS channels for the switch matrix for a total of 2.5 frames worst case.

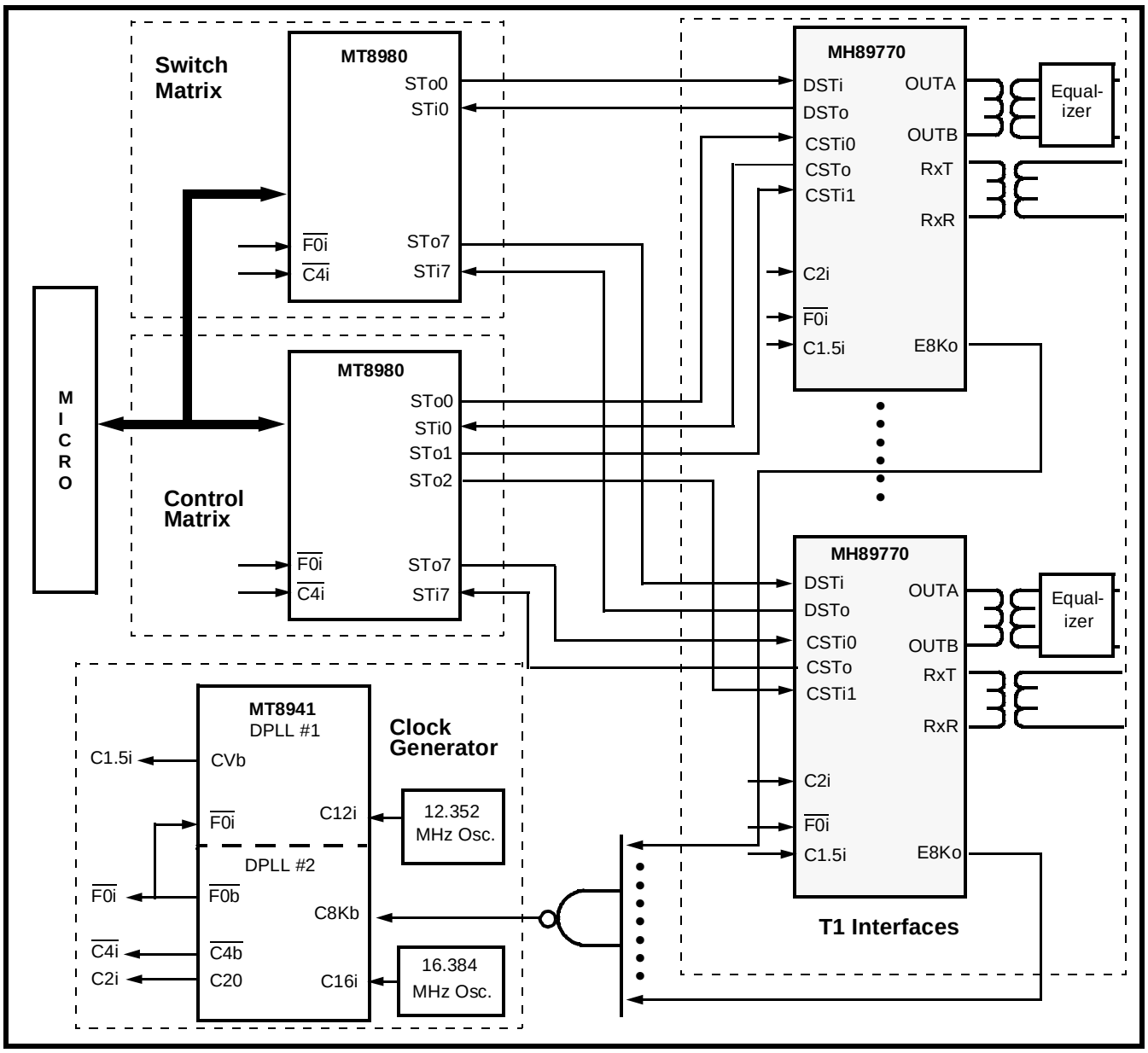


Figure 15 - Digital Access Cross Connect System (DACS)

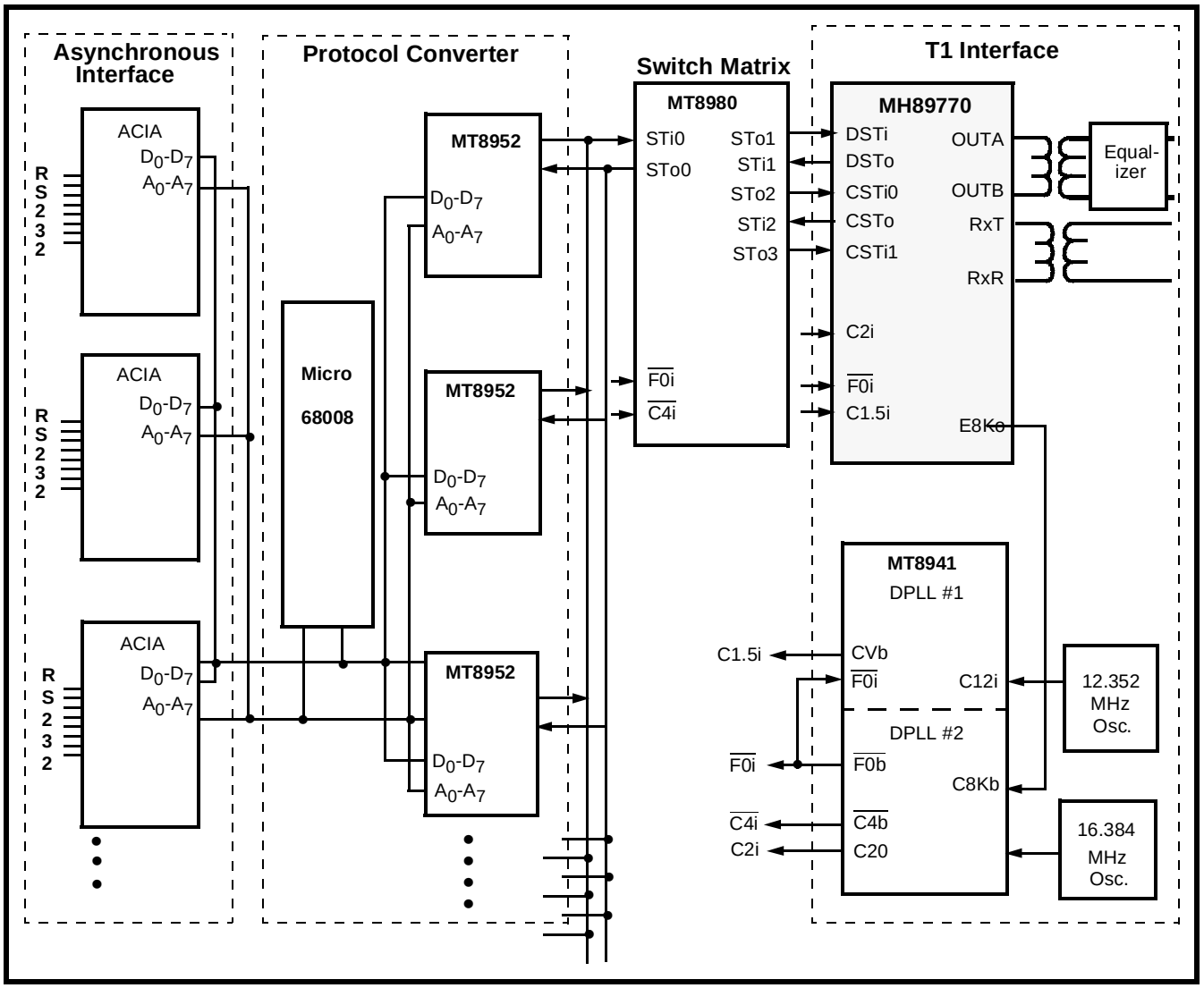


Figure 16 - Digital Multiplex Interface (DMI)

The control block only interfaces with the switch matrix. Besides routing channels and signalling through to the proper destination, the switch matrix must also supply the Master Control Words, and monitor the Master Status Words for each MH89770.

The clock generation block supplies the ST-BUS clocks and the T1 transmit clocks that are synchronized to one of the T1 trunks. All of the extracted 8 kHz outputs are NANDed together before they are input to PLL #2 of the MT8941.

Phase-locked Loop #2 of the MT8941, will generate ST-BUS clock signals for the MH89770s and the MT8980s that are synchronized with the chosen T1 line. The E8Ko of all of the other MH89770s can be tristated from the Master Control Word, which allows the system controller to select any one of 128 T1 lines to act as the synchronization source. By connecting the frame pulse output, $\overline{F0o}$, of PLL #2 to $\overline{F0i}$ of PLL # 1, the MT8941 will generate the T1 transmit clock that is phase-locked to $\overline{F0o}$, which in turn is phase-locked to the master synchronization signal, E8Ko. If all of the T1 trunks are from the network any short term differences in the received data rate will be absorbed by the elastic buffer in the MH89770.

6. Digital Multiplex Interface (DMI)

Figure 16 illustrates an implementation of the Digital Multiplex Interface (DMI) specification, which defines a computer to PBX interface. This interface can convert 300 baud to 64 kbaud asynchronous or synchronous data channels to T1 format with clear channel capabilities and common channel signalling.

Figure 16 is broken down into four functional blocks which are the asynchronous interface (ACIAs), the protocol converter (micro and MT8952s), the switch matrix (MT8980), and the T1 interface (MH89770).

The Asynchronous Communications Interface Adapters (ACIA) provide a standard RS232 interface that is compatible with many off-the-shelf modems and data sets. A single microprocessor is capable of handling the protocol conversion between the RS232 ports and the MT8952 HDLC protocol controller.

The MT8952 interfaces directly to the ST-BUS, which in turn interfaces directly to the T1 interface devices. Instead of the MT8952 operating at 64 kbit/s continuously, it operates at 2.048 Mbit/s and inputs/outputs an 8 bit burst every 125 µsec. This feature eliminates the need for an additional rate conversion circuit to multiplex the HDLC outputs up to the T1 data rate. Each of the HDLC chips is assigned a timeslot on the ST-BUS in a manner that is similar to enabling a voice codec. When the MT8952 is not enabled the output driver is tristated.

The channel assignment circuit is therefore very simple. The switch matrix, in the message mode, passes monitor and control information between the microprocessor and the T1 interface over ST-BUS stream 0. The MT8980 is also used to reformat the ST-BUS data streams between the protocol converter and the MH89770 interface.

The MH89770 and the MT8941 form the T1 interface. The MH89770 converts the data received on the ST-BUS into a 1.544 MHz T1 stream. All of the formatting and decoding of the T1 signal is performed by this device. The MT8941 provides the clock synchronization required to operate in a loop timed mode. Digital phase-locked loop #2 provides ST-BUS clocks that are synchronized to the extracted 8kHz, and digital phase-locked loop #1 provides the transmit 1.544 MHz clock synchronized to the ST-BUS.

7. High Speed Data Transmission Link

High speed data links are becoming increasingly popular in private networks and computer communications. The basic mode of transmission is to assemble data into packets (e.g., HDLC or ethernet) which are transported on a T1 link configured as a 1.536 Mbit/s serial channel. No T1 repeaters are required if the transmission link length is 1300 ft. or less (e.g., business complex or university). However, if the transmission link length is greater than 1300 ft., a repeatered T1 line must be leased from the local telephone operating company.

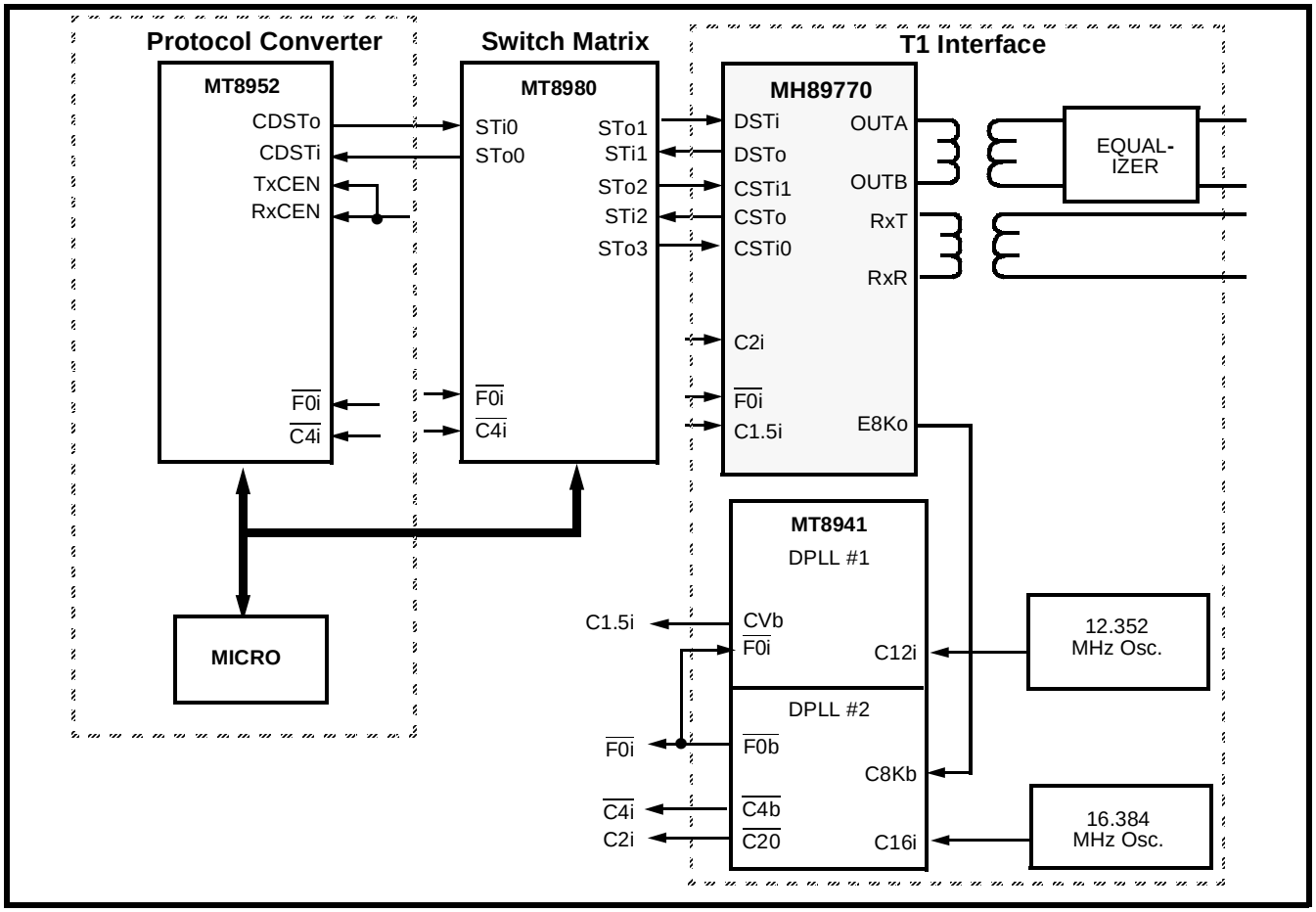


Figure 17 - High Speed Data Transmission Link

Figure 17 is divided into three functional blocks which are the protocol converter, switch matrix, and T1 interface. The protocol section is dependent on the particular format that is chosen. In this example it is assumed that the protocol is HDLC. The Transmit Clock Enable ($\overline{\text{TxCEN}}$) and the Receive Clock Enable ($\overline{\text{RxCEN}}$) of the MT8952 are active for a period of 24 consecutive ST-BUS channels, and the clock speed is 2.048 MHz. This enables the protocol conversion section to interface directly to the switch matrix. The switch matrix switches the first 24 channels received from the protocol section into the 24 valid timeslots used by the MH89770. Once the data enters the T1 interface the MH89770 formats and transmits the data on the T1 line.

Control and monitoring of the T1 interface is done through the MT8980 switch matrix. CSTi0 and CSTo1 are connected to the ST-BUS streams that are configured for message mode so the controlling microprocessor can access the Master Control Words and the Master Status Words.

The received portion of the T1 interface extracts the data from the T1 stream and formats it into ST-BUS channels. The MT8980 switches these ST-BUS channels into the first 24 consecutive channels of an ST-BUS stream, which is passed to the protocol conversion block. HDLC packets are disassembled from the incoming ST-BUS stream by the MT8952.

Clock generation and synchronization are handled by the MT8941. DPLL #2 generates ST-BUS clocks that are phase-locked to the extracted 8KHz, and DPLL #1 generates the transmit T1 clock that is phase-locked to the ST-BUS frame pulse. Therefore, the interface is operating in a loop timed mode and there will be no loss of information due to slips. The MT8941 can also be configured to operate in a master timing mode.

8. T1 to CEPT Digital Trunk Converter

The two main digital trunk transmission formats in use today are T1 and CEPT. Mitel's T1 and CEPT interfaces convert the digital trunk format into ST-BUS format. The common element between the two systems is the ST-BUS. Therefore, a T1 to CEPT digital trunk converter can be realized.

Figure 18 shows five blocks which are the T1 interface, switch matrix, CEPT interface, clock generation and synchronization, and DSP Element. The T1 interface converts the 1.544 MHz serial stream into the ST-BUS format which interfaces to the switch matrix through DSTi and DSTo. The CEPT interface converts the 2.048 MHz serial stream into the ST-BUS format and interfaces to the switch matrix through the DSP element.

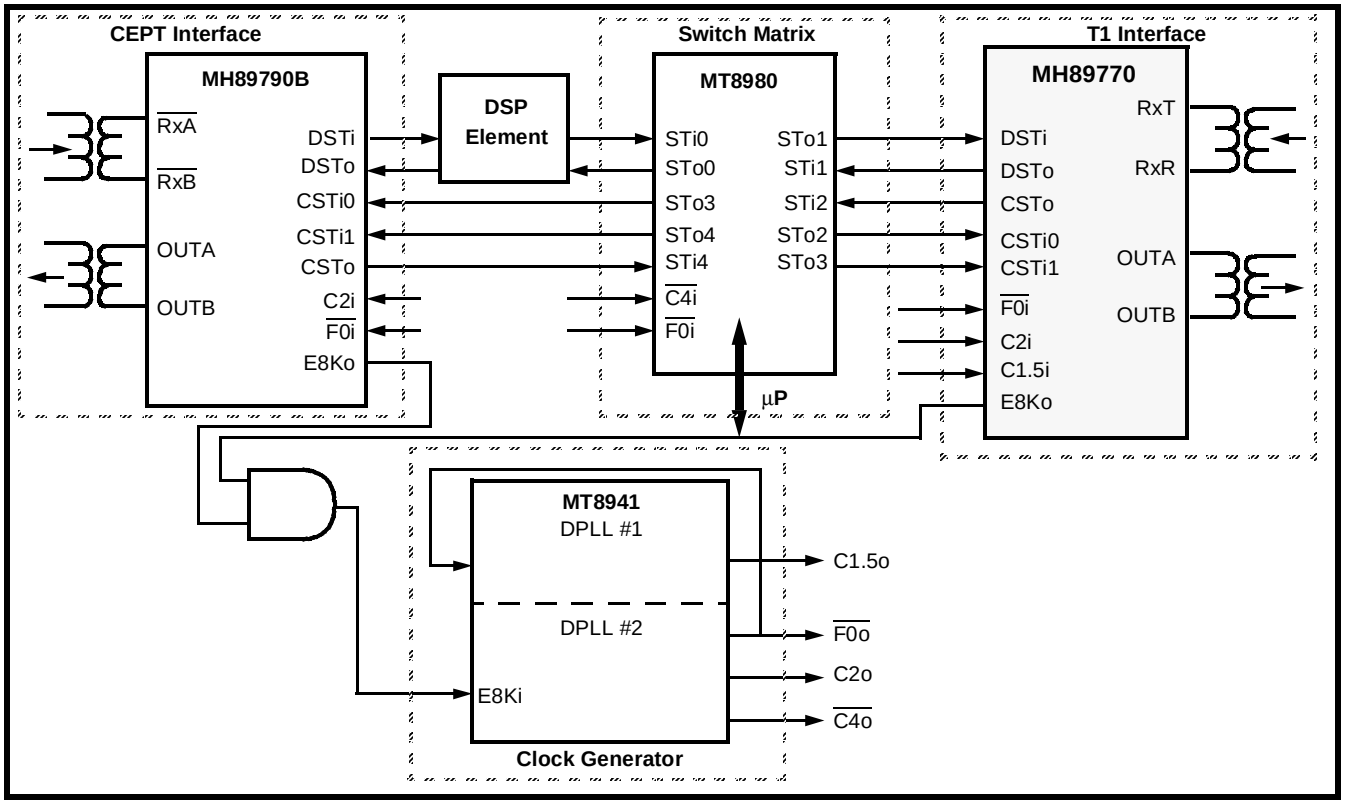


Figure 18 - T1 to CEPT Digital Trunk Converter

With both the T1 data and the CEPT data converted to the ST-BUS format, the two digital trunks can exchange information through the switch matrix. Unfortunately, the signalling information from the two formats is not exchanged as easily. The T1 A and B signalling bits must be read by the controlling microprocessor and converted in software to the CEPT ABCD signalling bits, and vice versa. The circuit must also convert all the channels carrying voice data to the appropriate encoding scheme, (i.e., T1 μ-Law or CEPT A-Law). This is done by the block labelled DSP in Figure 18, Digital Signal Processor.

The final component of the system is the MT8941. The extracted 8 kHz outputs from the T1 and the CEPT interfaces are combined with an AND gate before being connected to the MT8941. One of the interfaces is selected as the synchronization source by enabling its output through the Master Control Word of the chosen interface. Phase-locked loop #2 will then generate ST-BUS clocks that are synchronized to either the T1 network or the CEPT network. Phase-locked loop #1 is configured to generate the T1 transmit clock synchronized to the ST-BUS. Therefore, if the ST-BUS is synchronized to one network then the elastic buffer in the opposite interfaces will perform controlled slips between that network and the T1 to CEPT converter.

Magnetics Information

For supporting initial design activities, Mitel Semiconductor has available the MH89770 Magnetic Kit which contains the magnetics shown in Figure 11. Alternatively, they are available directly from the following manufacturer:

Filtran Ltd.
229 Colonnade Road
Nepean, Ontario
Canada K2E 7K3
Telephone: (613) 226-1626

Please refer to Figure 6 for the transformer part numbers.

Packaging

The MH89770 is available in two package options which are:

- The MH89770S which is a surface mountable version of the MH89770N is suitable for Infrared Reflow (I.R.) soldering. See Figure 35 for the dimensional drawing, and Figure 36 for the recommended footprint.
- The MH89770N has a row pitch of 0.8”. See Figure 37 for the dimensional drawing for this part.

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage with respect to V_{SS}	V_{DD}	-0.3	7	V
2	Voltage on any pin other than supplies, OUTA or OUTB		V_{SS}-0.3	V_{DD}+0.3	V
3	Voltage on OUTA or OUTB			15	V
4	Current at any pin other than supplies, OUTA or OUTB			20	mA
5	Current at OUTA or OUTB			200	mW
6	Storage Temperature	T_{ST}	-20	85	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Operating Temperature	T_{OP}	0		70	°C	
2		Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
3		Input High Voltage	V_{IH}	2.4		V_{DD}	V	Digital Inputs
			V_{IH}		3.0		V	Line Inputs
4		Input Low Voltage	V_{IH}	V_{SS}		0.4	V	Digital Inputs
			V_{IL}		0.3		V	Line Inputs

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges.

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Supply Current	I_{DD}		12	25	mA	Outputs Unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital Inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital Inputs
4		Input Leakage Current	I_{IL}		±1	±10	µA	Digital Inputs V_{IN}=0 to V_{DD}
5	Outputs	Output High Current	I_{OH}	7	20		mA	Source Current V_{OH}=2.4V
6		Output Low Current	I_{OL}	2	10		mA	Sink Current V_{OL}=0.4V
7		Output Low Voltage OUTA or OUTB	V_{OL}			0.25	V	I_{OL}=10mA
8		Input Impedance RxT to RxR	Z_{IN}		400		Ω	
		RxT or RxR to Gnd			1K		Ω	
9		Schmitt Trigger Input (XSt)	V_{T+}			4.0	V	
			V_{T-}	1.5			V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Capacitance

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figure 19 & 20)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Clock Period	t_{p20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	244	300	ns	t_{P20} = 488 ns
3	Frame Pulse Setup Time	t_{FPS}	50			ns	
4	Frame Pulse Hold Time	t_{FPH}	50			ns	
5	Frame Pulse Width	t_{FPW}	50			ns	
6	$\overline{RxSF}$ Output Delay	t_{FPOD}			125	ns	50pF Load
7	$\overline{TxSF}$ Hold Time	t_{TxSFH}	0.5		124.5	µs	
8	$\overline{TxSF}$ Setup Time	t_{TxSFS}	0.5		124.5	µs	

NB: Frame Pulse is repeated every 125µs in synchronization with the clock.
† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

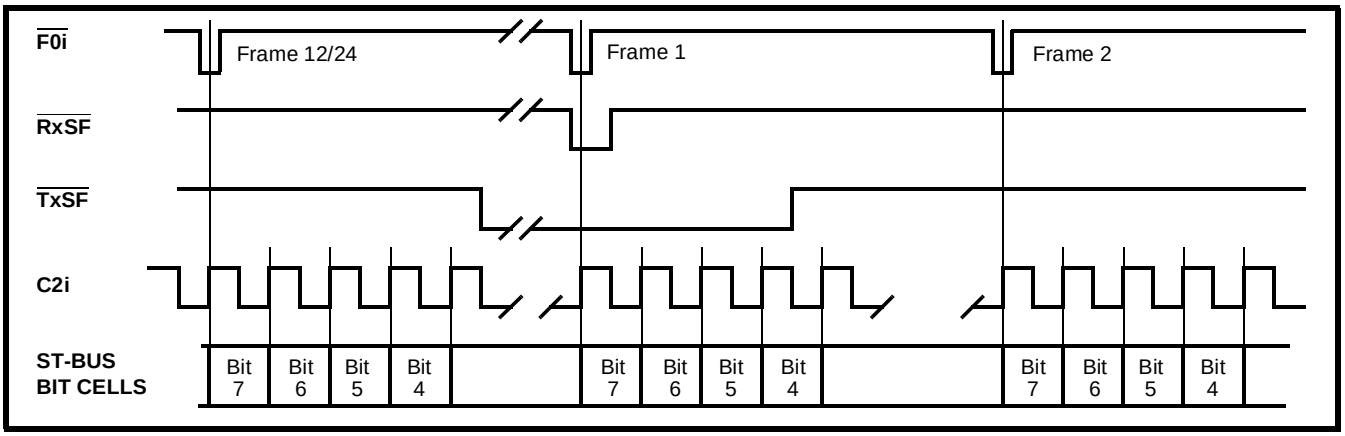


Figure 19 - Clock & Frame Alignment for ST-BUS Streams

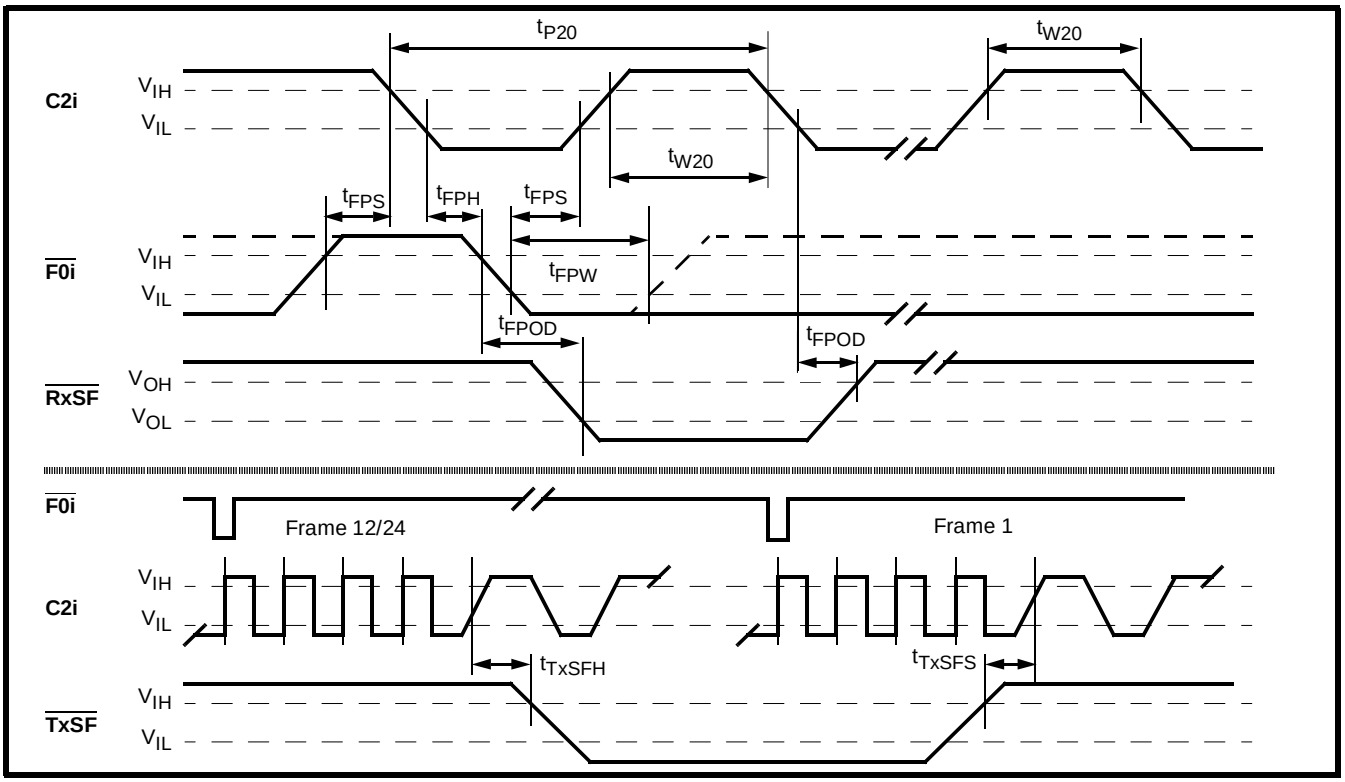


Figure 20 - Clock & Frame Pulse Timing for ST-BUS Streams

AC Electrical Characteristics† - Timing For DS1 Link Bit Cells (Figure 21)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	E1.50 Clock Period	t_{PEC}		648		ns	
2	E1.5o Clock Width High or Low	t_{WEC}		324		ns	
3	E1.5o Clock Rise Time	t_{REC}		60		ns	
4	E1.5o Clock Fall Time	t_{FEC}		20		ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

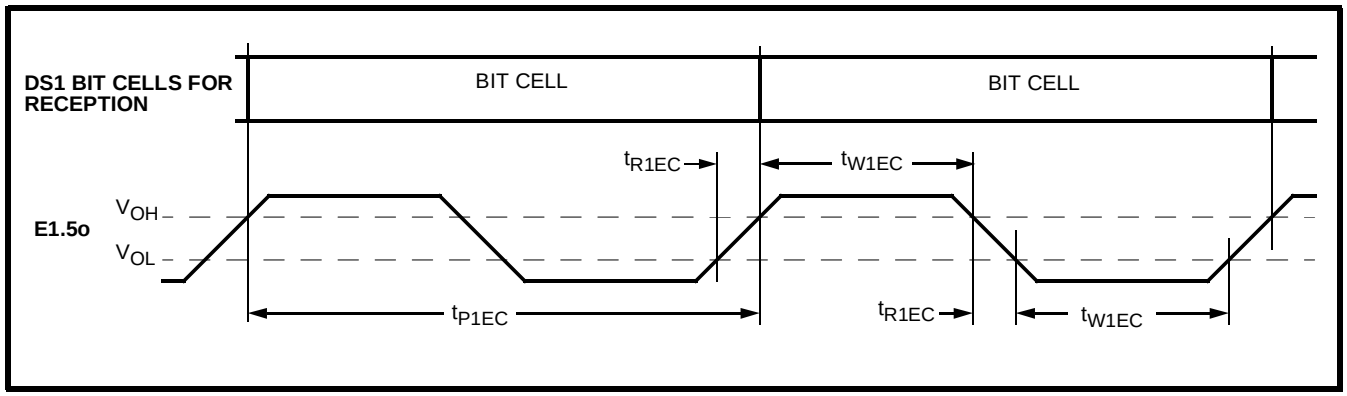


Figure 21 - DS1 Receive Clock Timing

AC Electrical Characteristics† - 2048 kbit/s ST-BUS Streams (Figure 22)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Serial Output Delay	t_{SOD}			125	ns	150pF load
2	Serial Input Setup Time	t_{SIS}	15			ns	
3	Serial Input Hold Time	t_{SIH}	50			ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

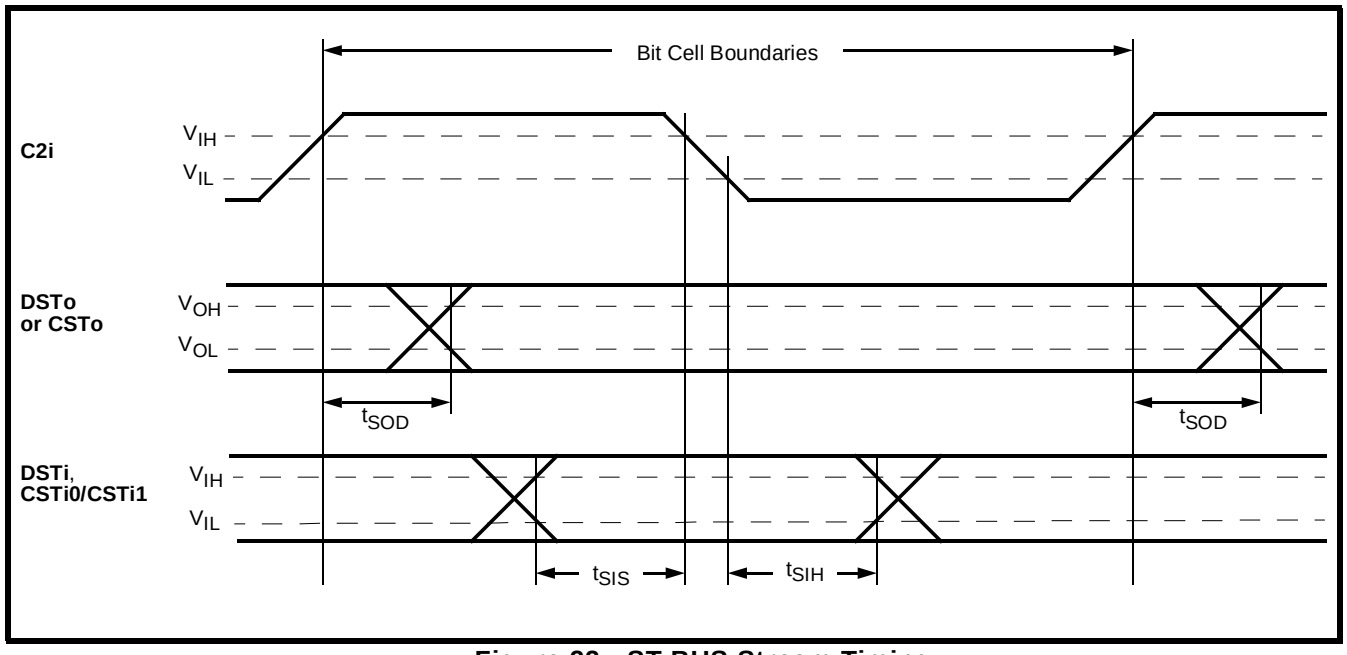


Figure 22 - ST-BUS Stream Timing

AC Electrical Characteristics† - XCTL, XSt, & E8Ko (Figure 23, 24, & 25)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	External Control Delay	t_{XCD}			140	ns	
2	External Status Setup Time	t_{XSS}			100	ns	
3	External Status Hold Time	t_{XSH}			400	ns	
4	8 kHz Output Delay	t_{8OD}			150	ns	
5	8 kHz Output Low Width	t_{8OL}		78		µs	
6	8 kHz Output High Width	t_{8OH}		47		µs	
7	8 kHz Rise Time	t_{8R}			10	ns	
8	8 kHz Fall Time	t_{8F}			10	ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

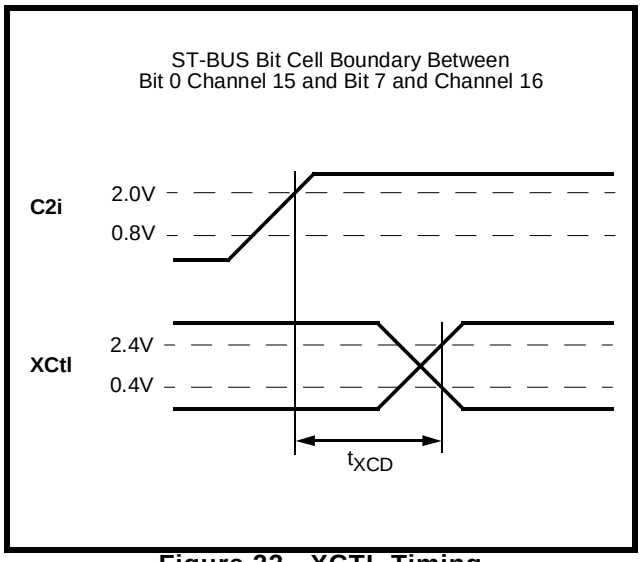


Figure 23 - XCTL Timing

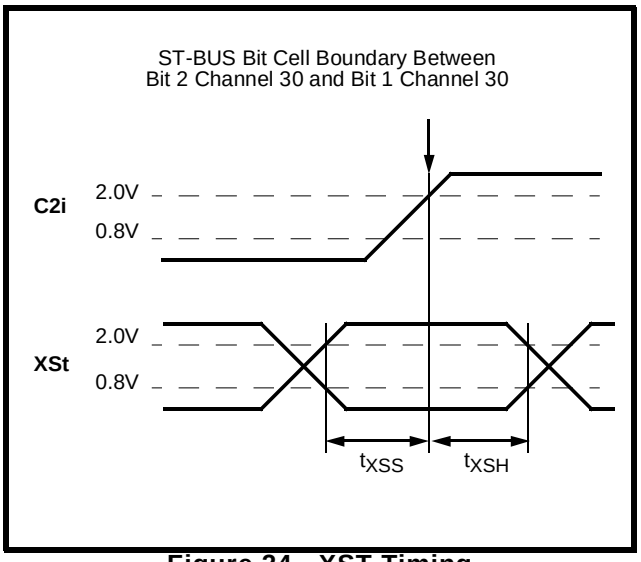


Figure 24 - XST Timing

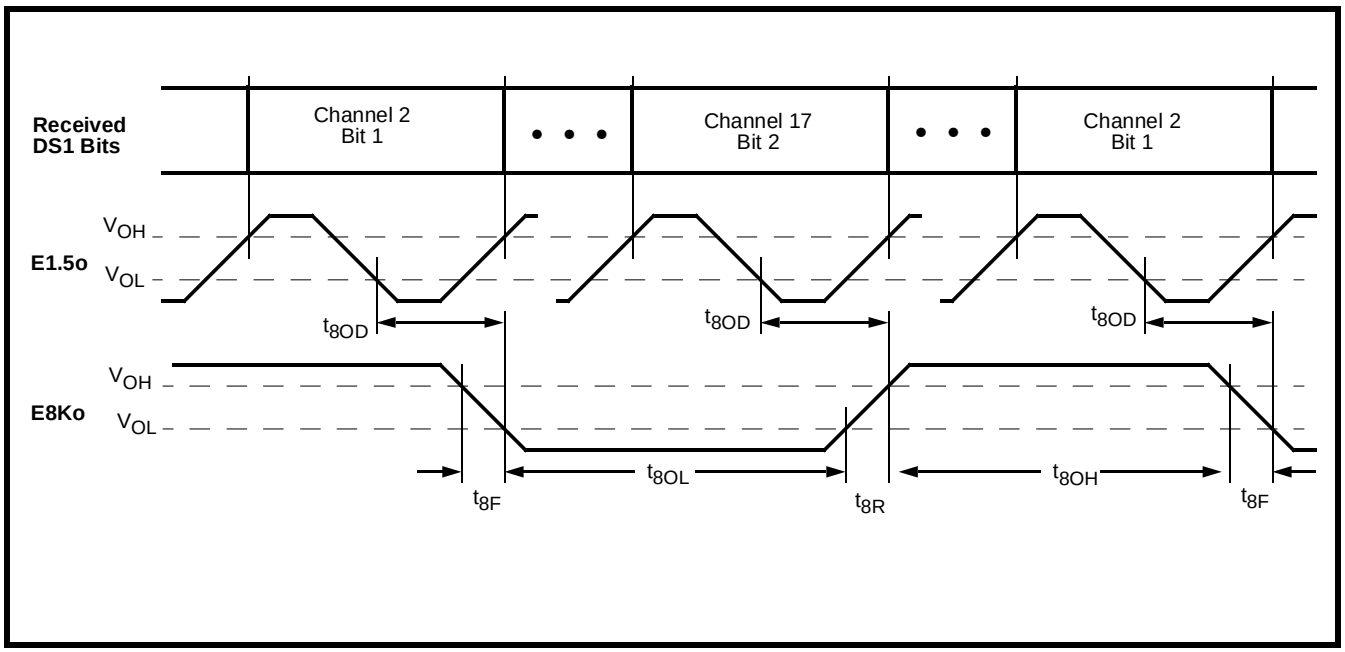


Figure 25 - E8Ko Timing

AC Electrical Characteristics† - DS1 Link Timing (Figures 26 and 27)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay	t_{TSD}	50		150	ns	150pF Load
2	E1.5o Clock Period	t_{PEC}		648		ns	
3	E1.5o Clock Width High or Low	t_{WEC}		324		ns	
4	Receive Data Setup Time	t_{RDS}		50		ns	
5	Receive Data Hold Time	t_{RDH}		50		ns	
6	Receive Data Pulse Width	t_{RDW}		324		ns	
7	Receive Data Fall Time	t_{RDF}		20		ns	
8	Receive Data Rise Time	t_{RDR}		20		ns	
9	C1.5i Period	$t_{PC1.5}$	500	648	800	ns	
10	C1.5i Pulse Width High or Low	$t_{WC1.5}$	250	324		ns	

† Timing is over recommended operating temperature and power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

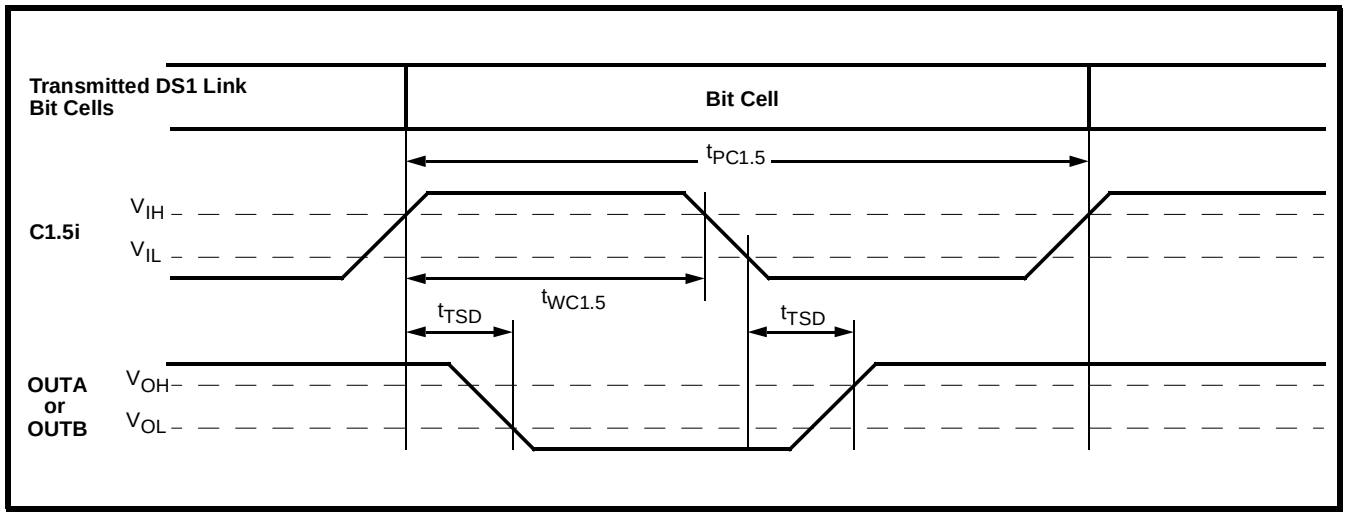


Figure 26 - Transmit Timing for DS1 Link

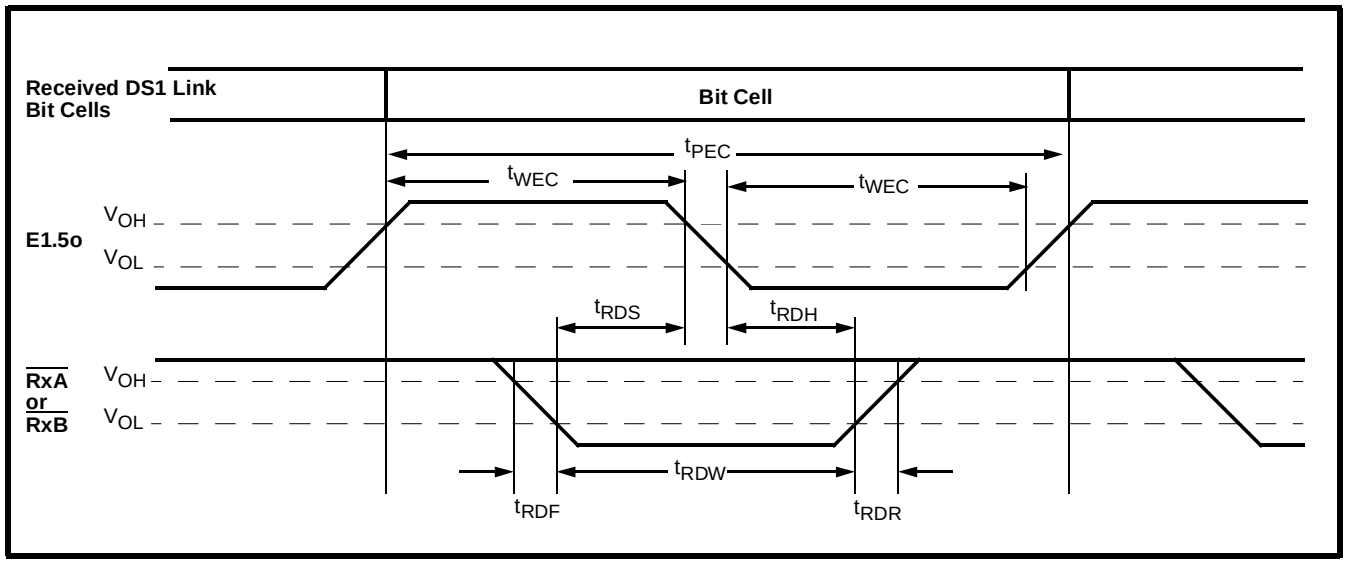


Figure 27 - Receive Timing for DS1 Link

AC Electrical Characteristics† - DS1 Link Timing (Figure 28 & 29)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit FDL Setup Time	t_{DLS}	110			ns	
2	Transmit FDL Hold Time	t_{DLH}	70			ns	
3	Receive FDL Output Delay	t_{DLOD}			0	ns	50pF Load
4	Facility Data Link Clock Delay	t_{FCD}			135	ns	50pF Load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

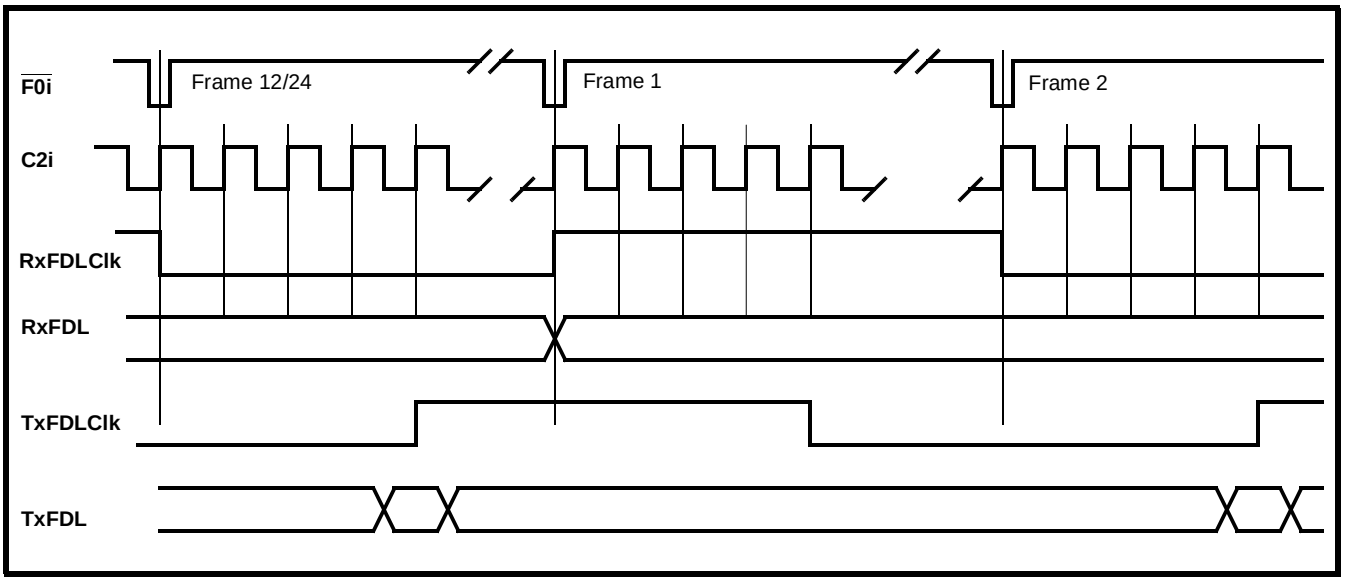


Figure 28 - Clock & Frame Alignment for RxFDL and TxFDL

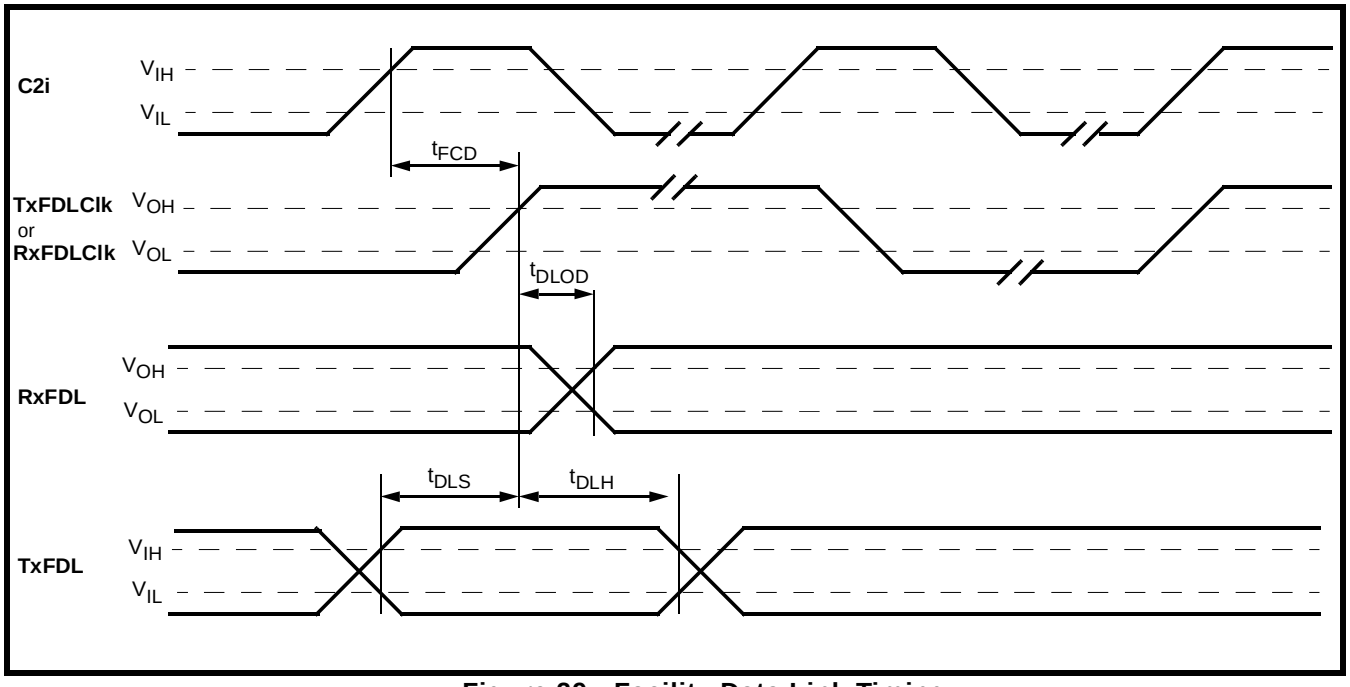


Figure 29 - Facility Data Link Timing

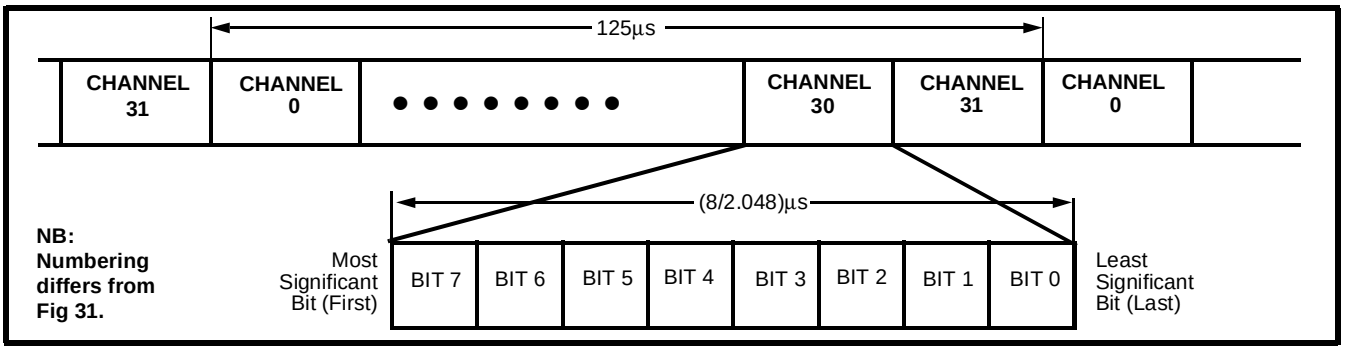


Figure 30 - Format of 2048 kbit/s ST/BUS Streams

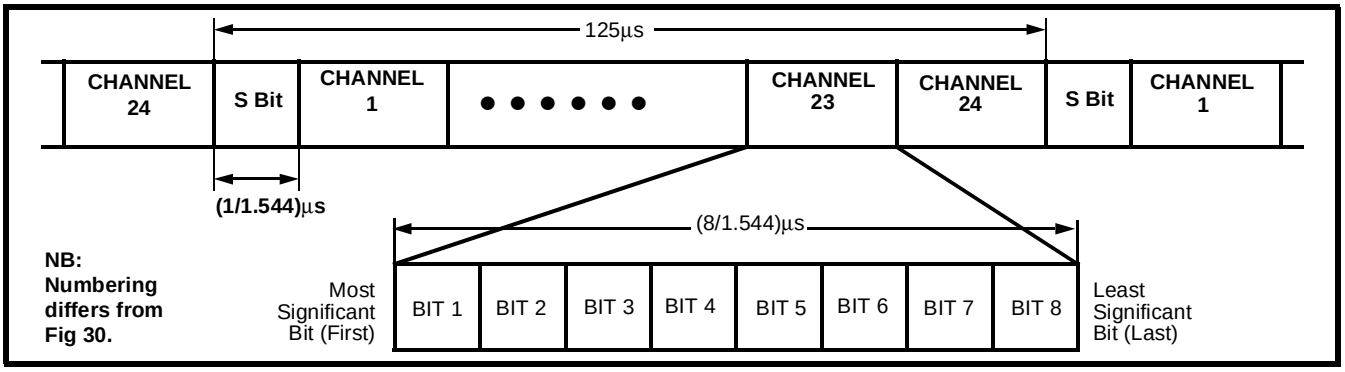


Figure 31 - DS1 Link Frame Format

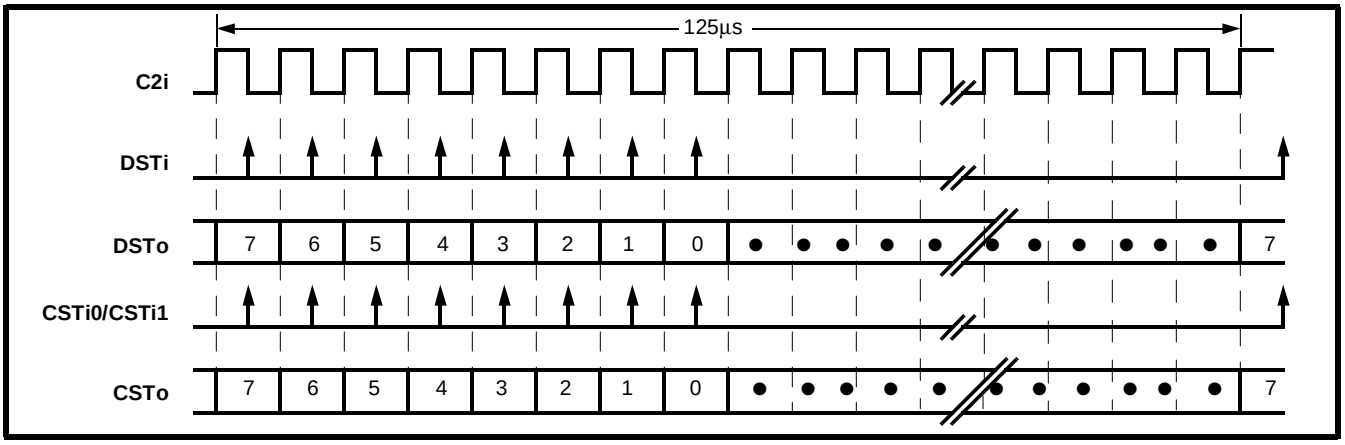


Figure 32 - Functional ST-BUS Timing

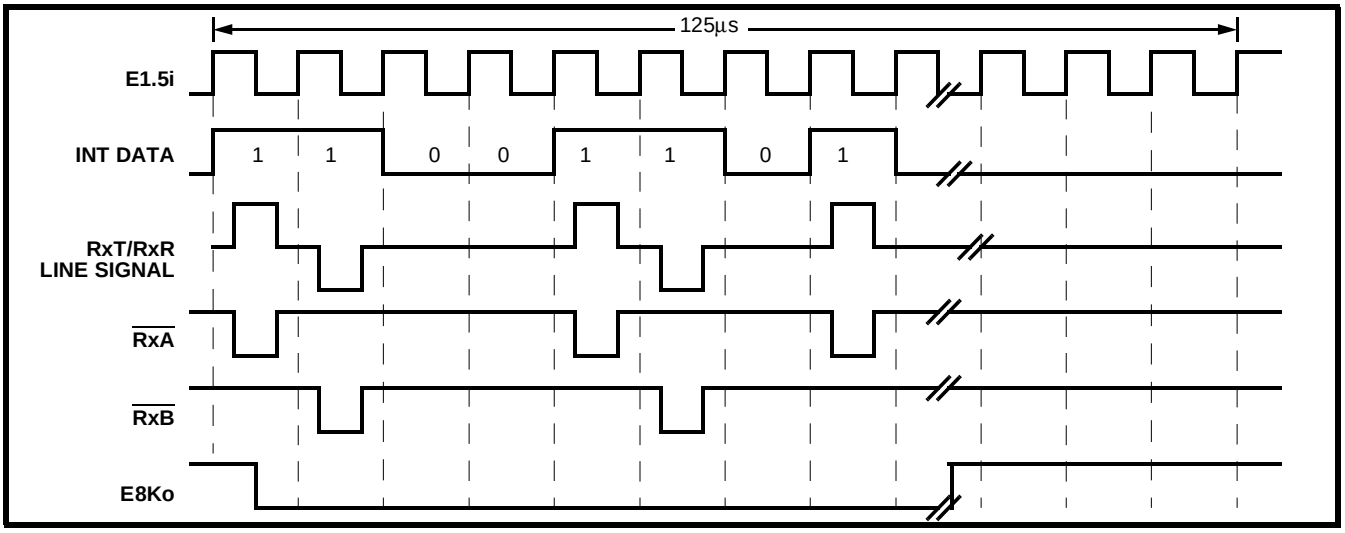


Figure 33 - Functional DS1 Receive Timing

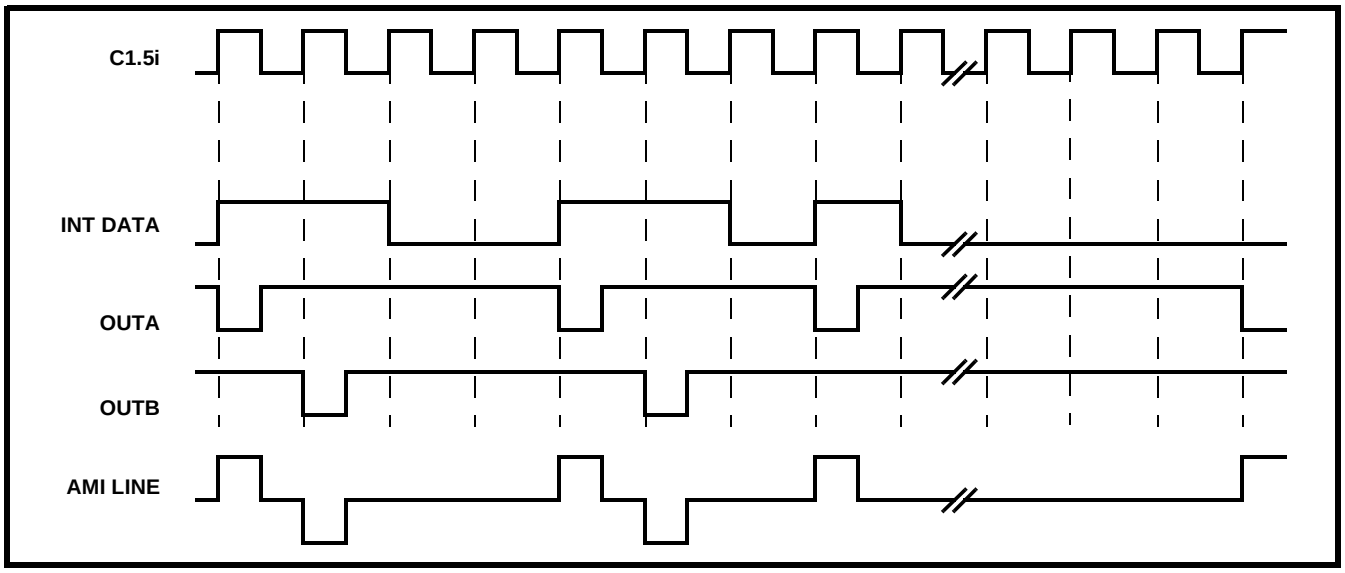
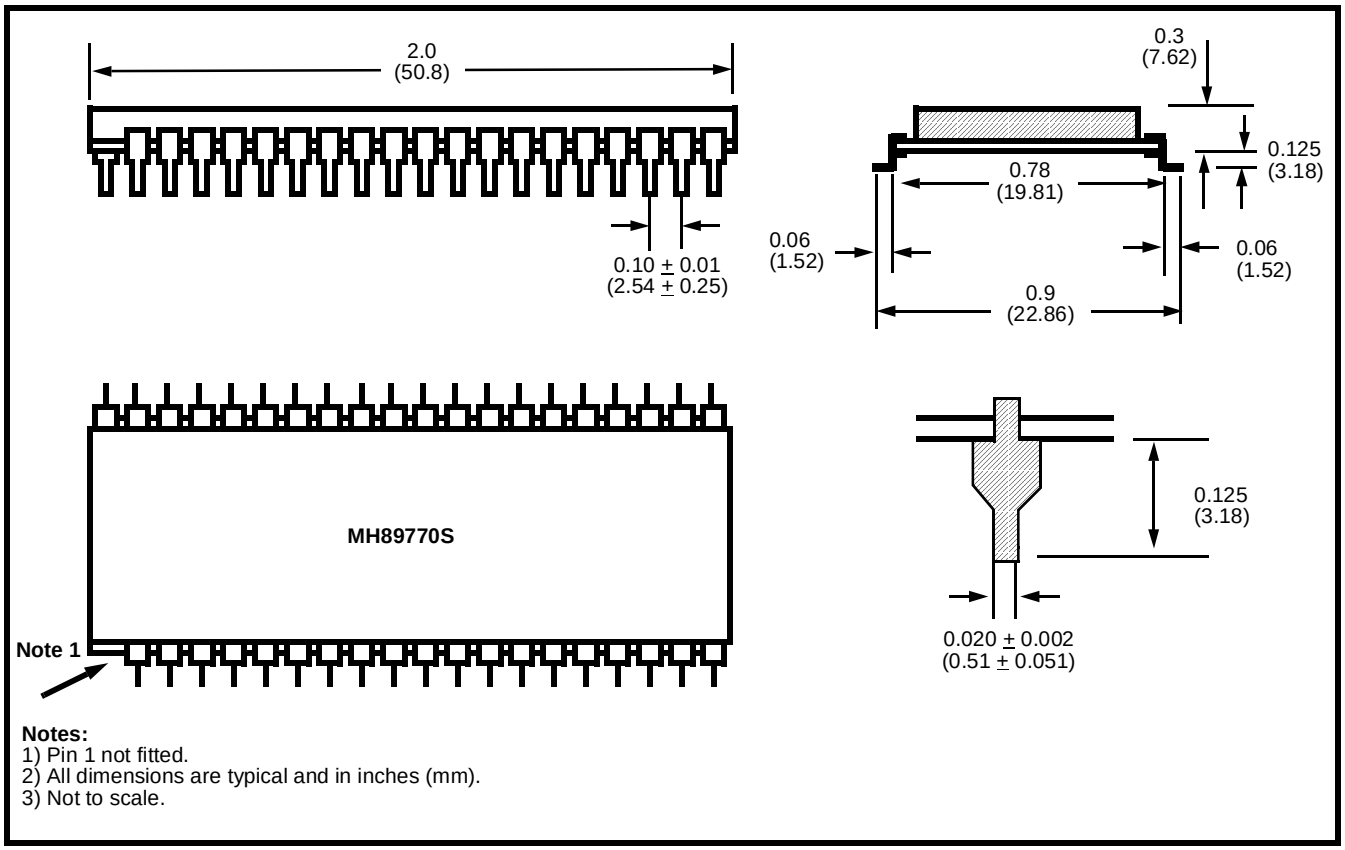


Figure 34 - DS1 Transmit Timing



Notes:
1) Pin 1 not fitted.
2) All dimensions are typical and in inches (mm).
3) Not to scale.

Figure 35 - Physical Dimensions for the 40 Pin Dual in Line S.M.T. Hybrid

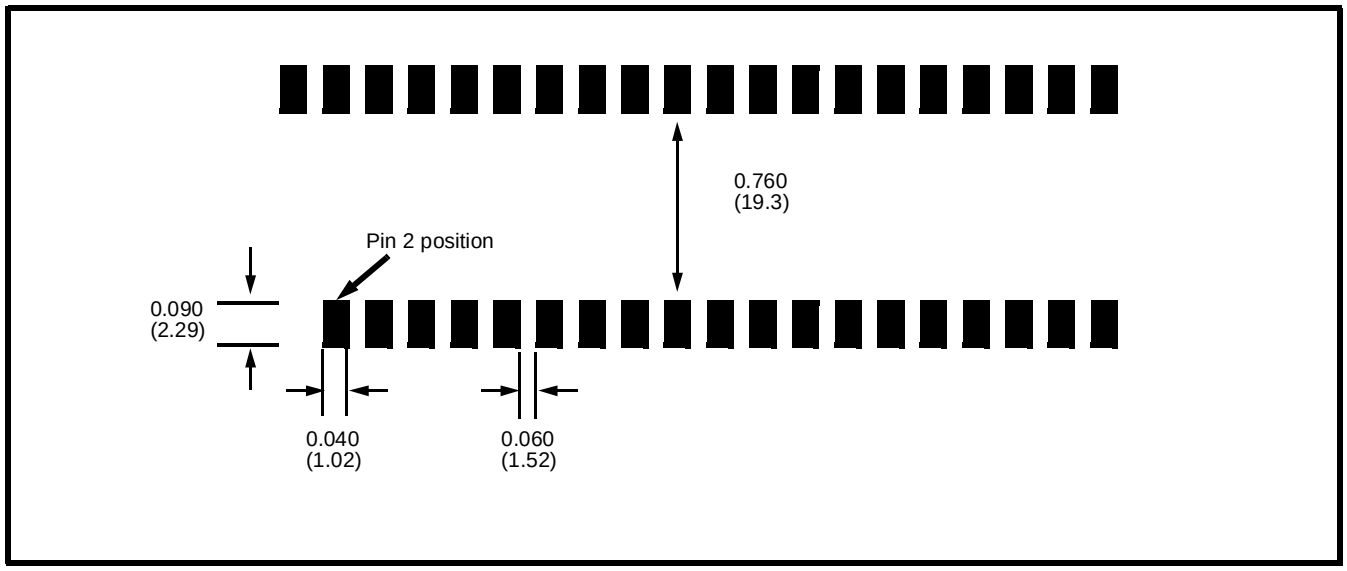
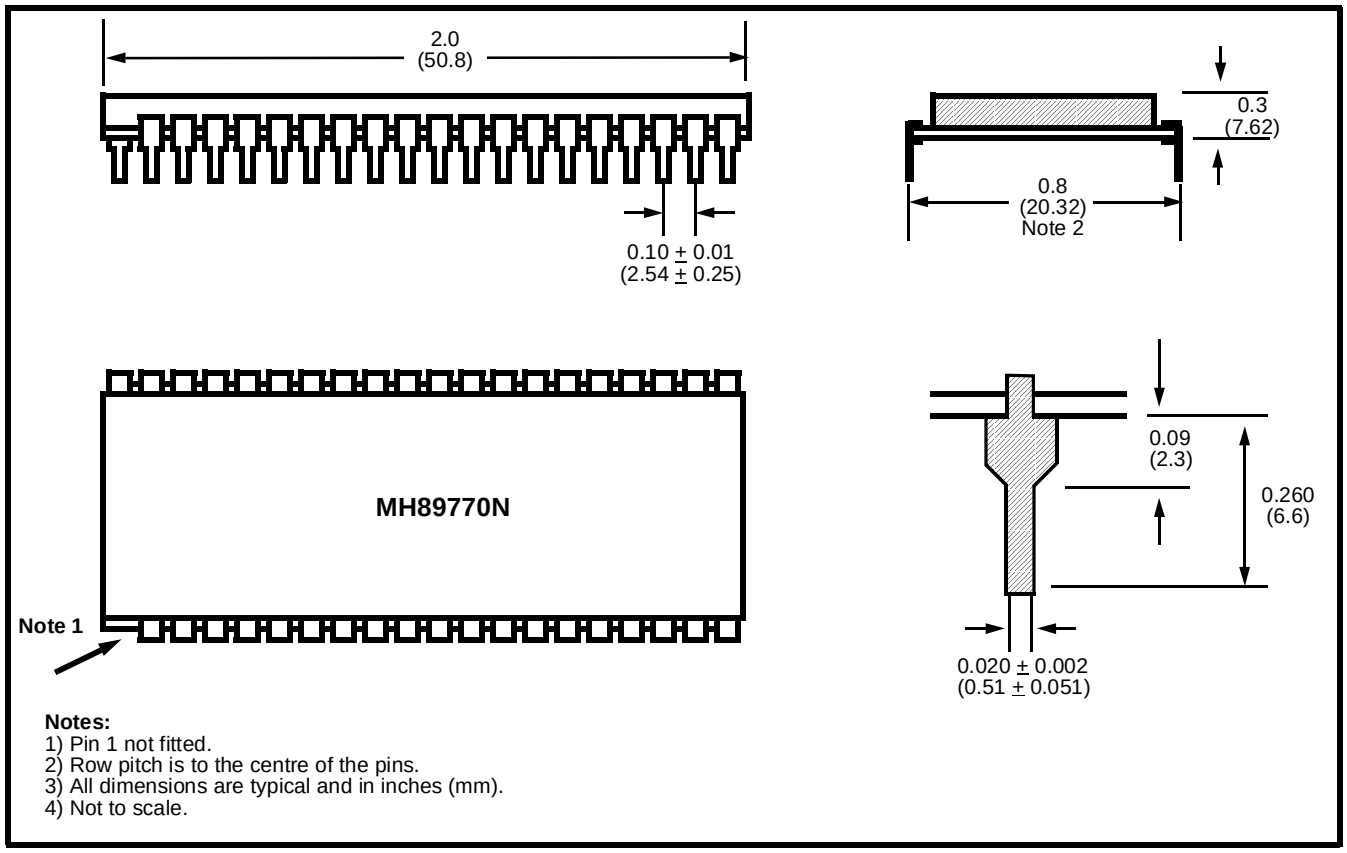


Figure 36 - Recommended Footprint for the 40 Pin Dual in Line S.M.T. Hybrid



Notes:
1) Pin 1 not fitted.
2) Row pitch is to the centre of the pins.
3) All dimensions are typical and in inches (mm).
4) Not to scale.

Figure 37 - Physical Dimensions for the 40 Pin Dual in Line Hybrid 0.8" Row Pitch

Appendix

Control and Status Register Summary

7	6	5	4	3	2	1	0
Debounce 1 Disabled 0 Enabled	**TSPZCS** 1 Disabled 0 Enabled	**B8ZS** 1 B8ZS 0 Jammed Bit	**8KHSel** 1 Disabled 0 Enabled	**XCtl** 1 Set High 0 Cleared	**ESFYLW** 1 Enabled 0 Disabled	**Robbed Bit** 1 Disabled 0 Enabled	**YLALR** 1 Enabled 0 Disabled

Master Control Word 1 (Channel 15, CSTi0)

RMLOOP 1 Enabled 0 Disabled	**DGLOOP** 1 Enabled 0 Disabled	**ALL1's** 1 Enabled 0 Disabled	**ESF/D4** 1 ESF 0 D3/D4	**Reframe** Device Reframes on High to Low Transition	**SLC-96** 1 Enabled 0 Disabled	**CRC/MIMIC** See Note 1	**Maint.** 1 4/12 0 2/4

Master Control Word 2 (Channel 31, CSTi0)

UNUSED - KEEP AT 0	**Polarity** 1 No Inversion 0 Inversion	**Loop** 1 Ch. looped back 0 Normal	**Data** 1 Enabled 0 Disabled

Per Channel Control Words (All Channels on CSTi0 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

UNUSED - KEEP AT 0	**A** Txt. Sig. Bit	**B** Txt. Sig. Bit	**C** Txt. Sig. Bit	**D** Txt. Sig. Bit

Per Channel Control Words (All Channels on CSTi1 Except Channels 3, 7, 11, 15, 19, 23, 27 & 31)

YLAIR 1 Detected 0 Normal	**MIMIC** Detected 0 Not Detected	**ERR** F_T Error Count	**ESFYLW** 1 Detected 0 Not Detected	**MFSYNC** 1 Not Detected 0 Detected	**BPV** Bipolar Violation count	**SLIP** Changes State when Slip Performed	**SYN** 1 Out-of-Sync. 0 In-Sync

Master Status Word 1 (Channel 15, CSTo)

BlAlm 1 Detected 0 Not Detected	**FrCnt** Frame Count	**XSt** 1 Xst High 0 Xst Low	**BIPOLAR VIOLATION COUNT**	**CRC-ERROR COUNT**

Master Status Word 2 (Channel 31, CSTo)

CHANNEL COUNT	**BIT COUNT**

Phase Status Word (Channel 3, CSTo)

UNUSED	**A** Rec'd. Sig. Bit	**B** Rec'd. Sig. Bit	**C** Rec'd. Sig. Bit	**D** Rec'd. Sig. Bit

Per Channel Status Word (All Channels on CSTo Except Channels 3, 7, 11, 15, 19, 23, 27, 31)

Note 1: In ESF mode:
1: CRC calc. ignored during Sync.
0: CRC checked for Sync.
In D3/D4 mode:
1: Sync. to first correct S-bit pattern.
0: Will not Sync. if Mimic detected.