MH89792

E1 Transceiver

Preliminary Information

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Features

- Complete primary rate 2048kb/s CEPT line driver and receiver
- Onboard pulse transformers for transmit and receive
- Meets latest ETSI requirements (ETSI ETS 300 011 (NET 5))
- Inductorless clock recovery
- Loss of signal indication/ polarity selection
- Programmable polarity of extracted clock & receive data
- Single +5V operation
- Compatible with all E1 framers
- Small footprint area (<330mm^2)

Applications

- Primary rate ISDN network Interface
- Multiplexer equipment
- Private Network links
- Isochronous LANS/WANS

Ordering Information

MH89792-1	20 Pin SIL Package
MH89792-2	20 Pin SIL Package
MH89792-3	20 Pin SIL Package

0°C to 70°C

Description

The Mitel MH89792 is a low cost E1 line driver/ receiver with clock extraction requiring no external components. There are three versions available:

MH89792-1 for 120Ω twisted pair cable;
MH89792-2 for 75Ω co-axial links;
MH89792-3 for 100Ω digital twisted pair.

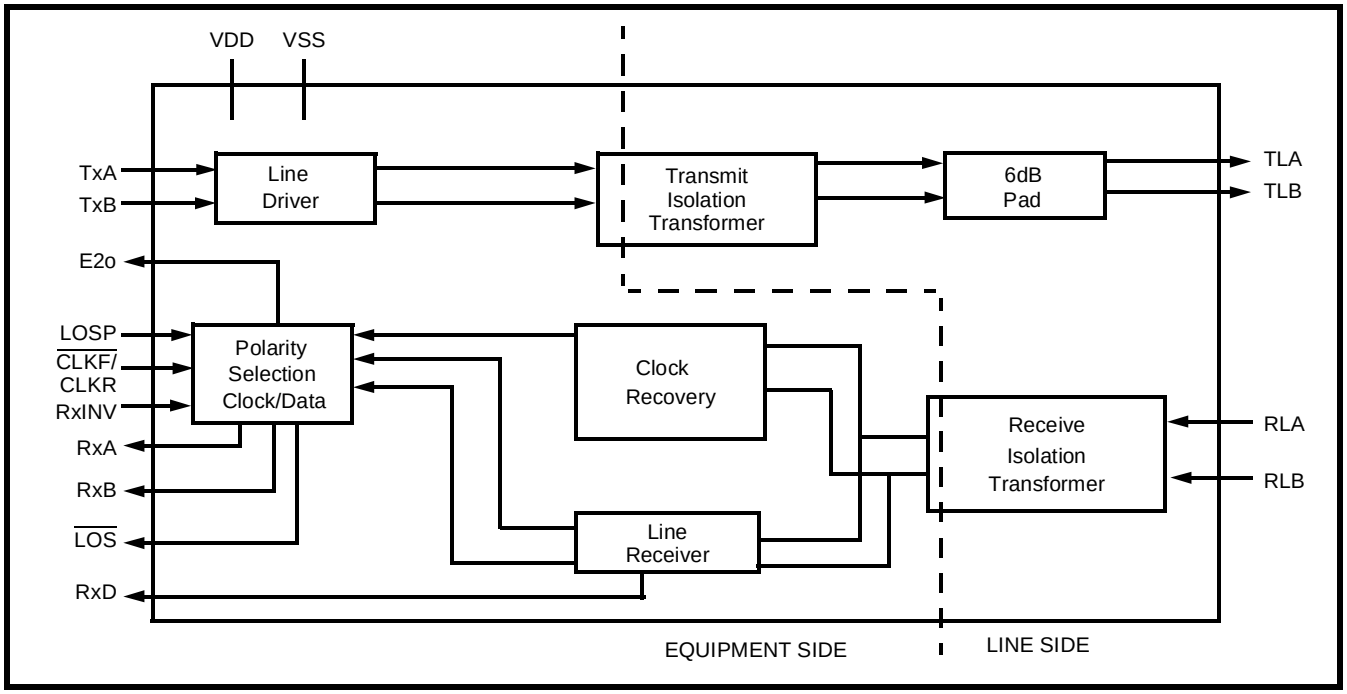

Figure 1 - Functional Block Diagram

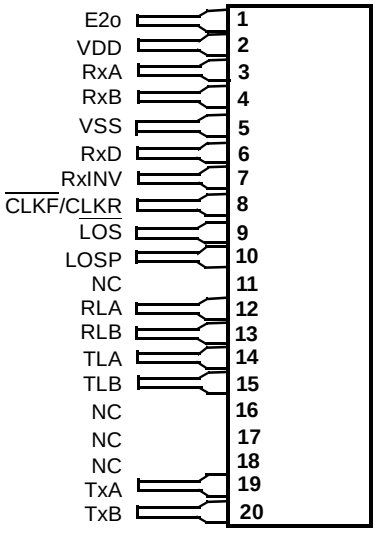

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	E2o	**2048kHz Extracted clock (Output)**. This clock is extracted by the device from the received signal. It is used internally to clock in data received from RLA and RLB.
2	V_{DD}	**D.C. Power (Input)** +5V supply
3	RxA	**Receiver A (Output)**. The bipolar CEPT signal received by the device at RLA and RLB inputs is converted to a unipolar format and output at this pin. This pin should be connected to the positive receive pin of the framer.
4	RxB	**Receiver A (Output)**. This pin should be connected to the negative receive gain pin of the framer and provides a signal of the same format as RxA.
5	V_{SS}	**Ground (Input).** D.C. power return path.
6	RxD	**Received Data (Output)** This unipolar return to zero format signal is the product of RxA and RxB logically “OR” ed and is required by some framers.
7	RxINV	**RxA/RxB inversion (Input**). A logic low applied to this pin will invert the outputs RxA and RxB. A logic high should be applied if no inversion is required.
8	$\overline{\text{CLKF}}$/ CLKR	**E2o phase selection is achieved by use of this pin**. A logic low provides E2o with a falling edge coinciding with the centre of the data bit. A logic high provides E2o with a rising edge.
9	$\overline{\text{LOS}}$	**Loss of signal (Output).** This pin goes low when 128 continuous zeros are received on the RLA and RLB inputs. When RxINV and $\overline{\text{LOS}}$ are low RxA and RxB are forced high. When RxINV is high and $\overline{\text{LOS}}$ is low RxA and RxB are forced low. $\overline{\text{LOS}}$ is reset when 64 ones are received in two dual E1 framer periods.
10	LOSP	**Loss of signal Polarity (Input).** A logic low applied to this pin will invert $\overline{\text{LOS}}$. A logic high should be applied when $\overline{\text{LOS}}$ is required.
11	NC	**No connection.** This pin is not fitted.
12	RLA	**Received Line A (Input)**. The A wire or Tip Connection of the E1 receive line should be connected to this pin.
13	RLB	**Receive Line B (Input).** The B wire or Ring connection of the E1 receive line should be connected to this pin.

Pin Description (Continued)

Pin #	Name	Description
14	TLA	**Transmit Line B (Output).** The B wire of Ring connection of the E1 receive line should be connected to this pin.
15	TLB	**Transmit Line B (Output).** The B wire or Tip connection of the E1 receive line should be connected to this pin.
16	NC	**No Connection.** This pin is not fitted.
17	NC	**No Connection.** This pin is not fitted.
18	NC	**No Connection.** This pin is not fitted.
19	TXA	**Transmit A (Input).** A unipolar signal from the framer device used in conjunction with TxB is used to generate the bipolar output signal.
20	TXB	**Transmit B (Input).** A unipolar signal from the framer device used in conjunction with TxA is used to generate the bipolar output signal.

Functional Description

The MH89792 is a E1 digital trunk interface which when used with an approved framer will conform to CCITT recommendation G.703 for PCM30 and I.431 for the ISDN. The functions provided include line driver and receive circuitry, inductorless clock recovery, data and clock polarity selection and loss of signal indication.

Bipolar Line Receiver

The MH89792 receiver interfaces to the transmission line through an internal pulse transformer which splits the received AMI lines signal into RxA and RxB. These two signals are combined by internal logic to form a new signal which represents the received data, RxD. The signals RxA and RxB may be inverted where required by applying a logic low signal permanently to pin 7, (RxINV). RxD will not be affected by use of this pin.

The input impedance seen by the transmission line is about 120 ohms when using the -1 variant for twisted pair applications, about 75 ohms when using the -2 variant for coaxial cable applications, and is about 100 ohms when using the -3 variant for digital twisted pair applications.

Attenuation of the transmission line shall not exceed 6dB (at 1024kHz) and attenuation characteristics shall be close to the “square root of f”

$$Af\ (dB) = AF_{ref}\ (dB) * \frac{\sqrt{f}}{f_{ref}}$$

Where:
AF - attenuation at frequency f in dB
AF_{ref} - attenuation at frequency f_{ref} in dB (in kHz)
f_{ref} - reference frequency (in this case 1024) kHz
f - frequency in kHz

Bipolar Line Transmitter

The MH89792 transmitter interfaces to the transmission line through an internal pulse transformer which combines the TxA and TxB data into an AMI line coded signal. This is then passed through the 6dB pad prior to being applied to the line.

Clock Extractor

The MH89792 contains a clock extraction circuit which generates the E2o clock from the received data without the use of external crystals or a tunable inductor.

The edge of the E2o extracted clock approximately aligns with the centre of the received data pulse and can be configured as either rising or falling edge by the use of pin 8. (CLKF/CLKR).

Loss of Signal

The circuitry on the MH89792 is capable of detecting 128 continuous ZEROs received on RLA and RLB and indicating this condition as a logic low on pin 9, ($\overline{LOS}$). When $\overline{LOS}$ and $\overline{RxINV}$ are low RxA and RxB are forced high, when $\overline{LOS}$ is $\overline{low}$ and RxINV is high RxA and RxB are forced low $\overline{LOS}$ will not reset $\overline{until}$ 64 ONEs are received in a two E1 frame period. $\overline{LOS}$ may be inverted by applying a logic low to pin 10, (LOSP).

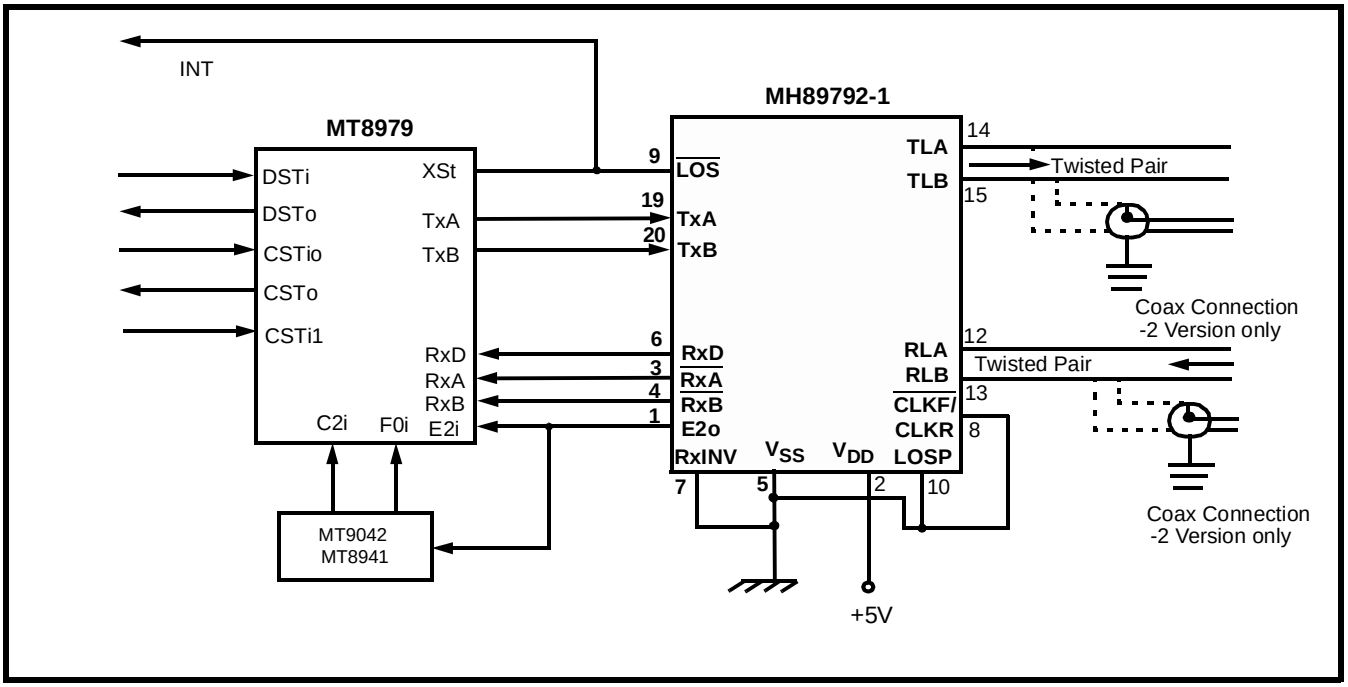

Figure 3a - Application Circuit

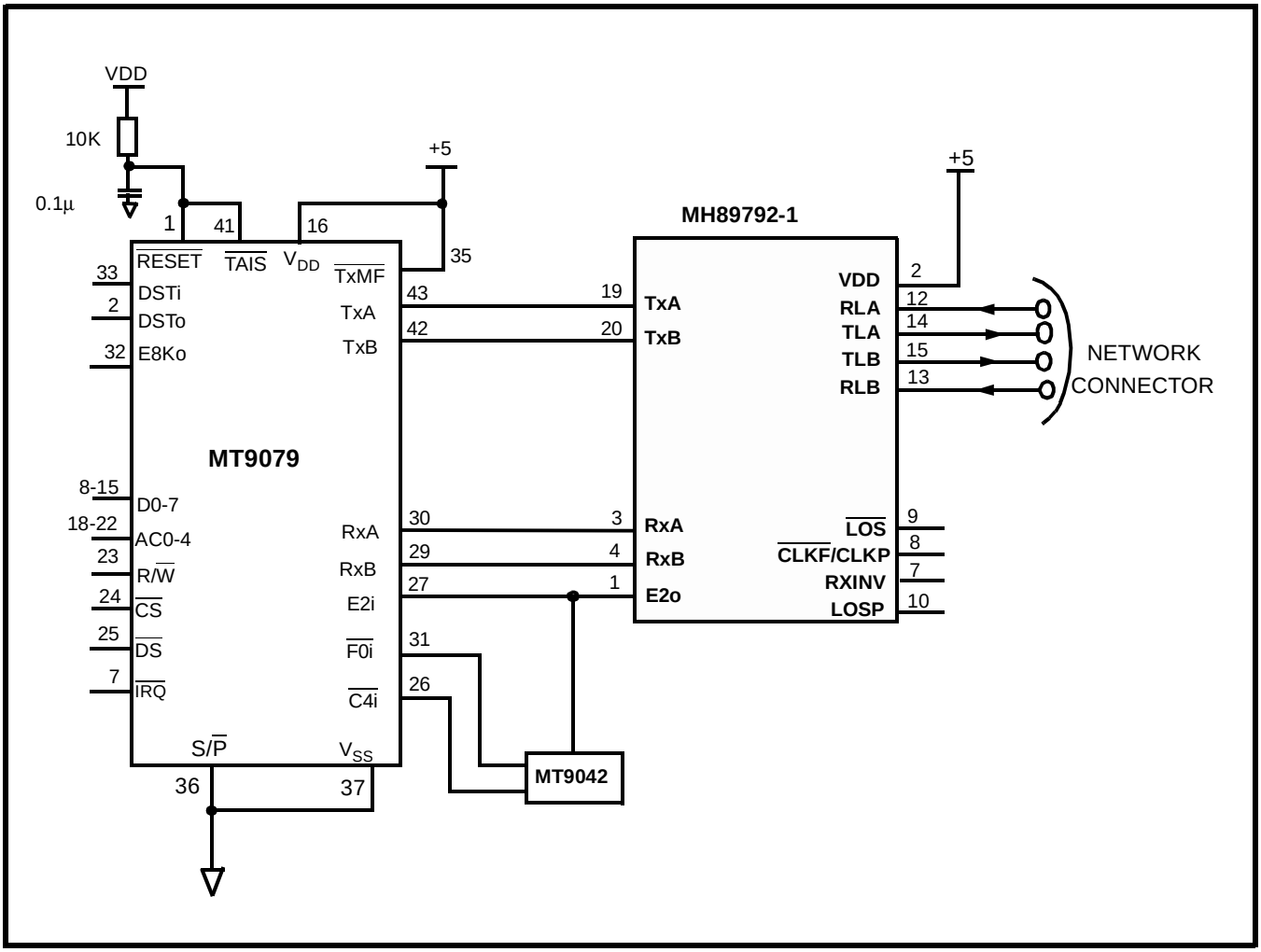

Figure 3b - Application Circuit

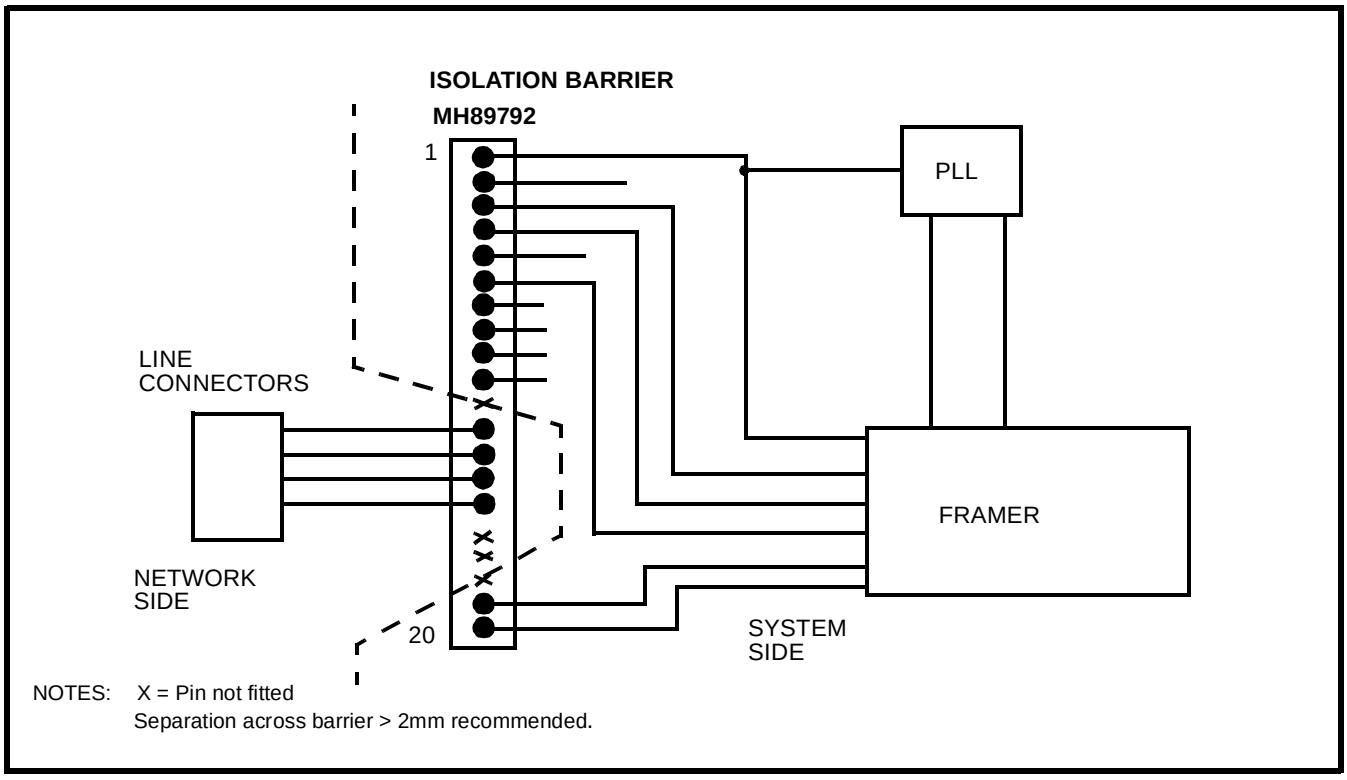

Figure 3c - Application Circuit

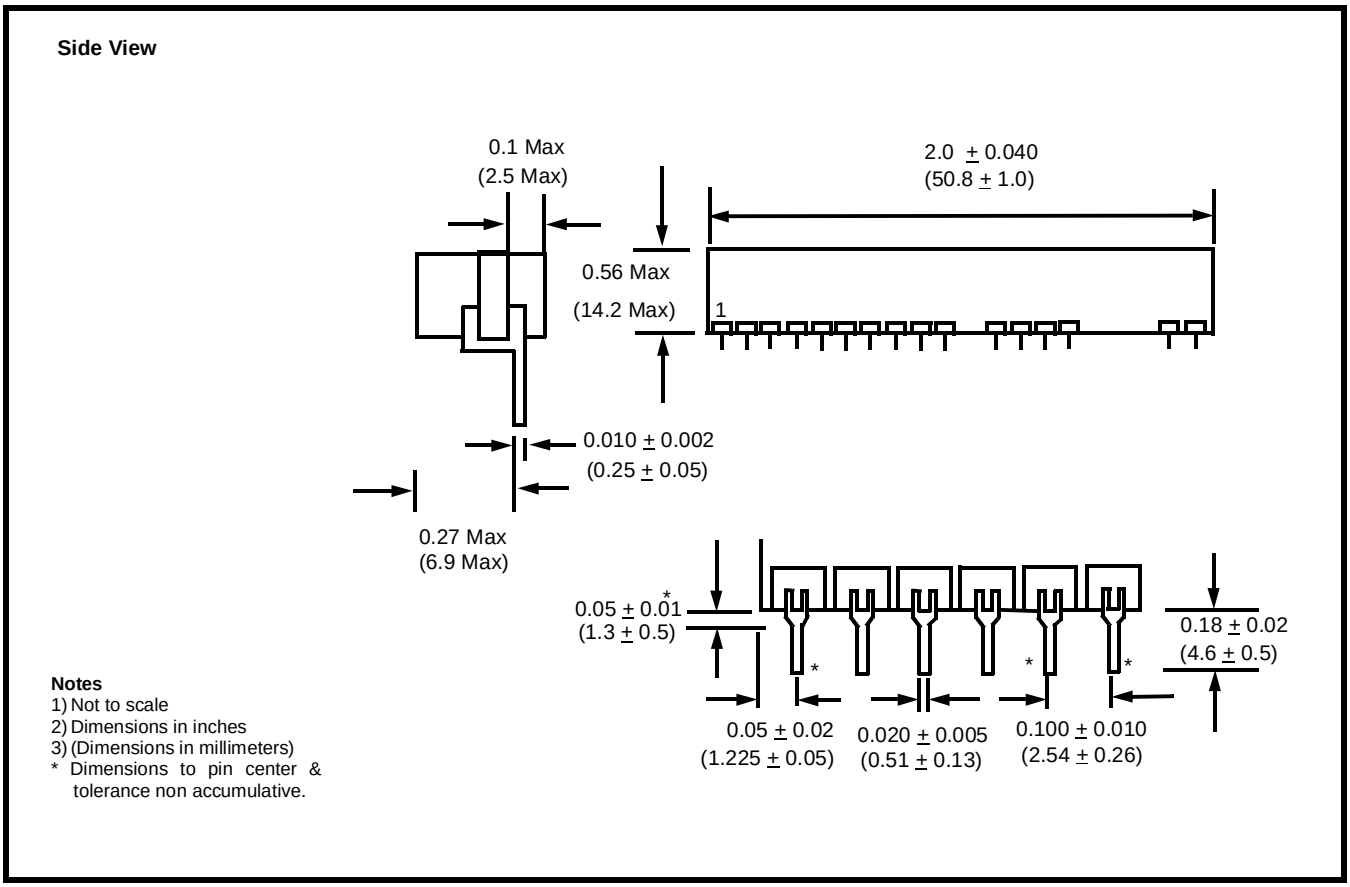

Figure 4 - Mechanical Data

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