

Pb Free Plating Product

MJ21195G/MJ21196G



CASE 1-07 TO-204AA

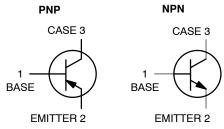
(TO-3)

250 Watt Silicon Type Metal Package Power Transistor

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain $-h_{FE} = 25$ Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

SCHEMATIC







Rating	:	Symbol	Value	Unit
Collector–Emitter Voltage		VCEO	250	Vdc
Collector–Base Voltage		V _{CBO}	400	Vdc
Emitter–Base Voltage		V _{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V		VCEX	400	Vdc
Collector Current — Continuous Peak ⁽¹⁾		IC	16 30	Adc
Base Current — Continuous		Ι _Β	5	Adc
Total Power Dissipation @ T _C = 25°C Derate Above 25°C		PD	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range		Tj, T _{stg}	- 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _θ JC	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = $25^{\circ}C \pm 5^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Мах	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}, I_B = 0$)	V _{CEO(sus)}	250	_	_	Vdc
Collector Cutoff Current (V _{CE} = 200 Vdc, I _B = 0)	ICEO	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μ s, Duty Cycle \leq 10%.

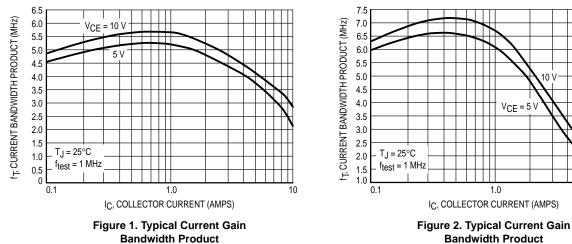
(continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

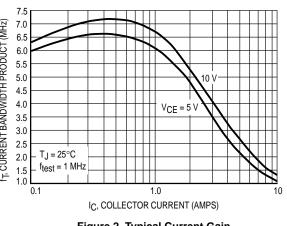
Characteristic		Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS						
Emitter Cutoff Current ($V_{CE} = 5 Vdc, I_C = 0$)		IEBO	_	_	100	μAdc
Collector Cutoff Current (V _{CE} = 250 Vdc, V _{BE(off)} = 1.5 Vdc)		ICEX	_	_	100	μAdc
SECOND BREAKDOWN				•		•
Second Breakdown Collector Current with Base Forv (V _{CE} = 50 Vdc, t = 1 s (non-repetitive) (V _{CE} = 80 Vdc, t = 1 s (non-repetitive)	ward Biased	I _{S/b}	5 2.5			Adc
ON CHARACTERISTICS						
DC Current Gain (I _C = 8 Adc, V_{CE} = 5 Vdc) (I _C = 16 Adc, V_{CE} = 5 Vdc)		hFE	25 8		75	
Base–Emitter On Voltage (I _C = 8 Adc, V _{CE} = 5 Vdc)		V _{BE(on)}	_	—	2.2	Vdc
Collector–Emitter Saturation Voltage ($I_C = 8 \text{ Adc}, I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}, I_B = 3.2 \text{ Adc}$)		V _{CE(sat)}			1.4 4	Vdc
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output $V_{RMS} = 28.3 \text{ V}, f = 1 \text{ kHz}, P_{LOAD} = 100 \text{ W}_{RMS}$ (Matched pair h _{FE} = 50 @ 5 A/5 V)	hFE unmatched	THD	_	0.8	_	%
	h _{FE} matched		_	0.08	_	
Current Gain Bandwidth Product (I _C = 1 Adc, V _{CE} = 10 Vdc, f _{test} = 1 MHz)		fΤ	4	—	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)		C _{ob}	—	_	500	pF

(1) Pulse Test: Pulse Width = $300 \ \mu$ s, Duty Cycle $\leq 2\%$









Bandwidth Product

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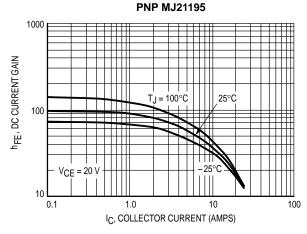


Figure 3. DC Current Gain, VCE = 20 V

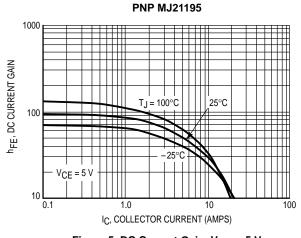


Figure 5. DC Current Gain, V_{CE} = 5 V

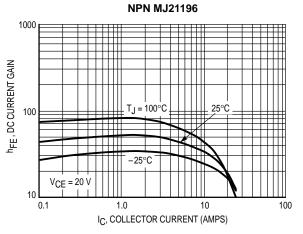


Figure 4. DC Current Gain, VCE = 20 V

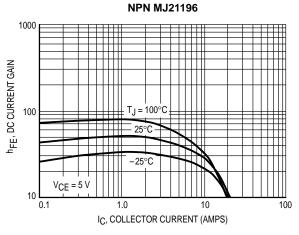


Figure 6. DC Current Gain, V_{CE} = 5 V

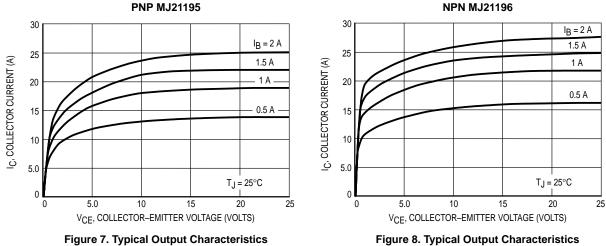


Figure 7. Typical Output Characteristics

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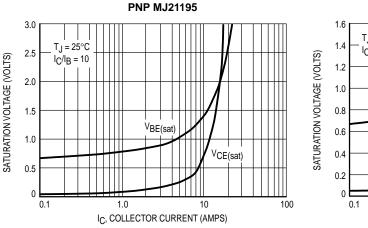
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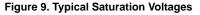
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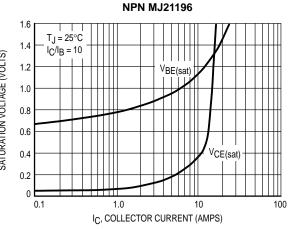


Figure 10. Typical Saturation Voltages

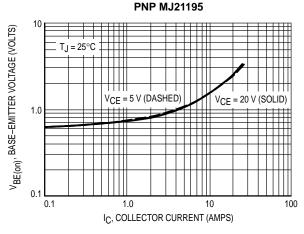


Figure 11. Typical Base–Emitter Voltage

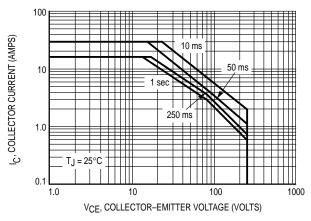
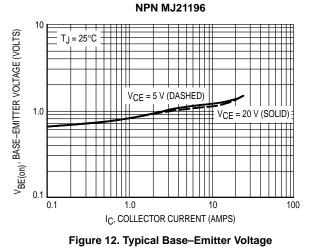


Figure 13. Active Region Safe Operating Area



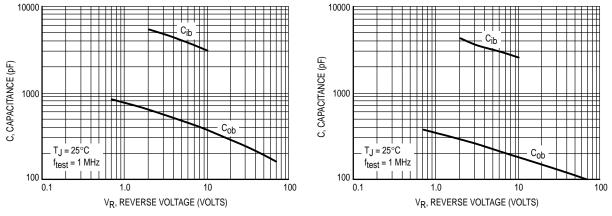
There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_{C} - V_{CE}$ limits of the transistor that must be observed for reliable

greater dissipation than the curves indicate. The data of Figure 13 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

operation; i.e., the transistor must not be subjected to

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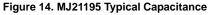


Figure 15. MJ21196 Typical Capacitance

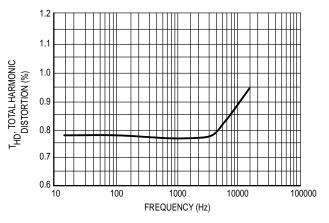


Figure 16. Typical Total Harmonic Distortion

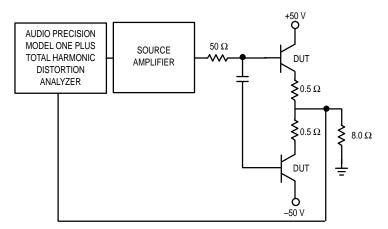


Figure 17. Total Harmonic Distortion Test Circuit