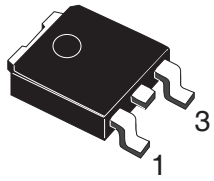
MJD31CT4-A

Low voltage NPN power transistor

General features

- This device is qualified for automotive application
- Surface-mounting TO-252 power package in tape & reel
- In compliance with the 2002/93/EC European Directive



DPAK

TO-252

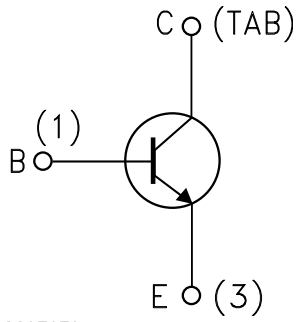
Applications

- General purpose switching and amplifier transistor

Description

The device is manufactured in Planar technology with “Base Island” layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

Internal schematic diagram



Order codes

Part Number	Marking	Package	Packaging
MJD31CT4-A	MJD31C	DPAK	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage (I_E = 0)	100	V
V_{CEO}	Collector-base voltage (I_B = 0)	100	V
V_{EBO}	Emitter-base voltage (I_C = 0)	5	V
I_C	Collector current	3	A
I_{CM}	Collector peak current	5	A
I_B	Base current	1	A
P_{TOT}	Total dissipation at T_c = 25°C	15	W
T_{stg}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 2. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} = 0)	V_{CE} = 100V			20	µA
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CB} = 60V			50	µA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = 5V			0.1	mA
$V_{CEO(sus)}$ (1)	Collector-emitter sustaining voltage (I_B = 0)	I_C =30mA	100			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = 3A I_B = 375mA			1.2	V
$V_{BE(on)}$ (1)	Base-emitter on voltage	I_C = 3A V_{CE}= 4V			1.8	V
h_{FE}	DC current gain	I_C = 1A V_{CE} =4V I_C = 3A V_{CE} =4V	25 10		 50	

Note (1) Pulsed duration = 300 µs, duty cycle ≤1.5%

2.1 Electrical characteristic (curves)

Figure 1. Safe operating area

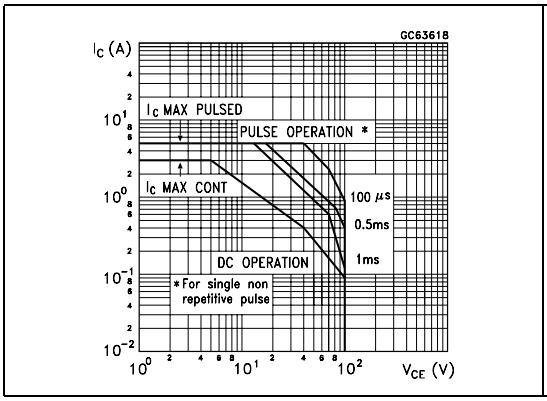


Figure 2. Derating curve

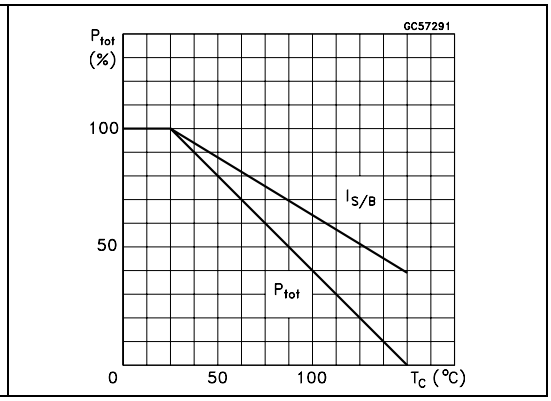


Figure 3. DC current gain

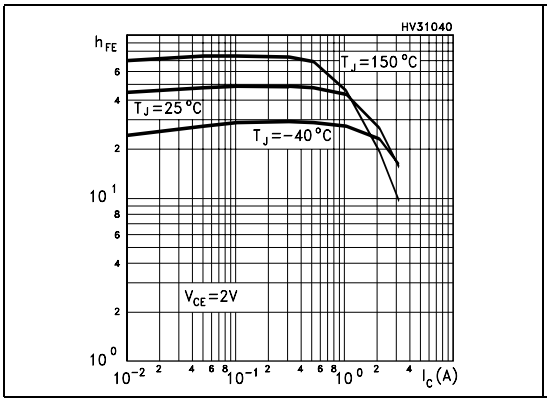


Figure 4. DC current gain

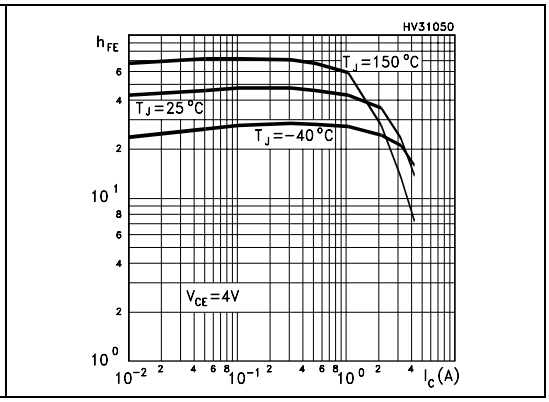


Figure 5. Collector-emitter saturation voltage

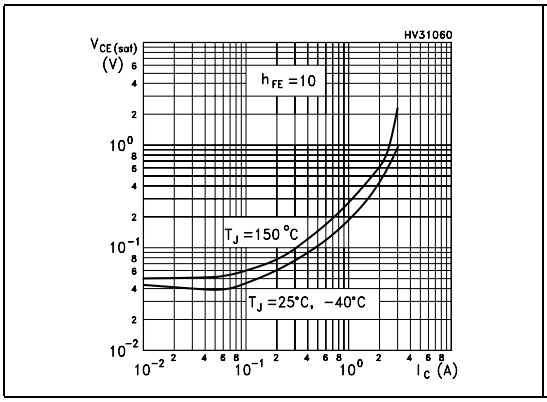


Figure 6. Base-emitter saturation voltage

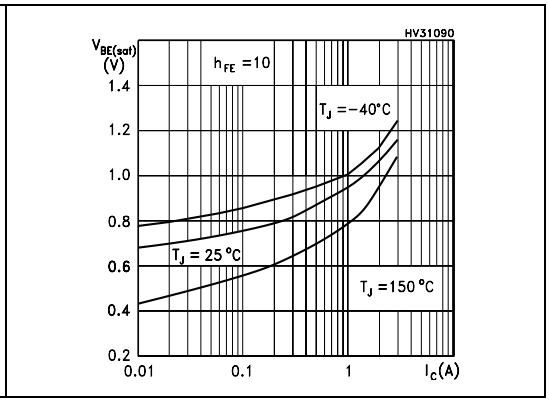


Figure 7. Collector-emitter on voltage

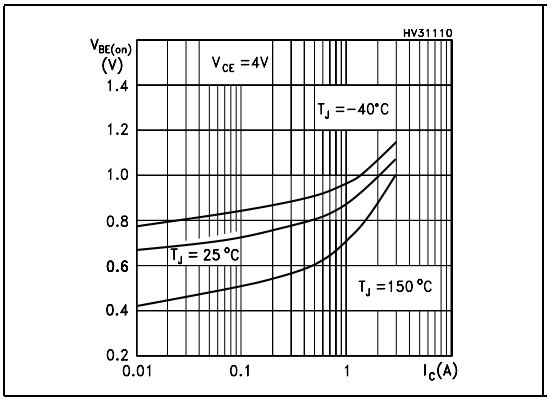


Figure 8. Resistive load switching time

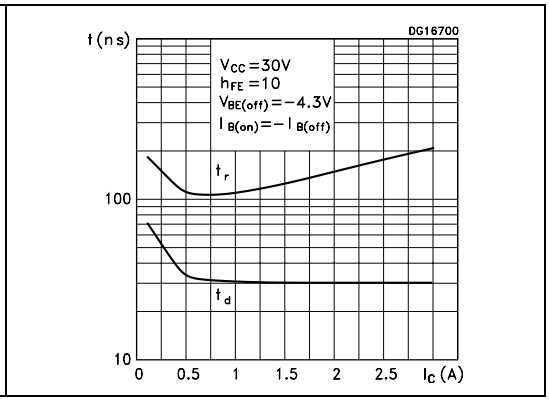
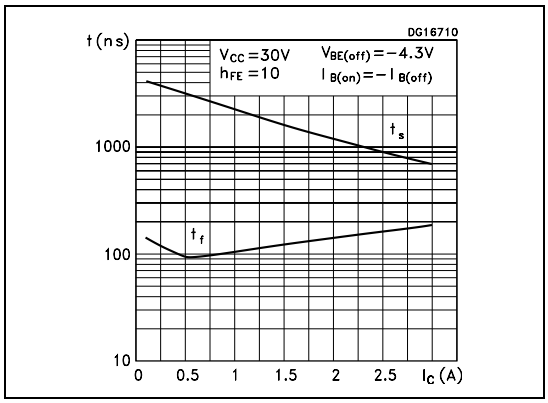


Figure 9. Resistive load switching time



2.2 Test circuits

Figure 10. Resistive load switching test circuit

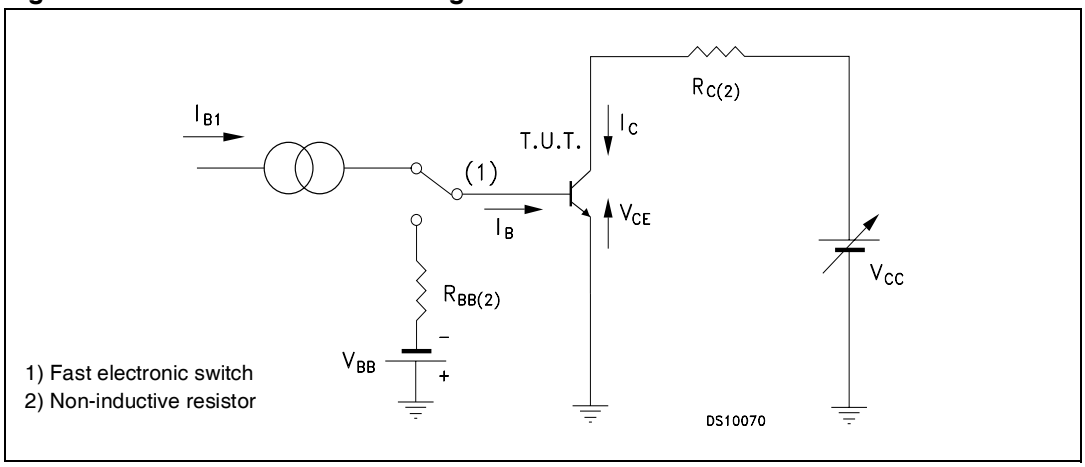
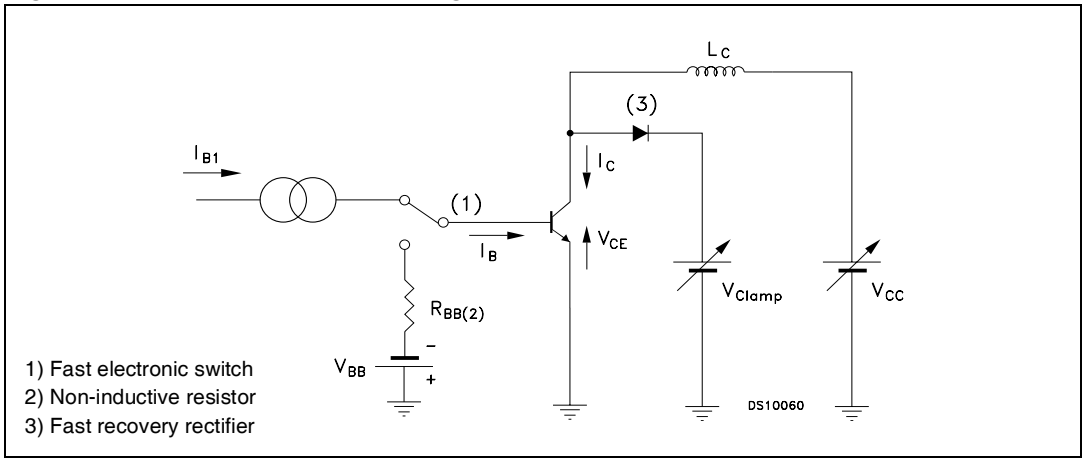


Figure 11. Inductive load switching test circuit

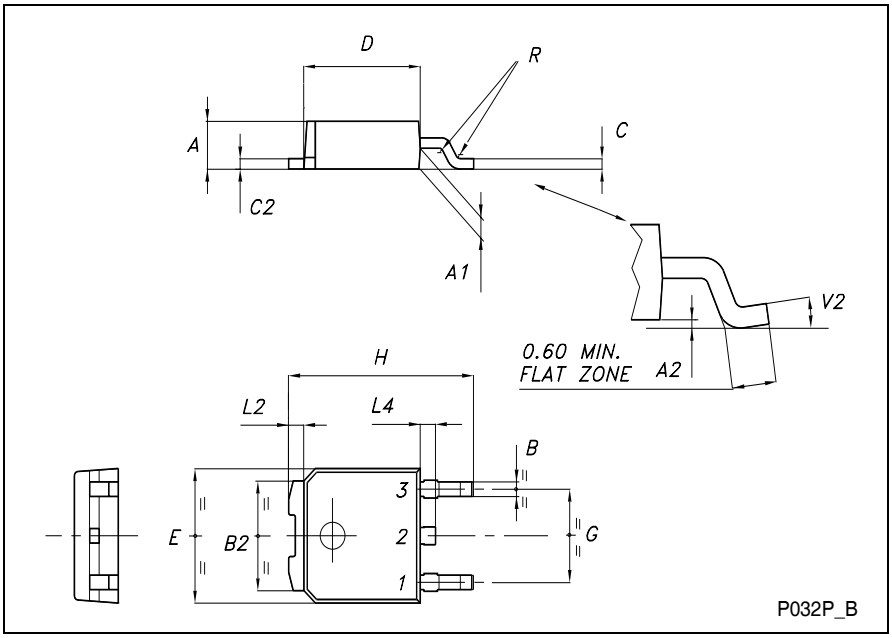


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



4 Revision history

Table 3. Revision history

Date	Revision	Changes
24-Apr-2007	1	Initial release.

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