



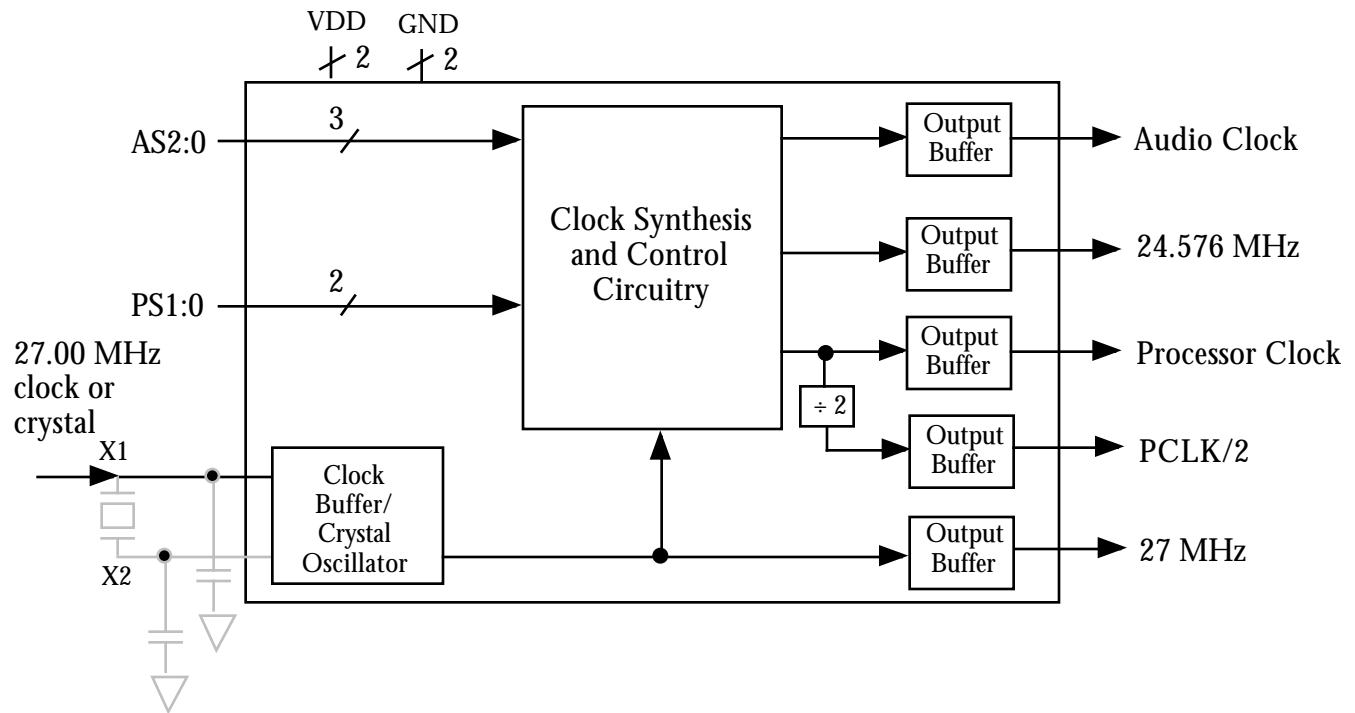
MK2745-21 DVD/MPEG Clock Source

Description


The MK2745-21 is a low cost, low jitter, high performance clock synthesizer for DVD and other MPEG 2 based applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 27.00MHz fundamental mode crystal or clock input to produce multiple output clocks including the processor clock, the processor clock divided by two, 27 MHz, 24.576 MHz, and a selectable audio clock. The audio clocks are frequency locked to the 27.00MHz input using our patented zero ppm error techniques, allowing audio and video to track exactly, thereby eliminating the need for large buffer memory.

MicroClock manufactures the largest variety of DVD, Set-Top Box, and multimedia clock synthesizers for all applications. Consult MicroClock to eliminate crystals and oscillators from your board.

Block Diagram



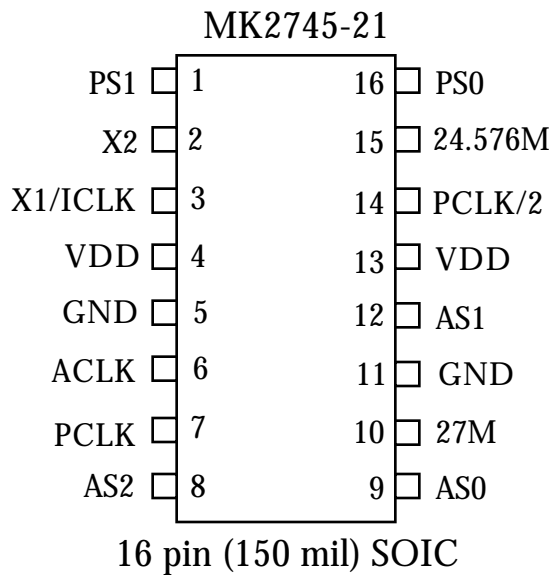
Features

- Packaged in 16 pin narrow (150 mil) SOIC 
- Ideal for LuxSonor's DVD solutions
- 3.3V upgrade to MK2744
- Patented zero ppm audio clock error for 256X and 384X sampling rates
- Selectable audio sampling frequencies support 32 kHz, 44.1 kHz, and 48 kHz in most DACs
- 27.00 MHz fundamental crystal or clock input
- Eight selectable processor frequencies
- Fixed clocks of 27 and 24.576 MHz
- Zero ppm error in all clocks
- Full CMOS outputs with 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.0V to 5.5V operating voltage
- See also the MK2712 for NTSC/PAL clocks



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Pin Assignment



Audio Clock (in MHz) Decoding Table

AS2	AS1	AS0	ACLK
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

Processor Clock (in MHz)

PS1	PS0	PCLK	PCLK/2
0	0	66.66	33.33
0	1	80	40
1	0	50	25
1	1	60	30

0 = connect directly to ground
1 = connect directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	PS1	I	Processor clock Select 1. Selects processor clock outputs per table above.
2	X2	XO	Crystal connection. Connect to 27 MHz crystal. Leave unconnected for clock input.
3	X1/ICLK	XI	Crystal connection. Connect to 27 MHz crystal or connect to 27 MHz input clock.
4	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
5	GND	P	Connect to ground.
6	ACLK	O	Audio Clock output. Determined by status of AS2, AS1, AS0. See table above.
7	PCLK	O	Processor Clock output. Determined by status of PS1, PS0. See table above.
8	AS2	I	Audio clock Select 2. Selects audio clock on pin 6 per table above.
9	AS0	I	Audio clock Select 0. Selects audio clock on pin 6 per table above.
10	27M	O	27.00 MHz clock output.
11	GND	P	Connect to ground.
12	AS1	I	Audio clock Select 1. Selects audio clock on pin 6 per table above.
13	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
14	PCLK/2	O	Processor Clock divided by two output. Determined by status of PS1, PS0. See table above.
15	24.576M	O	24.576 MHz clock output.
16	PS0	I	Processor clock Select 0. Selects processor clock outputs per table above.

Key: I = Input, O = output, P = power supply connection



Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, X1/ICLK pin only		VDD/2 + 1	VDD/2		V
Input Low Voltage, VIL, X1/ICLK pin only			VDD/2	VDD/2 - 1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, note 2		37		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Frequency			27.000		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40		60	%
Frequency error, all clocks			0	1	ppm
Absolute Jitter, short term	Variation from mean		200		ps

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With Processor clock at 50MHz, and ACLK at 16.93MHz.

External Components

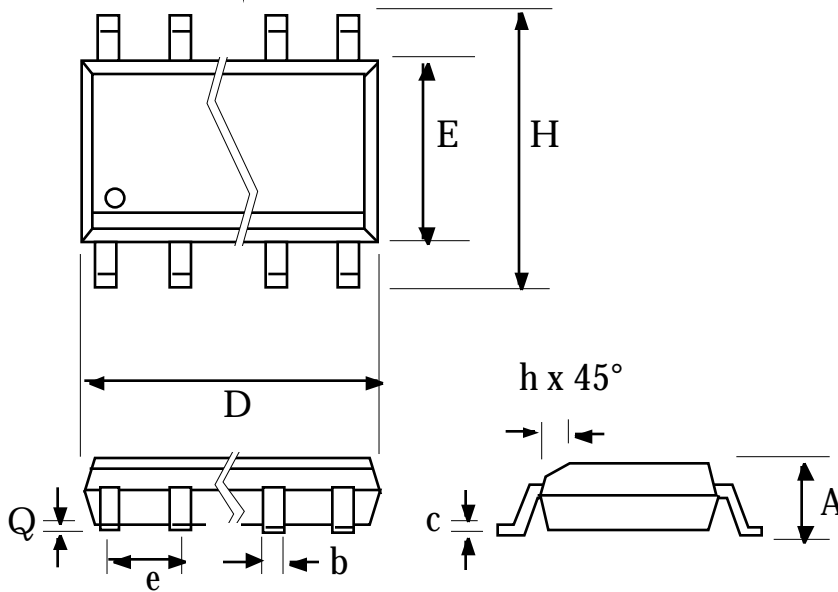
The MK2745-21 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD and GND, as close to the MK2745-21 as possible. A series termination resistor of 33 Ω may be used for each clock output. If a clock input is not used, the 27.00 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant, 50ppm or better. Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = $(C_L - 6) \times 2$. So for a crystal with 16pF load capacitance, two 20pF caps should be used.



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Package Outline and Package Dimensions

16 pin SOIC narrow



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.055	0.070	1.397	1.778
b	0.013	0.019	0.330	0.483
c	0.007	0.010	0.191	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2745-21S	MK2745-21S	tubes	16 pin narrow SOIC	0-70°C
MK2745-21STR	MK2745-21S	tape and reel	16 pin narrow SOIC	0-70°C

Rev. 03318, version A . First publication, Preliminary.

Rev. 04218, version B. Corrected VDD, VIH/VIL under DC Characteristics. Preliminary.

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