FEDL9092-01
Issue Date: Nov. 4, 2003

OKI Semiconductor

ML9092-01/02/03/04

LCD Driver with Key Scanner and RAM

GENERAL DESCRIPTION

The ML9092-01/02/03/04 are LCD drivers that have internal RAM and a key scan function. They are best suited for car audio displays.
Since 1-bit data of the display data RAM corresponds to the light-on or light-off of 1-dot of the LCD panel (a bit map system), a flexible display is possible.
A graphic display system of a maximum of 60 × 10 dots (56 × 10 dots for ML9092-01, 60 × 10 dots for ML9092-02/03/04). can be implemented.
The ML9092-01/02 do not require any power supply circuit to drive the LCD, because they have internal voltage doublers. (If a large-sized panel is driven, use the ML9092-03, to which the LCD driving voltage is supplied externally.)
The internal key scan circuit (5 × 5 key scanning for ML9092-01/04, 6 × 4 key scanning for ML9092-02/03) has eliminated the needs of key scanning by the CPU, thereby enabling the efficient use of the CPU ports.

FEATURES

- Logic voltage : 4.5 to 5.5 V
- LCD drive voltage : 4.5 to 16.5 V (positive voltage)
- Segment output : 56 outputs for ML9092-01; 60 outputs for ML9092-02/03/04
- Common output : 10 outputs
- Built-in bit-mapped RAM : 60 × 10 = 600 bits (for ML9092-01 only: 56 × 10 = 560 bits for the RAM display area)
- 4-pin serial interface with CPU: $\overline{CS}$, $\overline{CP}$, DI/O, KREQ
- Built-in LCD drive bias resistors
- Built-in voltage doubler circuit
- For the ML9092-01/04, the built-in 5 × 5 key scanner makes it possible to read the status of 25 key switches and 1-channel rotary encoder. In addition, the ML9092-01/04 have an 8-bit, 3-channlel PWM circuit built in.
  For the ML9092-02/03, the built-in 6 × 4 key scanner makes it possible to read the status of 24 key switches and 1-channel rotary encoder.
- Port A output : 1 pin, output current = –15 mA : Can be used for LED driving
- Port B output : 3 pins, output current = –2 mA : Applies to ML9092-01/04 (capable of PWM output)
- Port C output : 5 pin, output current = –2 mA : Applies to ML9092-01 only
- Port D output : 5 pins, output current = –2 mA : Applies to ML9092-01 only
- Temperature range : –40 to +85°C
- Package: 100-pin plastic TQFP (TQFP100-P-1414-0.50-K)
  (Product name: ML9092-01TB, ML9092-02TB, ML9092-03TB, ML9092-04TB)

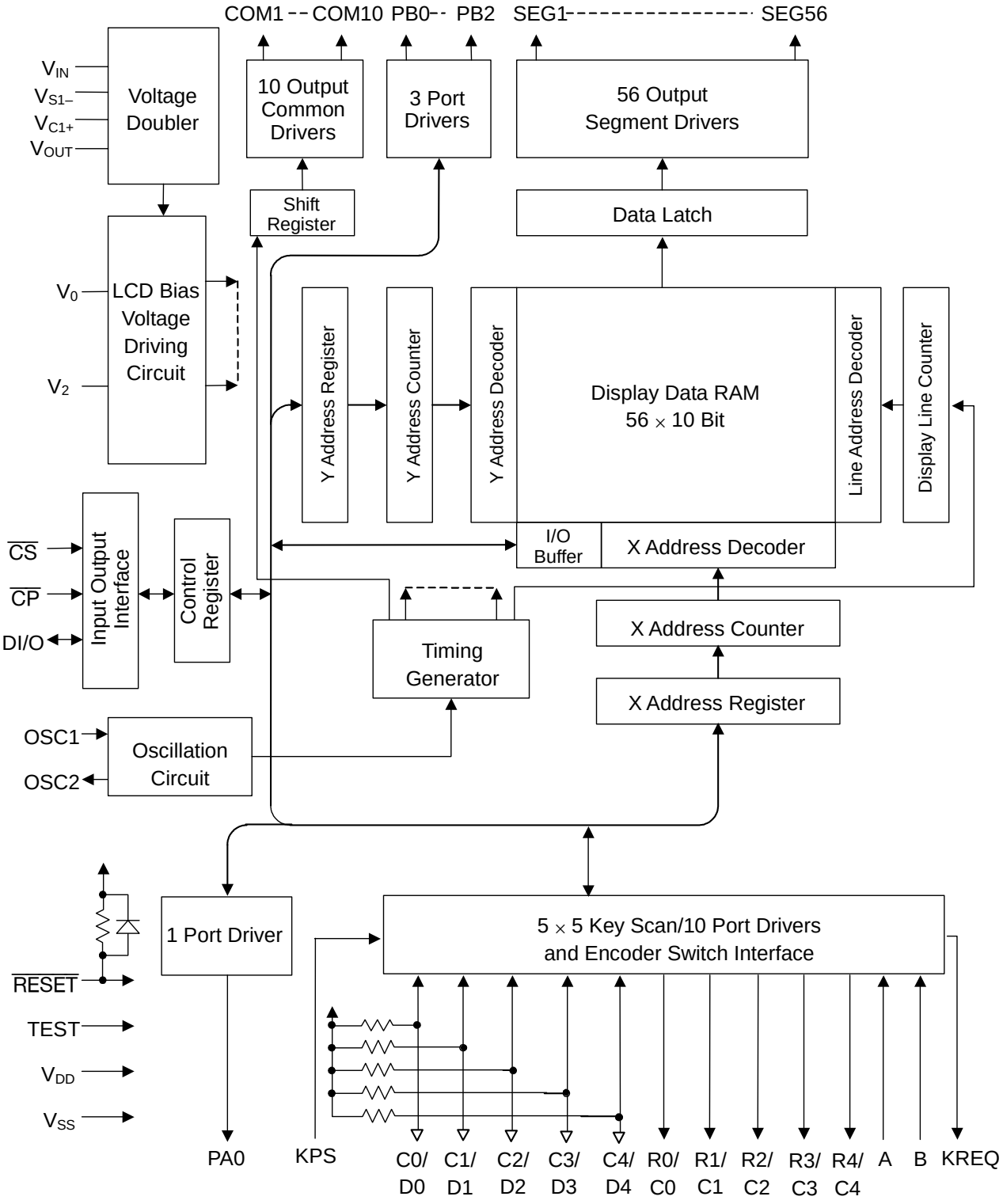
Comparison between the ML9092-01, ML9092-02, ML9092-03, and ML9092-04

Item	ML9092-01	ML9092-02	ML9092-03	ML9092-04
Number of common outputs	10 Max.	10 Max.	10 Max.	10 Max.
Number of dots on the LCD screen (selectable by program)	8 × 56 9 × 56 10 × 56	8 × 60 9 × 60 10 × 60	8 × 60 9 × 60 10 × 60	8 × 60 9 × 60 10 × 60
Number of port A outputs	1	1	1	1
Number of port B outputs	3	0	0	3
Number of port C and D outputs (see note below)	5 each	0	0	0
Key scan (see note below)	5 × 5 key scan	4 × 6 key scan	4 × 6 key scan	5 × 5 key scan
Rotary encoder	1 channel	1 channel	1 channel	1 channel
Voltage doubler	Yes	Yes	No	No
PWM circuit	8-bit, 3-channel	No	No	8-bit, 3-channel

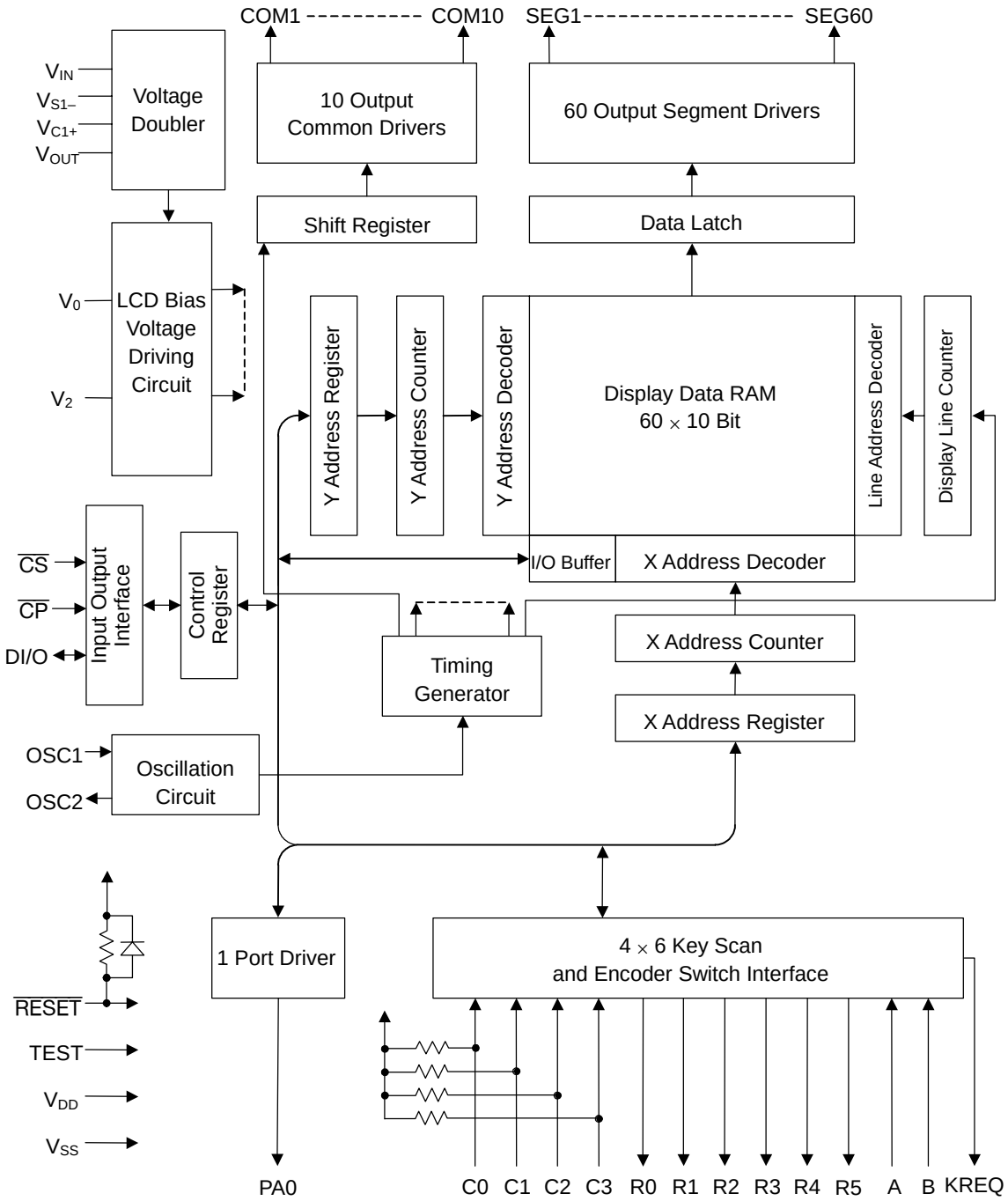
Note: The key scan function and port C/D cannot be used concurrently. Use either.

BLOCK DIAGRAM

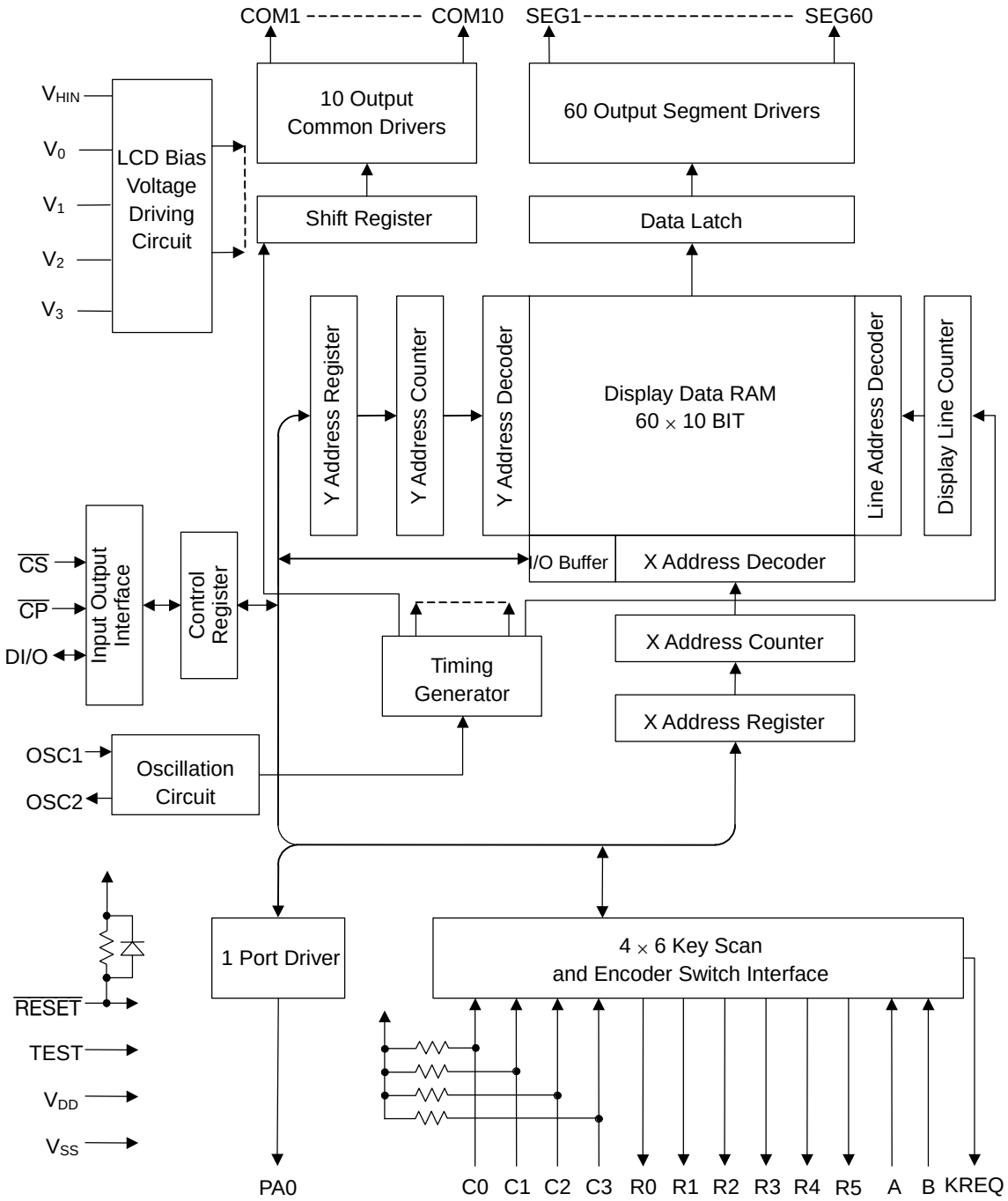
ML9092-01



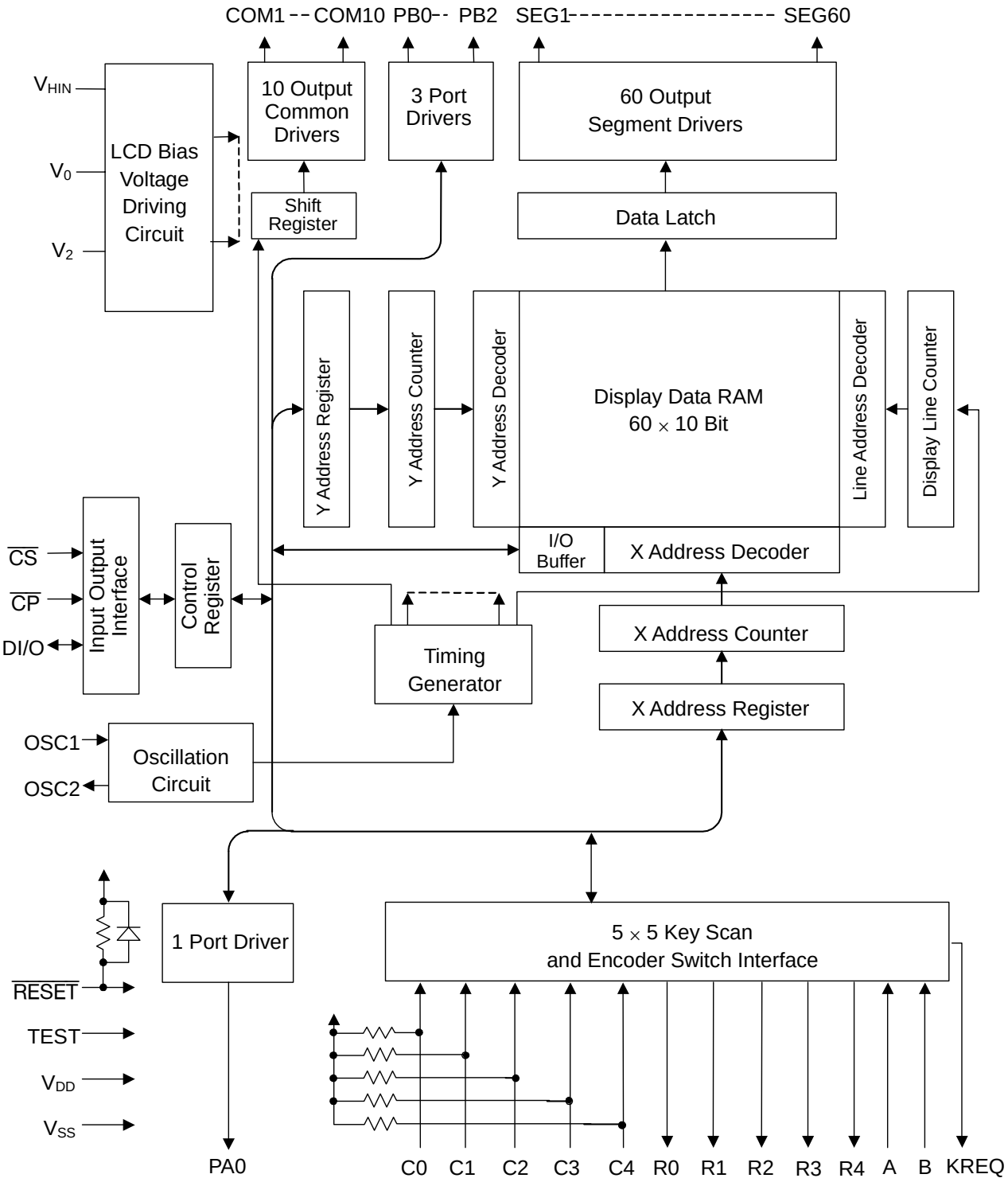
ML9092-02


COM1
COM10
SEG1
SEG60
VIN
VS1–
VC1+
VOUT
Voltage Doubler
10 Output Common Drivers
60 Output Segment Drivers
Shift Register
Data Latch
V0
V2
LCD Bias Voltage Driving Circuit
Y Address Register
Y Address Counter
Y Address Decoder
Display Data RAM 60 × 10 Bit
Line Address Decoder
Display Line Counter
CS
CP
DI/O
Input Output Interface
Control Register
I/O Buffer
X Address Decoder
X Address Counter
Timing Generator
X Address Register
OSC1
OSC2
Oscillation Circuit
1 Port Driver
4 × 6 Key Scan and Encoder Switch Interface
RESET
TEST
VDD
VSS
PA0
C0 C1 C2 C3 R0 R1 R2 R3 R4 R5 A B KREQ

ML9092-03

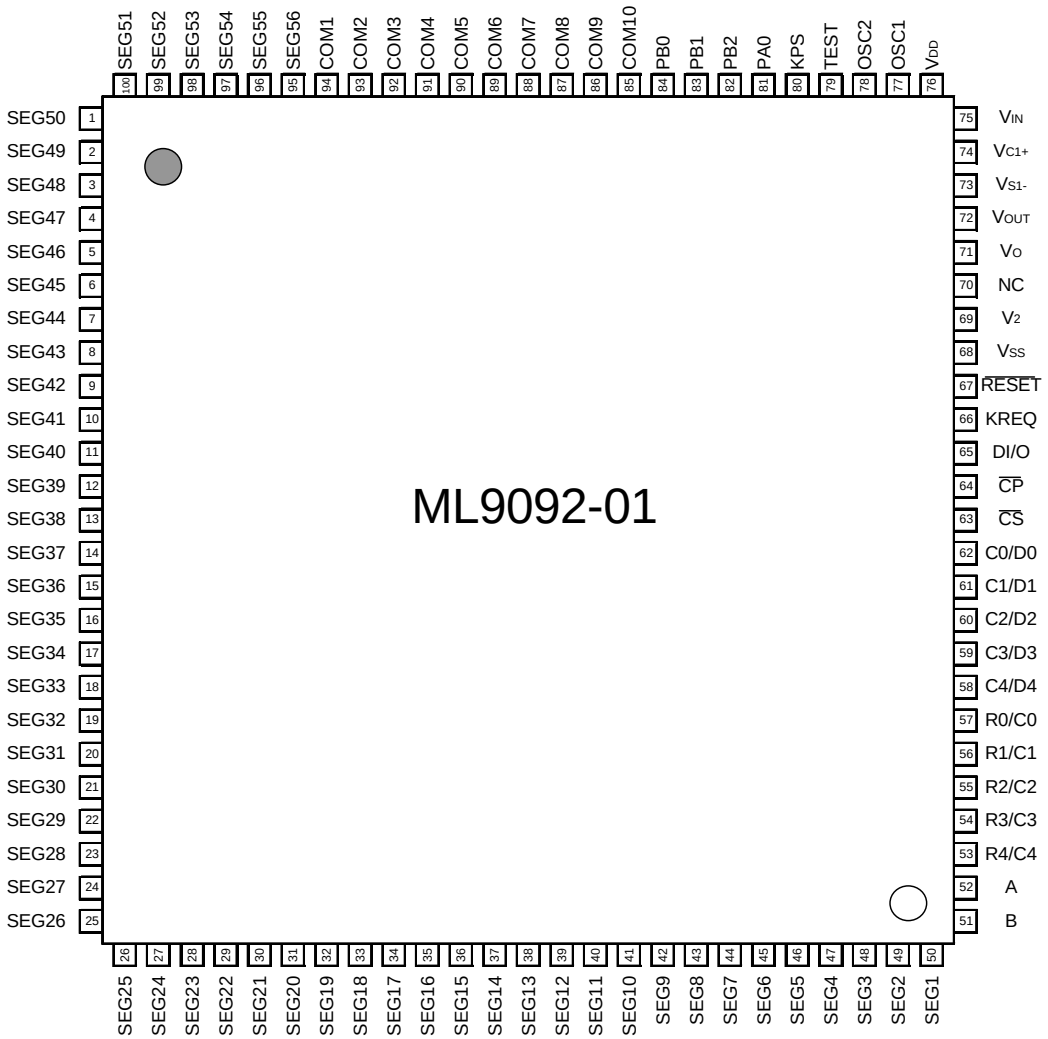

COM1
COM10
SEG1
SEG60
V_{HIN}
V_0
V_1
V_2
V_3
LCD Bias Voltage Driving Circuit
10 Output Common Drivers
60 Output Segment Drivers
Shift Register
Data Latch
Y Address Register
Y Address Counter
Y Address Decoder
Display Data RAM 60 × 10 BIT
Line Address Decoder
Display Line Counter
I/O Buffer
X Address Decoder
X Address Counter
X Address Register
$\overline{CS}$
$\overline{CP}$
DI/O
Input Output Interface
Control Register
Timing Generator
OSC1
OSC2
Oscillation Circuit
$\overline{RESET}$
TEST
V_{DD}
V_{SS}
1 Port Driver
4 × 6 Key Scan and Encoder Switch Interface
PA0
C0 C1 C2 C3 R0 R1 R2 R3 R4 R5 A B KREQ

ML9092-04


COM1
COM10
PB0
PB2
SEG1
SEG60
V_{HIN}
V_0
V_2
LCD Bias Voltage Driving Circuit
10 Output Common Drivers
3 Port Drivers
60 Output Segment Drivers
Shift Register
Data Latch
Y Address Register
Y Address Counter
Y Address Decoder
Display Data RAM 60 × 10 Bit
Line Address Decoder
Display Line Counter
I/O Buffer
X Address Decoder
$\overline{CS}$
$\overline{CP}$
DI/O
Input Output Interface
Control Register
Timing Generator
X Address Counter
X Address Register
OSC1
OSC2
Oscillation Circuit
1 Port Driver
5 × 5 Key Scan and Encoder Switch Interface
$\overline{RESET}$
TEST
V_{DD}
V_{SS}
PA0
C0
C1
C2
C3
C4
R0
R1
R2
R3
R4
A
B
KREQ

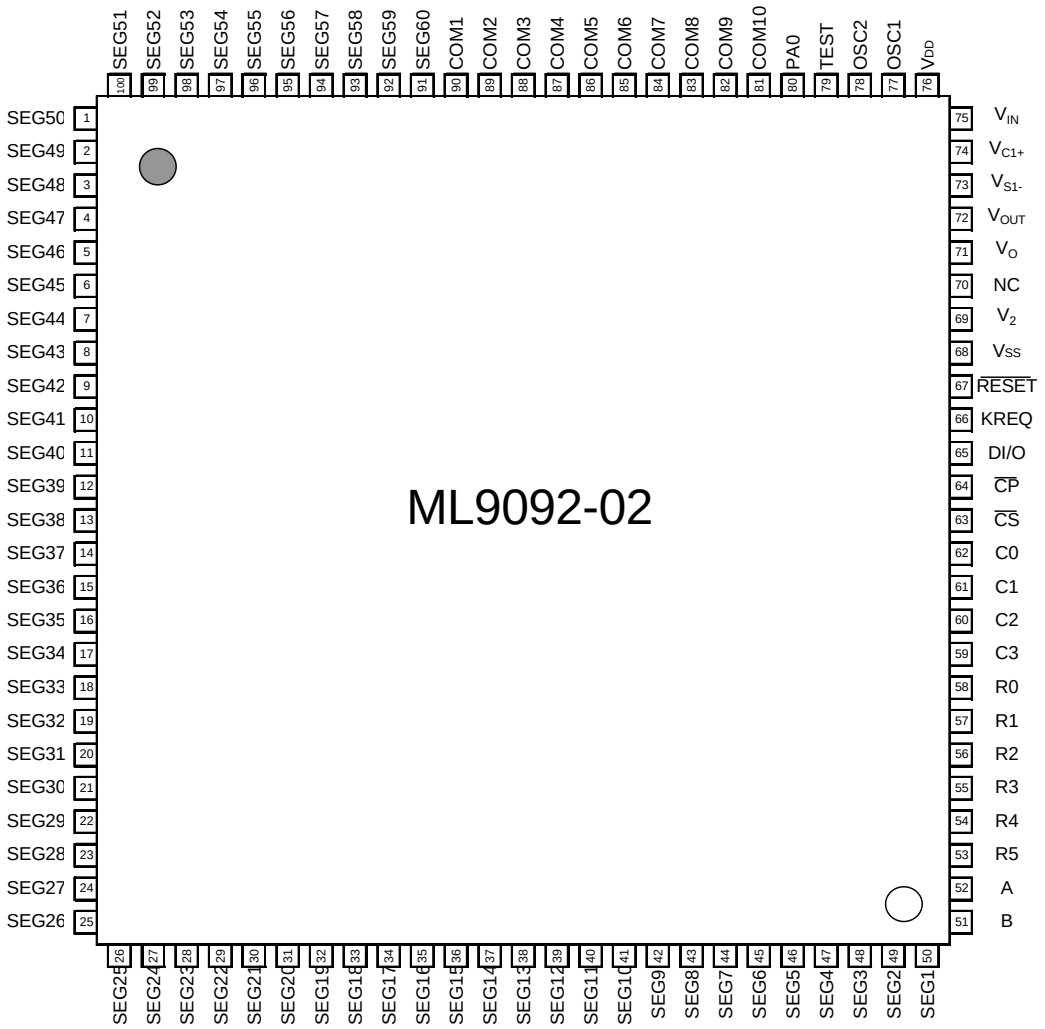
PIN CONFIGURATION (TOP VIEW)

ML9092-01



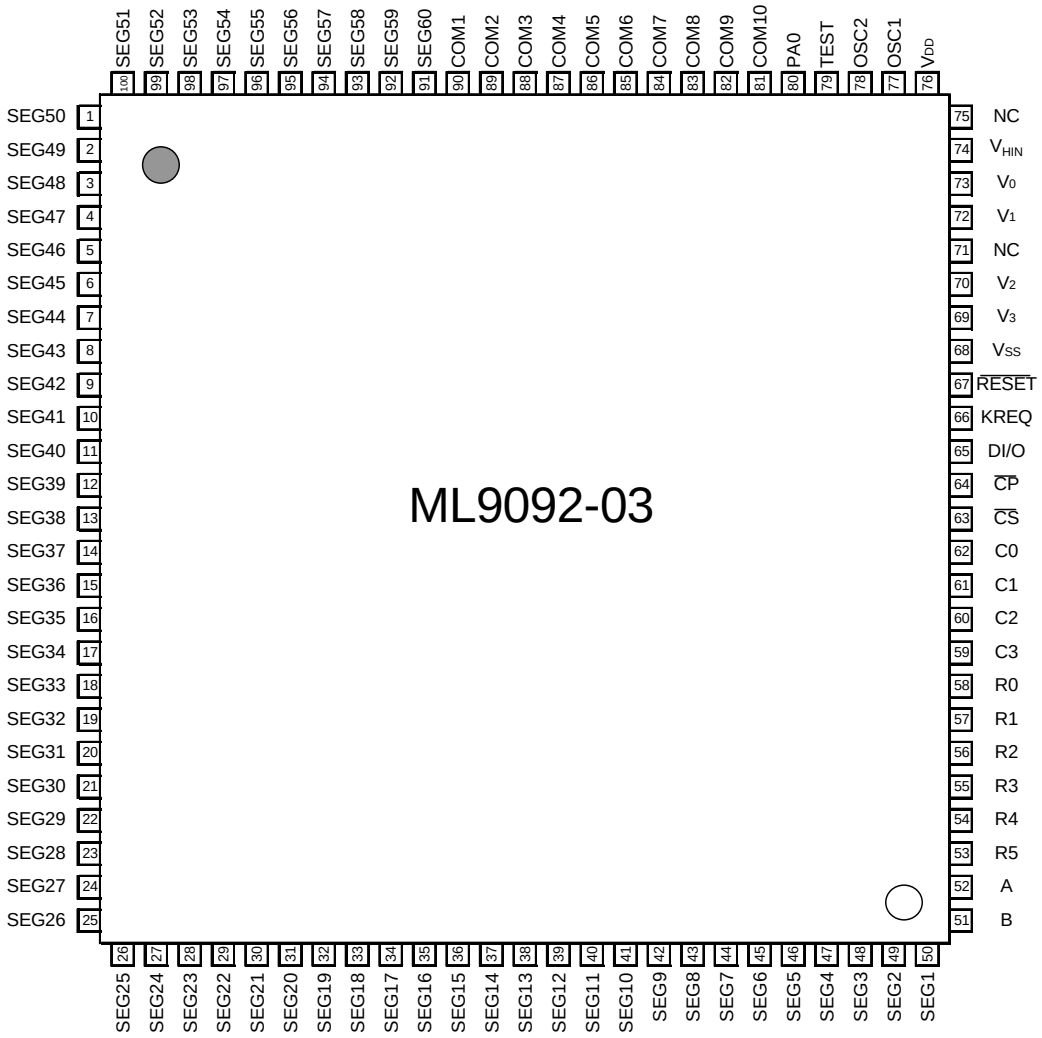
100-Pin Plastic TQFP

ML9092-02



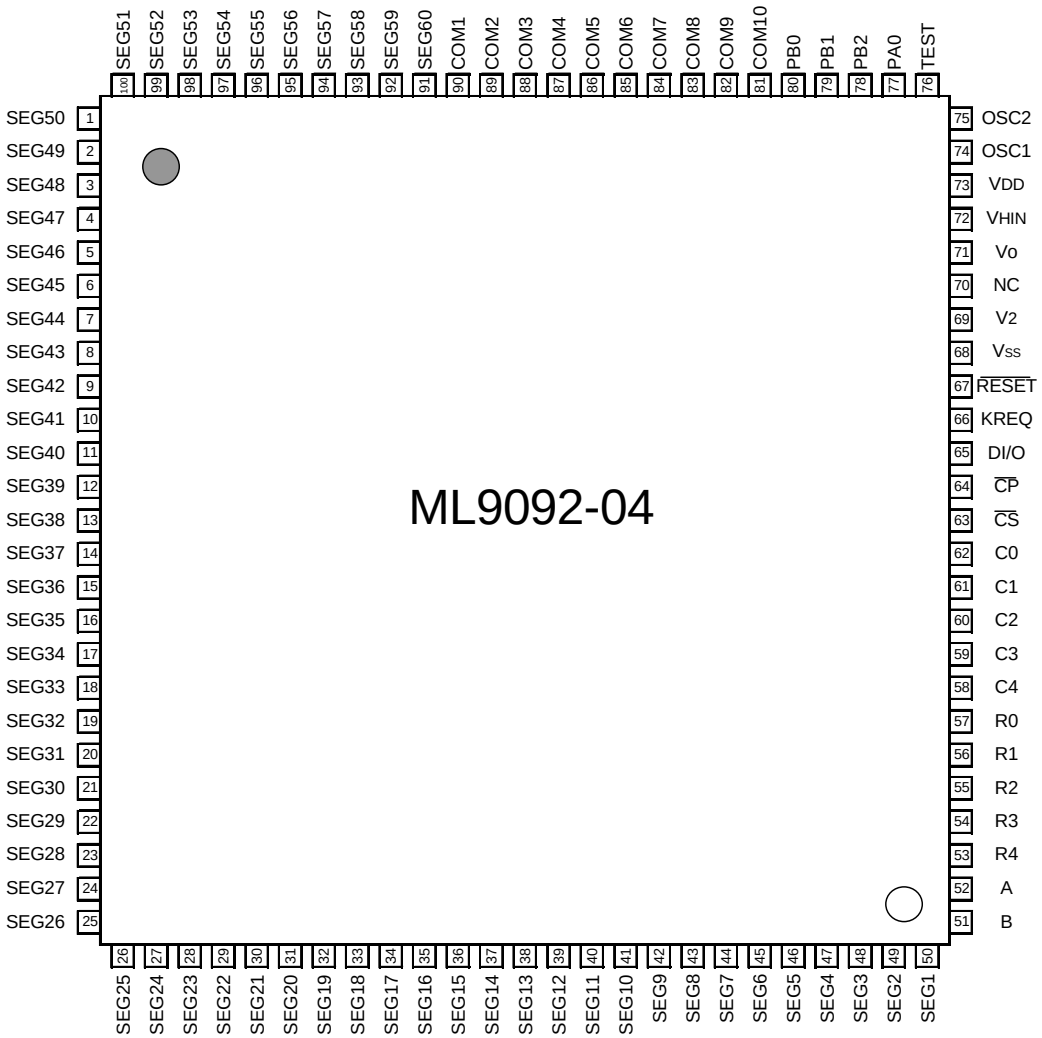
100-Pin Plastic TQFP

ML9092-03



100-Pin Plastic TQFP

ML9092-04



100-Pin Plastic TQFP

FUNCTIONAL DESCRIPTIONS

Pin Functional Descriptions

ML9092-01

Function	Pin	Symbol	Type	Description
CPU interface	63	$\overline{CS}$	I	Chip select signal input pin
	64	$\overline{CP}$	I	Shift clock signal input pin. This pin is connected to the Schmitt circuit internally.
	65	DI/O	I/O	Serial data signal I/O pin. This pin is connected to the Schmitt circuit internally.
	66	KREQ	O	Key scan read and rotary encoder read READY signal output pin.
Oscillation	77	OSC1	I	Connect external resistors with this pin. This pin is connected to the Schmitt circuit internally. If using an external clock, input it from the OSC1 pin and leave the OSC2 pin open.
	78	OSC2	O	
Control signal	67	$\overline{RESET}$	I	Reset input. Initial settings can be established by applying a “L” level to this pin. This pin is connected to the Schmitt circuit internally.
	80	KPS	I	Input pin for switching between key scanning and ports C and D
	79	TEST	I	Test input pin. This pin is connected to the V_{SS} pin.
Switch signal	62–58	C0/D0–C4/D4	I/O	Input pins that detect status of key switches/port D output pins. When used as input pins, these pins are connected to the Schmitt circuit internally.
	57–53	R0/C0–R4/C4	O	Key switch scan signal output pins/port C output pins
	51, 52	A, B	I	Rotary encoder signal input pins. These pins are connected to the Schmitt circuit internally.
Port output	81	PA0	O	Port A output pin
	84–82	PB0–PB2	O	Port B output pins
LCD driver output	50–1 100–95	SEG1–SEG56	O	LCD segment driver output pins
	94–85	COM1–COM10	O	LCD common driver output pins
Power supply	76	V_{DD}	—	Logic power supply pin
	68	V_{SS}	—	GND pin
	75	V_{IN}	—	Voltage doubler reference voltage input pin
	74, 73	$V_{C1}+$, $V_{S1}-$	—	Pins to connect a capacitor for voltage doubler
	72	V_{OUT}	—	Voltage doubler output pin
	71, 69	V_0, V_2	—	LCD bias pins
	70	NC	—	Should be left open.

ML9092-02

Function	Pin	Symbol	Type	Description
CPU interface	63	$\overline{CS}$	I	Chip select signal input pin
	64	$\overline{CP}$	I	Shift clock signal input pin. This pin is connected to the Schmitt circuit internally.
	65	DI/O	I/O	Serial data signal I/O pin. This pin is connected to the Schmitt circuit internally.
	66	KREQ	O	Key scan read and rotary encoder read READY signal output pin.
Oscillation	77	OSC1	I	Connect external resistors with this pin. This pin is connected to the Schmitt circuit internally. If using an external clock, input it from the OSC1 pin and leave the OSC2 pin open.
	78	OSC2	O	
Control signal	67	$\overline{RESET}$	I	Reset input. Initial settings can be established by applying a “L” level to this pin. This pin is connected to the Schmitt circuit internally.
	79	TEST	I	Test input pin. This pin is connected to the V_{SS} pin.
Switch signal	62–59	C0–C3	I	Input pins that detect status of key switches. These pins are connected to the Schmitt circuit internally.
	58–53	R0–R5	O	Key switch scan signal output pins
	51, 52	A, B	I	Rotary encoder signal input pins. These pins are connected to the Schmitt circuit internally.
Port output	80	PA0	O	Port A output pin
LCD driver output	50–1 100–91	SEG1–SEG60	O	LCD segment driver output pins
	90–81	COM1–COM10	O	LCD common driver output pins
Power supply	76	V_{DD}	—	Logic power supply pin
	68	V_{SS}	—	GND pin
	75	V_{IN}	—	Voltage doubler reference voltage input pin
	74, 73	$V_{C1}+$, $V_{S1}-$	—	Pins to connect a capacitor for voltage doubler
	72	V_{OUT}	—	Voltage doubler output pin
	71, 69	V_0, V_2	—	LCD bias pins
	70	NC	—	Should be left open.

ML9092-03

Function	Pin	Symbol	Type	Description
CPU interface	63	$\overline{CS}$	I	Chip select signal input pin
	64	$\overline{CP}$	I	Shift clock signal input pin. This pin is connected to the Schmitt circuit internally.
	65	DI/O	I/O	Serial data signal I/O pin. This pin is connected to the Schmitt circuit internally.
	66	KREQ	O	Key scan read and rotary encoder read READY signal output pin.
Oscillation	77	OSC1	I	Connect external resistors with this pin. This pin is connected to the Schmitt circuit internally. If using an external clock, input it from the OSC1 pin and leave the OSC2 pin open.
	78	OSC2	O	
Control signal	67	$\overline{RESET}$	I	Reset input. Initial settings can be established by applying a “L” level to this pin. This pin is connected to the Schmitt circuit internally.
	79	TEST	I	Test input pin. This pin is connected to the V_{SS} pin.
Switch signal	62–59	C0–C3	I	Input pins that detect status of key switches. These pins are connected to the Schmitt circuit internally.
	58–53	R0–R5	O	Key switch scan signal output pins
	51, 52	A, B	I	Rotary encoder signal input pins. These pins are connected to the Schmitt circuit internally.
Port output	80	PA0	O	Port A output pin
LCD driver output	50–1, 100–91	SEG1–SEG60	O	LCD segment driver output pins
	90–81	COM1–COM10	O	LCD common driver output pins
Power supply	76	V_{DD}	—	Logic power supply pin
	68	V_{SS}	—	GND pin
	74	V_{HIN}	—	High-voltage power supply pin
	73, 72, 70, 69	V_0, V_1, V_2, V_3	—	LCD bias pins
	75, 71	NC	—	Should be left open.

ML9092-04

Function	Pin	Symbol	Type	Description
CPU interface	63	$\overline{CS}$	I	Chip select signal input pin
	64	$\overline{CP}$	I	Shift clock signal input pin. This pin is connected to the Schmitt circuit internally.
	65	DI/O	I/O	Serial data signal I/O pin. This pin is connected to the Schmitt circuit internally.
	66	KREQ	O	Key scan read and rotary encoder read READY signal output pin.
Oscillation	74	OSC1	I	Connect external resistors with this pin. This pin is connected to the Schmitt circuit internally. If using an external clock, input it from the OSC1 pin and leave the OSC2 pin open.
	75	OSC2	O	
Control signal	67	$\overline{RESET}$	I	Reset input. Initial settings can be established by applying a “L” level to this pin. This pin is connected to the Schmitt circuit internally.
	76	TEST	I	Test input pin. This pin is connected to the V_{SS} pin.
Switch signal	62–58	C0–C4	I	Input pins that detect status of key switches. These pins are connected to the Schmitt circuit internally.
	57–53	R0–R4	O	Key switch scan signal output pins
	51, 52	A, B	I	Rotary encoder signal input pins. These pins are connected to the Schmitt circuit internally.
Port output	77	PA0	O	Port A output pin
	80–78	PB0–PB2		Port B output pins
LCD driver output	50–1, 100–91	SEG1–SEG60	O	LCD segment driver output pins
	90–81	COM1–COM10	O	LCD common driver output pins
Power supply	73	V_{DD}	—	Logic power supply pin
	68	V_{SS}	—	GND pin
	72	V_{HIN}	—	High-voltage power supply pin
	71, 69	V_0, V_2	—	LCD bias pins
	70	NC	—	Should be left open.

- $\overline{CS}$

Chip select input pin. A Schmitt circuit is internally connected to this pin. An "L" level selects the chip, and an "H" level does not select the chip. During the "L" level, internal registers can be accessed.

- $\overline{CP}$

Clock input pin for serial interface data I/O. A Schmitt circuit is internally connected to this pin. Data input to the DI/O pin is synchronized to the rising edge of the clock. Output from the DI/O pin is synchronized to the falling edge of the clock.

- **DI/O**

Serial interface data I/O pin. A Schmitt circuit is internally connected to this pin. This pin is in the output state only during the interval beginning when commands for key scan data read, RAM read or rotary encoder are written until the $\overline{CS}$ signal rises. At all other times this pin is in the input state. (When reset, the input state is set.) The relation between data level of this pin and operation is listed below.

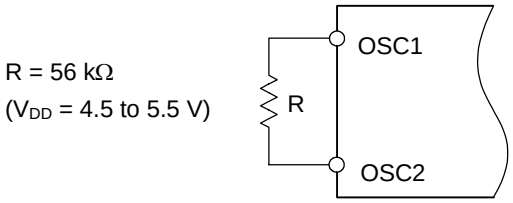
Data level	LCD display	Key status	Rotary switch
"H"	Light ON	ON	Count value
"L"	Light OFF	OFF	Count value

- **KREQ**

Key scan read and rotary encoder read READY signal output pin.

- **OSC1**

Input pin for RC oscillation. A Schmitt circuit is internally connected to this pin. An oscillation circuit is configured by connecting this pin and OSC2 with a resistor (R) placed across the connection (see figure below). Make the wiring between this pin and the resistor as short as possible. If an external master oscillation clock is to be input, input the master oscillation clock to this pin.



- **OSC2**

Output pin for RC oscillation. A Schmitt circuit is internally connected to this pin. An oscillation circuit is configured by connecting this pin and OSC1 with a resistor (R) placed across the connection (see figure above). Make the wiring between this pin and the resistor as short as possible. If an external master oscillation clock is to be input, leave this pin unconnected (open).

- $\overline{RESET}$

Reset signal input pin. A Schmitt circuit is internally connected to this pin. The initial state can be set by pulling this pin to an "L" level. Refer to the "Output, I/O and Register States in Response to Reset Input" page for the initial states of each register and display.
An internal pull-up resistor is connected to this pin. Connecting an external capacitor enables power-on reset.

- **TEST**

Test signal input pin. Connect this pin to V_{SS}.

- **R0/C0 to R4/C4 (ML9092-01), R0 to R5 (ML9092-02/03), R0 to R4 (ML9092-04)**

Key switch scan signal output pins. During the scan operation, "L" level signals are output in the order of R0/C0, R1/C1, ..., R4/C4 (ML9092-01) or R0, R1, ..., R5 (ML9092-02/03) or R0, R1, ..., R4 (ML9092-04). (Refer to the description under the heading "Key scan" for details.) For the ML9092-01, R0 to R4 can be used as the output ports for the general-purpose port C depending on the input signal to the KPS pin.

- **C0/D0 to C4/D4 (ML9092-01), C0 to C3 (ML9092-02/03), C0 to C4 (ML9092-04)**

Input pins that detect the key switch status. Pull-up resistors and a Schmitt circuit are internally connected to these pins. Assemble a key matrix between these pins and the R0/C0 to R4/C4 (ML9092-01) or R0 to R5 (ML9092-02/03) or R0 to R4 (ML9092-04) pins. For the ML9092-01, C0 to C4 can be used as the output ports for the general-purpose port D depending on the input signal to the KPS pin.

- **KPS**

Input pin that selects whether the R0/C0 to R4/C4 pins and C0/D0 to C4/D4 pins are used to detect the key switch status or whether they are used as the output pins for the general-purpose ports C and D. When this pin is pulled to a "H" level, the R0/C0 to R4/C4 pins and C0/D0 to C4/D4 pins function as pins that detect the key switch status. When this pin is pulled to a "L" level, it functions as the output pin for the general-purpose ports C and D. This pin must be fixed at either a "H" or "L" level.
This pin is provided only for the ML9092-01.

- **A, B**

Input pins for encoder format rotary switches. A Schmitt circuit is internally connected to these pins. When turning the rotary switch clockwise, input to the A pin a signal more advancing in phase than the B pin. When turning the rotary switch counterclockwise, input to the B pin a signal more advancing in phase than the A pin.

- **PA0**

General-purpose port A output pin. This pin can output a current of –15 mA. If this pin is used to drive an LED, insert an external current limiting resistor in series with the LED. If this pin is not used, leave it unconnected (open).

- **PB0 to PB2**

Port B pins, which are used for PWM outputs. These pins are provided for the ML9092-01/04. Any pins not to be used should be left unconnected (open).

- **SEG1 to SEG60(56)**

Segment signal output pins for LCD driving. Any pins not to be used should be left unconnected (open). For the ML9092-01, only SEG1 to SEG56 apply.

- **COM1 to COM10**

Common signal output pins for LCD driving. Any pins not to be used should be left unconnected (open).

- **V_{DD}**

Logic power supply connection pin.

- **V_{SS}**

Power supply GND connection pin.

- **V_{IN}**

Voltage doubler reference voltage input pin. A voltage twice that which is input to this pin is output to the V_{OUT} pin. When the voltage doubler is not used, connect this pin to GND.
This pin is provided for the ML9092-01/02.

- **$V_{S1}-$**

Negative connection pin for the capacitor for the voltage doubler. Connect a 4.7 μF (±30%) capacitor between this pin and the $V_{C1}+$ pin. When the voltage doubler is not used, leave this pin unconnected (open).
This pin is provided for the ML9092-01/02.

- **$V_{C1}+$**

Positive connection pin for the capacitor for the voltage doubler. Connect a 4.7 μF (±30%) capacitor between this pin and the $V_{S1}-$ pin. When the voltage doubler is not used, leave this pin unconnected (open).
This pin is provided for the ML9092-01/02.

- **V_{OUT}**

A voltage twice that which is input to the V_{IN} pin is output to this pin. Connect a 4.7 μF capacitor between this pin and the V_{SS} pin. When the internal voltage doubler is not used, input the specified voltage to this pin from the outside. When built-in contrast adjustment (electronic volume) is used, leave the connection between this pin and the V_0 pin open. The LCD drive voltage will be output from the V_0 pin according to the contrast adjustment value. When built-in contrast adjustment is not used, connect this pin with the V_0 pin.
This pin is provided for the ML9092-01/02.

- **V_0, V_2**

LCD bias pins. A bias dividing resistor is connected to these pins.
These pins are provided for the ML9092-01/02/04.

- **V_{HIN}**

LCD drive high voltage power supply connection pin. When built-in contrast adjustment (electronic volume) is used, input the LCD drive power supply voltage to this pin. The LCD drive voltage will be output from the V_0 pin according to the contrast adjustment value. When built-in contrast adjustment is not used, strap the V_{HIN} pin and V_0 pin outside the IC, and input the LCD drive voltage into both pins.
This pin is provided for the ML9092-03/04.

- **V_0, V_1, V_2, V_3**

LCD bias pins. A bias dividing resistor is connected to these pins. When using a large-screen LCD, however, input the LCD bias voltage from outside the IC to these pins.
This is applicable to the ML9092-03.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V	V_{DD}
High Power Supply Voltage	V_H	Ta = 25°C	–0.3 to +18.0	V	V_{OUT}, V_{HIN}
Bias Voltage	V_{BI}	Ta = 25°C	–0.3 to V_{OUT} (V_{HIN}) + 0.3	V	V_{C1}+, V_0, V_1, V_2, V_3
Voltage Doubler Reference Voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	V_{IN}
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	$\overline{CS}$, $\overline{CP}$, DI/O, OSC1, C0 to C3, C0 to C4, C0/D0 to C4/D4, KPS, A, B, $\overline{RESET}$
Output Current	I_O	Ta = 25°C	–20 to +3	mA	PA0
		Ta = 25°C	–3 to +4	mA	PB0 to PB2, R0/C0 to R4/C4, C0/D0 to C4/D4, R0 to R4, R0 to R5, DI/O, KREQ
Power Dissipation	P_D	Ta = 85°C	190	mW	—
Storage Temperature	T_{stg}	—	–55 to +150	°C	—

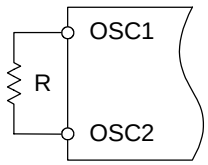
V_{SS} is the reference voltage potential for all pins.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	—	4.5 to 5.5	V	V_{DD}
Externally Input Power Supply Voltage 1 (Applies to ML9092-01/02)	V_{OUT}	Voltage doubler not used (Contrast adjustment used)	4.5 to 16.5	V	V_{OUT}
		Voltage doubler not used & V_{OUT} pin connected with V_0 pin (Contrast adjustment not used)	4.0 to 16.5	V	V_{OUT}, V_0
Externally Input Power Supply Voltage 2 (Applies to ML9092-03/04)	V_{HIN}	Contrast adjustment used	4.5 to 16.5	V	V_{HIN}
		Contrast adjustment not used (V_{HIN} pin connected with V_0 pin)	4.0 to 16.5	V	V_{HIN}, V_0
Bias Voltage	V_0	—	4.0 to 16.5	V	V_0
Voltage Doubler Input Voltage	V_{IN}	—	$0.8V_{DD}$ to V_{DD}	V	V_{IN}
Operating Frequency of External Clock	f_{OPE}	—	210 to 445	kHz	OSC1
Oscillation Resistance	R	V_{DD} = 4.5 to 5.5 V	56[*1]	kΩ	OSC1, OSC2
Operating Temperature	T_{op}	—	–40 to +85	°C	—

V_{SS} is the reference voltage potential for all pins.

*1: Use a resistor with an accuracy of ±2 %



ELECTRICAL CHARACTERISTICS

Oscillating Frequency Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Oscillating Frequency	f_{OSC}	56 kΩ (resistor with accuracy within ±2%)	210	306	445	kHz	OSC1, OSC2

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
"H" Input Voltage 1	V_{IH1}	When input externally	$0.85V_{DD}$	—	—	V	OSC1
"H" Input Voltage 2	V_{IH2}	—	$0.85V_{DD}$	—	—	V	$\overline{RESET}$
"H" Input Voltage 3	V_{IH3}	—	$0.85V_{DD}$	—	—	V	$\overline{CP}$, A, B, C0–C3, C0/D0–C4/D4,C0–C4 $\overline{CS}$, DI/O
"H" Input Voltage 4	V_{IH4}	—	$0.8V_{DD}$	—	—	V	KPS
"L" Input Voltage 1	V_{IL1}	When input externally	—	—	$0.15V_{DD}$	V	OSC1
"L" Input Voltage 2	V_{IL2}	—	—	—	$0.15V_{DD}$	V	$\overline{RESET}$
"L" Input Voltage 3	V_{IL3}	—	—	—	$0.15V_{DD}$	V	$\overline{CP}$, A , B, $\overline{CS}$, DI/O,
"L" Input Voltage 4	V_{IL4}	—	—	—	$0.2V_{DD}$	V	KPS
"L" Input Voltage 5	V_{IL5}	—	—	—	$0.23V_{DD}$	V	C0/D0–C4/D4,C0–C3, C0–C4
"H" Input Current 1	I_{IH1}	$V_I = V_{DD}$	—	—	10	µA	$\overline{RESET}$
"H" Input Current 2	I_{IH2}	$V_I = V_{DD}$	—	—	10	µA	C0/D0–C4/D4, C0–C3, C0–C4
"H" Input Current 3	I_{IH3}	DI/O = Input mode, All ports = HiZ, $V_I = V_{DD}$	—	—	10	µA	DI/O, PA0, PB0–PB2, R0/C0–R4/C4, C0/D0–C4/D4
"H" Input Current 4	I_{IH4}	$V_I = V_{DD}$	—	—	1	µA	OSC1, $\overline{CS}$, $\overline{CP}$, KPS , A , B
"L" Input Current 1	I_{IL1}	V_{DD} = 5 V, V_I = 0 V	–0.1	–0.05	–0.02	mA	$\overline{RESET}$
"L" Input Current 2	I_{IL2}	V_{DD} = 5 V, V_I = 0 V	–0.9	–0.45	–0.18	mA	C0/D0–C4/D4, C0–C3,C0–C4
"L" Input Current 3	I_{IL3}	DI/O = Input mode, All ports = HiZ, V_I = 0 V	–10	—	—	µA	DI/O, PA0, PB0–PB2, R0/C0–R4/C4, C0/D–C4/D4
"L" Input Current 4	I_{IL4}	V_I = 0 V	–1	—	—	µA	OSC1, $\overline{CS}$, $\overline{CP}$, KPS, A, B

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
"H" Output Voltage 1	V_{OH1}	I_O = –0.4 mA	V_{DD} – 0.4	—	—	V	DI/O, KREQ
"H" Output Voltage 2	V_{OH2}	I_O = –40 µA	$0.9V_{DD}$	—	—	V	OSC2
"H" Output Voltage 3	V_{OH3}	I_O = –15 mA	V_{DD} – 1.7	—	—	V	PA0
"H" Output Voltage 4	V_{OH4}	I_O = –2 mA (When R0/C0–R4/C4 and C0/D0–C4/D4 are used as ports C and D)	V_{DD} – 1.2	—	—	V	Only applies to ML9092-01. PB0–PB2, R0/C0–R4/C4, C0/D0–C4/D4
"H" Output Voltage 5	V_{OH5}	I_O = –50 µA (When R0/C0–R4/C4 are used for key scanning)	V_{DD} – 2.0	—	—	V	R0/C0–R4/C4(-01), R0–R5 (-02, -03) R0–R4 (-04)
"L" Output Voltage 1	V_{OL1}	I_O = 0.4 mA	—	—	0.4	V	DI/O, KREQ
"L" Output Voltage 2	V_{OL2}	I_O = 40 µA	—	—	$0.1V_{DD}$	V	OSC2
"L" Output Voltage 3	V_{OL3}	I_O = 1 mA (When R0/C0–R4/C4 and C0/D0–C4/D4 are used as ports C and D)	—	—	0.4	V	PA0, PB0–PB2, C0/D0–C4/D4, R0/C0–R4/C4
"L" Output Voltage 4	V_{OL4}	I_O = 2.7 mA (When R0/C0–R4/C4 are used for key scanning)	—	—	0.3	V	R0/C–R4/C4 (-01), R0–R5 (-02, -03) R0–R4 (-04)

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Segment Output Voltage 2 (1/5 bias)	V_{OS0}	I_O = –10 µA	V_0 – 0.6	—	—	V	SEG1–SEG56 (SEG60 for ML9092-02/03 /04)
	V_{OS1}	I_O = ±10 µA	2/4V_0 – 0.6	—	2/4V_0 + 0.6	V	
	V_{OS2}	I_O = ±10 µA	2/4V_0 – 0.6	—	2/4V_0 + 0.6	V	
	V_{OS3}	I_O = +10 µA	—	—	V_{SS} + 0.6	V	
Common Output Voltage 1 (1/4 bias)	V_{OC0}	I_O = –10 µA	V_0 – 0.3	—	—	V	COM1–COM10
	V_{OC1}	I_O = ±10 µA	3/4V_0 – 0.3	—	3/4V_0 + 0.3	V	
	V_{OC2}	I_O = ±10 µA	1/4V_0 – 0.3	—	1/4V_0 + 0.3	V	
	V_{OC3}	I_O = +10 µA	—	—	V_{SS} + 0.3	V	
Supply Current 1 (Applies to ML9092-01/02)	I_{DD1}	R = 56 kΩ Voltage doubler operating, No load *1	—	—	0.6	mA	V_{DD}
Supply Current 2 (Applies to ML9092-01/02)	I_{DD2}	External clock = 445 kHz Voltage doubler operating, No load *2	—	—	0.6	mA	V_{DD}
Supply Current 3 (Applies to ML9092-01/02)	I_{VIN}	External clock = 445 kHz Voltage doubler operating, No load *2	—	—	2	mA	V_{IN}
Supply Current 4 (Applies to ML9092-01/02)	I_{VHIN1}	External clock = 445 kHz Voltage doubler not operating, No load *3	—	—	1	mA	V_{OUT}
Supply Current 5 (Applies to ML9092-03/04)	I_{DD3}	R = 56 kΩ No load *4	—	—	0.6	mA	V_{DD}
Supply Current 6 (Applies to ML9092-03/04)	I_{DD4}	External clock = 445 kHz No load *5	—	—	0.6	mA	V_{DD}
Supply Current 7 (Applies to ML9092-03/04)	I_{VHIN2}	External clock = 445 kHz No load *5	—	—	1	mA	V_{HIN}
Supply Current 8 (Applies to ML9092-03/04)	I_{DD5}	R = 56 kΩ Voltage doubler not operating, No load *6	—	—	100	µA	V_{DD}

*1: Refer to the Current Measuring Circuit 1.
*2: Refer to the Current Measuring Circuit 2.
*3: Refer to the Current Measuring Circuit 3.
*4: Refer to the Current Measuring Circuit 4.
*5: Refer to the Current Measuring Circuit 5.
*6: Refer to the Current Measuring Circuit 6.

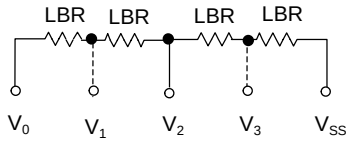
(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Voltage doubler Voltage	V_{DB}	External clock = 210 kHz V_{IN} = 0.8 V_{DD} to V_{DD} (*1)	$V_{IN} \times 1.9 - 0.5$	9.8 *3	$V_{IN} \times 2$	V	V_{OUT}
LCD driving voltage when internal variable resistor is used	V_{LCDMAX}	V_{DD} = 5 V, V_{OUT} = 10 V (Voltage doubler not operating, but voltage applied externally) Contrast data = FH, No load	9.5	9.8	10	V	$V_0 - V_{SS}$
	V_{LCDMIN}	V_{DD} = 5 V, V_{OUT} = 10 V (Voltage doubler not operating, but voltage applied externally) Contrast data = 0H, No load	6.7	7	7.3	V	
LCD Driving Bias Resistance	LBR	(*2)	5	9	14	kΩ	$V_0 - V_{ss}$

*1 Refer to the Voltage Doubler Voltage Measuring Circuit.

*3 V_{IN} = 5 V, Ta = 25°C

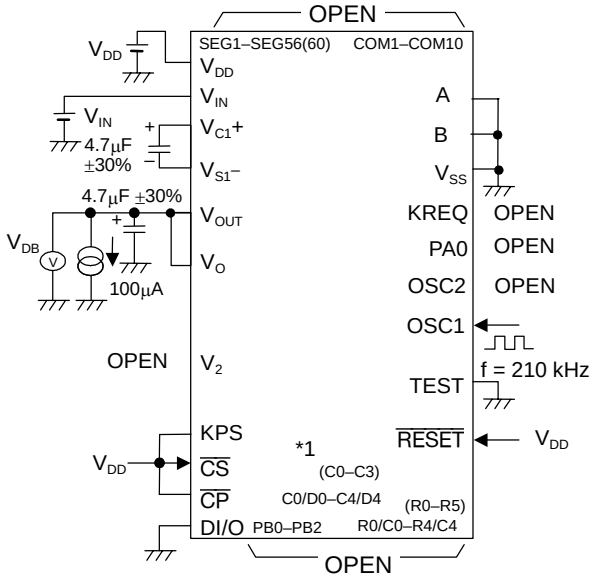
*2



Measuring Circuits

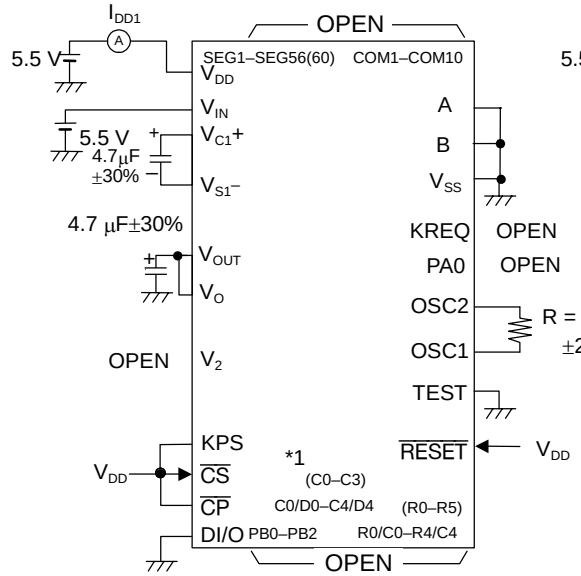
Voltage Doubler Voltage Measuring Circuit

Voltage is doubled
(1/4 bias)



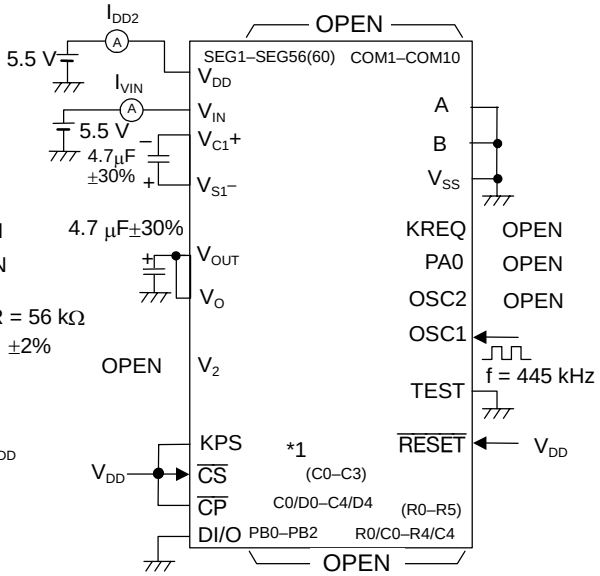
Current Measuring Circuit 1

Voltage is doubled (internal oscillation)



Current Measuring Circuit 2

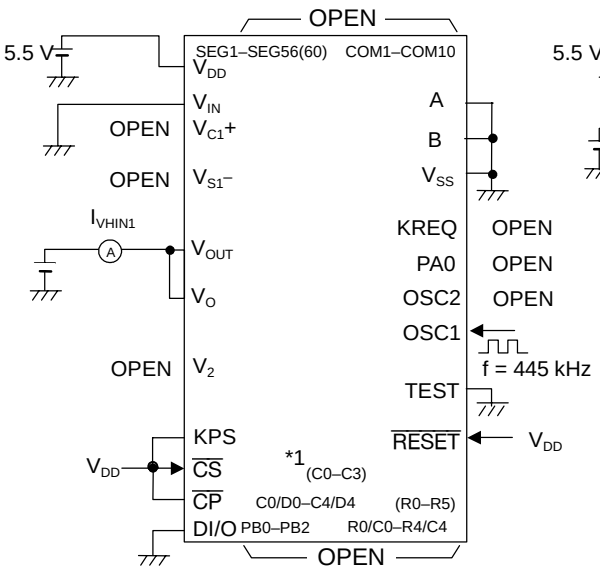
Voltage is doubled (external clock)



*1: For ML9092-01, these are SEG1–56, PB0–PB2, KPS, C0/D0–C4/D4, and R0/C0–R4/C4.
For ML9092-02, these are SEG1–60, C0–C3, and R0–R5; PB0–PB2 and KPS are not provided.

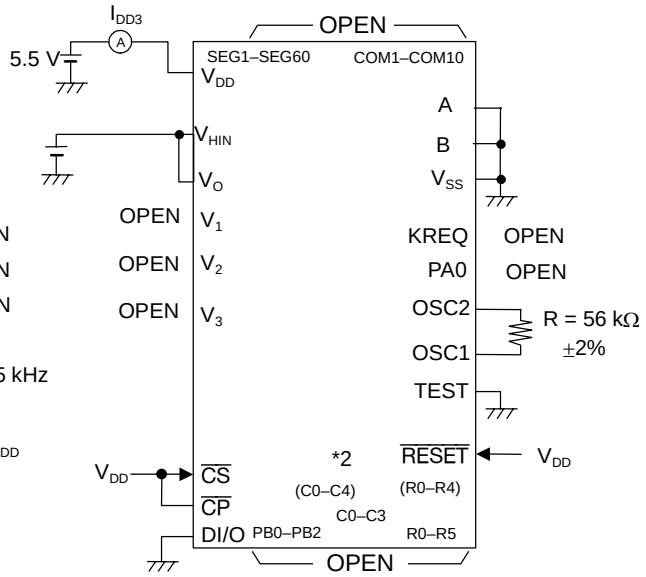
Current Measuring Circuit 3

External LCD voltage applied
(External clock)



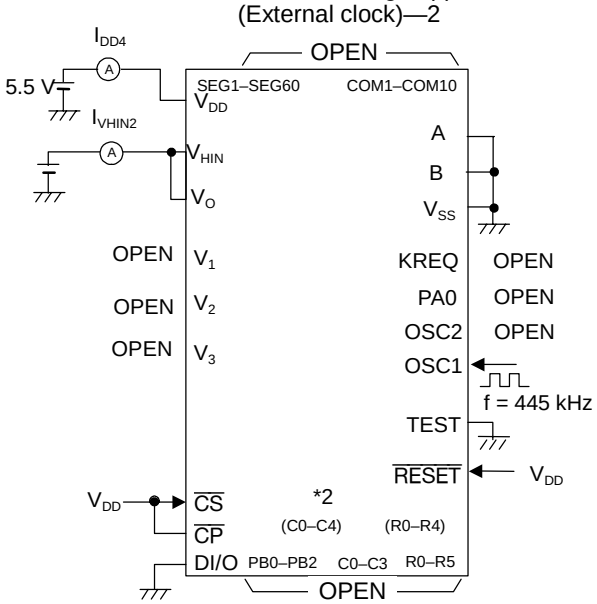
Current Measuring Circuit 4

External LCD voltage applied
(Internal oscillation)



Current Measuring Circuit 5

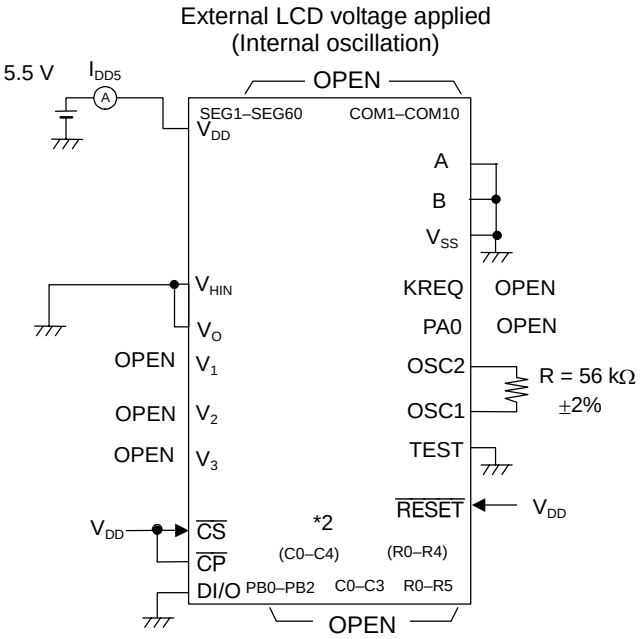
External LCD voltage applied
(External clock)—2



*1: For ML9092-01, these are SEG1–56, PB0–PB2, KPS, C0/D0–C4/D4, and R0/C0–R4/C4.
For ML9092-02, these are SEG1–60, C0–C3, and R0–R5; PB0–PB2 and KPS are not provided.

*2: For ML9092-03, these are C0–C3 and R0–R5; PB0–PB2 are not provided.
For ML9092-04, these are C0–C4 and R0–R4; PB0–PB2 are provided.

Current Measuring Circuit 6



*2: For ML9092-03, these are C0–C3 and R0–R5; PB0–PB2 are not provided.
For ML9092-04, these are C0–C4 and R0–R4; PB0–PB2 are provided.

Switching Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{CP}$ Clock Cycle Time	t_{SYS}	—	500	—	ns
$\overline{CP}$ "H" Pulse Width	t_{WH}	—	200	—	ns
$\overline{CP}$ "L" Pulse Width	t_{WL}	—	200	—	ns
$\overline{CS}$ "H" Pulse Width	t_{WCH}	—	100	—	ns
$\overline{CP}$ Clock Rise/fall Time	t_r, t_f	—	—	50	ns
$\overline{CS}$ Setup Time	t_{CSU}	—	30	—	ns
$\overline{CS}$ Hold Time	t_{CHD}	—	150	—	ns
DI/O Setup Time	t_{DSU}	—	50	—	ns
DI/O Hold Time	t_{DHD}	—	50	—	ns
DI/O Output Delay Time	t_{DOD}	CL = 50 pF	—	100	ns
DI/O Output OFF Delay Time	t_{DOFF}	CL = 50 pF	—	100	ns
$\overline{RESET}$ Pulse Width	t_{WRE}	—	2	—	µs
External Clock Cycle Time	t_{SES}	—	1612	3389	ns
External Clock "H" Pulse Width	t_{WEH}	—	645	—	ns
External Clock "L" Pulse Width	t_{WEL}	—	645	—	ns
External Clock Rise/fall Time	t_{rE}, t_{fE}	—	—	50	ns

Key Scan Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Register setting	Dividing ratio	Oscillation frequency			Unit
		KT		210 kHz	306kHz	445 kHz	
Key Scan Period	T_{scn}	0	1/1536	7.3	5.0	3.5	ms
		1	1/3072	14.6	10.0	6.9	

Frame Frequency, PWM Frequency, and Voltage Doubler Frequency Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

Model	Parameter	Symbol	Display duty	Dividing ratio	Oscillation frequency			Unit
					210 kHz	306 kHz	445 kHz	
ML9092-01/02/03/04	Frame Frequency	FRM	1/8	1/2560	82	120	174	Hz
			1/9	1/2520	83	121	177	
			1/10	1/2560	82	120	174	
ML9092-01/04	PWM Frequency	PWM	—	1/1020	205	300	436	
ML9092-01/02	Voltage Doubler Frequency	—	—	1/64	3281	4781	6953	

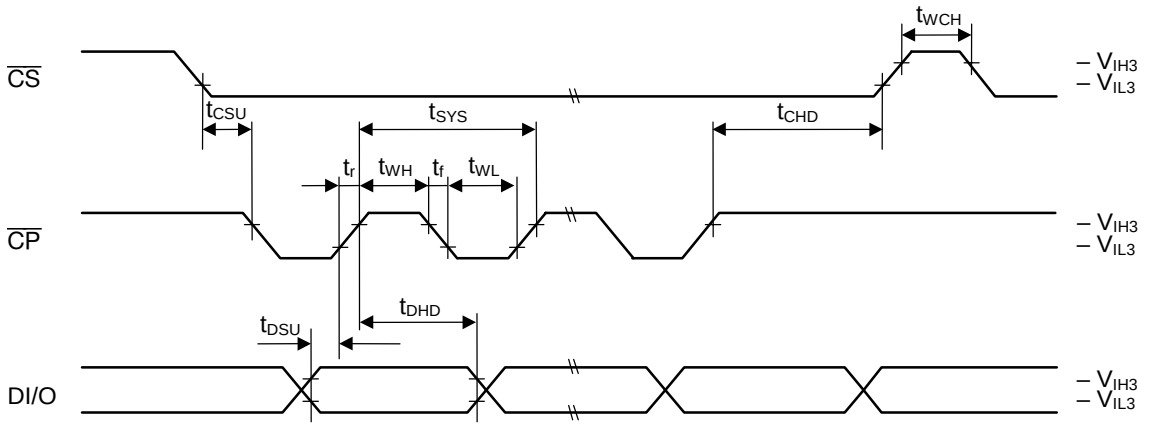
Switching Characteristics of Rotary Switch

(V_{DD} = 4.5 to 5.5 V, V_{OUT} (V_{HIN}) = 4.5 to 16.5 V, Ta = –40 to +85°C)

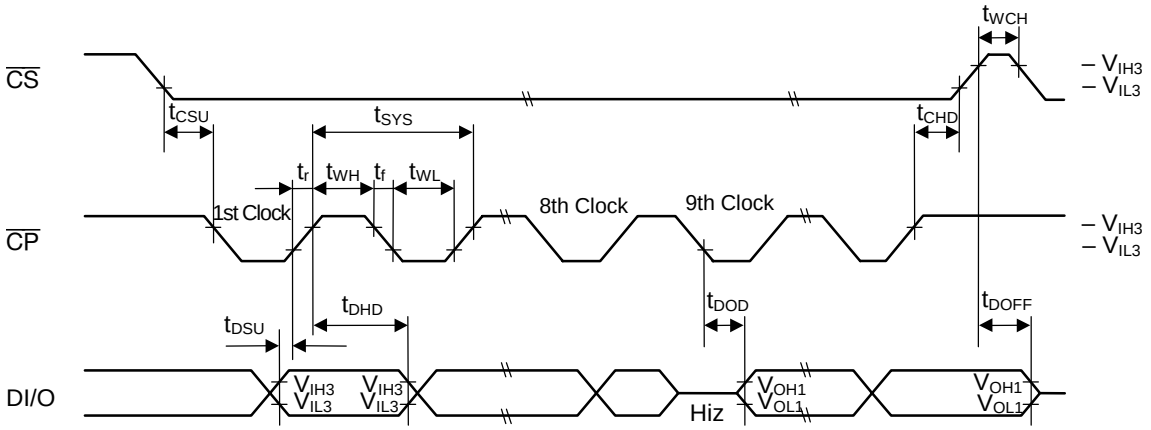
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Phase Recognition Time (A to B)	t_{SAW}	R = 56 kΩ ±2%,	950	—	—	µs
Phase Recognition Time (B to A)	t_{SBW}		950	—	—	µs
Phase Input Fixed Time	t_{AB}		950	—	—	µs

Clock synchronous serial interface timing diagrams

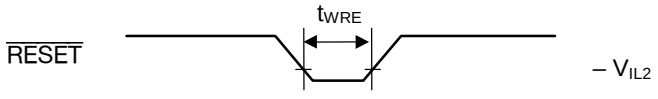
Clock synchronous serial interface input timing



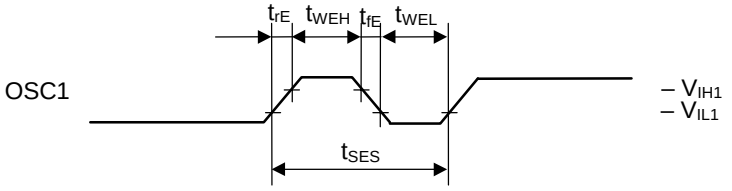
Clock synchronous serial interface input→output timing



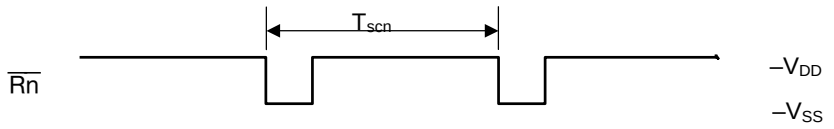
Reset timing



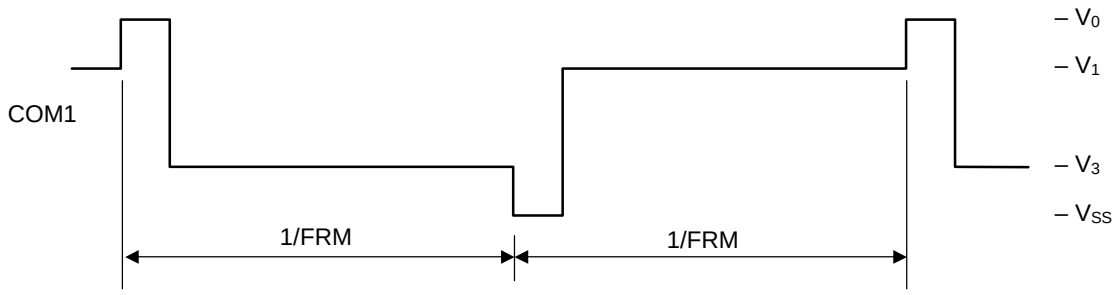
External clock



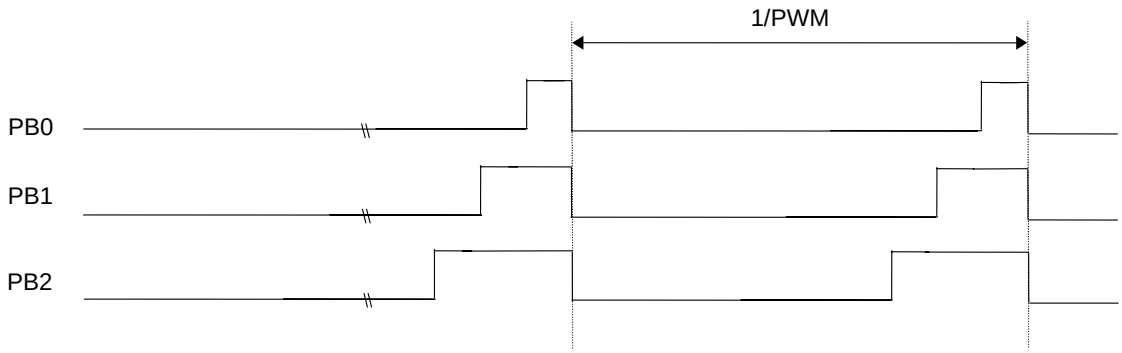
Key scan timing



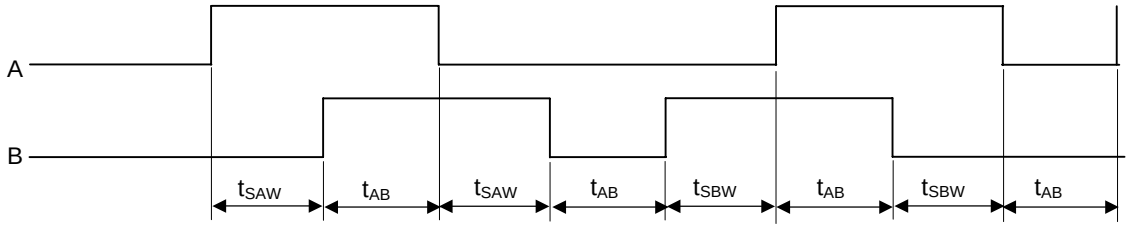
Frame frequency



PWM output frequency for port B (applies to ML9092-01/04)



Rotary switch input timing



Instruction Code List (ML9092-01)

No.	Instruction	Instruction Code								Data								Description
		Fixed bit		R/W	Register No.													
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
0	Key scan register read	1	1	1	0	0	0	0	0	ST2	ST1	ST0	S4	S3	S2	S1	S0	Reads scan read timing bits (ST0 to ST2) and key scan data (S0 to S4) of the key scan register.
1	Display data RAM write	1	1	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Writes display data (D0 to D7) in the display data RAM after setting the X address of Y address.
1	Display data RAM read	1	1	1	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Reads display data (D0 to D7) from the display data RAM after setting the X address of Y address.
2	X address register set	1	1	0	0	0	0	1	0	–	–	–	–	X3	X2	X1	X0	Sets the X address (X0 to X3) of the display data RAM.
3	Y address register set	1	1	0	0	0	0	1	1	–	–	–	–	Y3	Y2	Y1	Y0	Sets the Y address (Y0 to Y3) of the display data RAM.
4	Port register A set	1	1	0	0	0	1	0	0	–	–	–	–	–	–	–	PTA0	Controls the output of the general-purpose port A (PTA0).
5	Port register B set	1	1	0	0	0	1	0	1	–	–	–	–	–	PTB2	PTB1	PTB0	Controls the output of the general-purpose port B (PTB0 to PTB2).
6	Port register C set	1	1	0	0	0	1	1	0	–	–	–	PTC4	PTC3	PTC2	PTC1	PTC0	Controls the output of the general-purpose port C (PTC0 to PTC4).
7	Port register D set	1	1	0	0	0	1	1	1	–	–	–	PTD4	PTD3	PTD2	PTD1	PTD0	Controls the output of the general-purpose port D (PTD0 to PTD4).
8	Control register 1 set	1	1	0	0	1	0	0	0	INC	WLS	KT	SHL	BE	PE	DTY1	DTY0	Sets the address increment X or Y direction (INC), display data word length (WLS), key scan time (KT), common driver shift direction (SHL), voltage doubler control (BE), port control (PE), and display duty (DTY0, DTY1).
9	Control register 2 set	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	DISP	Sets display ON/OFF (DISP).
A	Rotary encoder read	1	1	1	0	1	0	1	0	Q4	Q4	Q4	Q4	Q4	Q3	Q2	Q1	Reads the counter bits (Q1 to Q4) of the rotary encoder.
B	Contrast ADJ set	1	1	0	0	1	0	1	1	–	–	–	–	CT3	CT2	CT1	CT0	Sets contrast adjustment values with the contrast adjustment bits (CT0 to CT3).
C	PWM0 register set	1	1	0	0	1	1	0	0	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	Sets the pulse width to be output from general-purpose port B (PTB0) with the bits (PW00 to PW07) of PWM0.
D	PWM1 register set	1	1	0	0	1	1	0	1	PW17	PW16	PW15	PW14	PW13	PW12	PW11	PW10	Sets the pulse width to be output from general-purpose port B (PTB1) with the bits (PW10 to PW17) of PWM1.
E	PWM2 register set	1	1	0	0	1	1	1	0	PW27	PW26	PW25	PW24	PW23	PW22	PW21	PW20	Sets the pulse width to be output from general-purpose port B (PTB2) with the bits (PW20 to PW27) of PWM2.
F	Test register set	1	1	0	0	1	1	1	1	–	–	–	T5	T4	T3	T2	T1	Test instruction exclusively used by manufacturer (T1 to T5). Customers must not use this instruction.

Notes:

R/W : Read/write select bit 1:Read, 0: Write
ST0 to ST2 : Key scan read count display bits
S0 to S4 : Key scan data
D0 to D7 : Write or read data of the display data RAM
X0 to X3 : X addresses of the display data RAM
Y0 to Y3 : Y addresses of the display data RAM
PTA0 : Port A data
PTB0 to PTB2 : Port B output control 1: Output enable, 0: Fixed at "L"
PTC0 to PTC4 : Port C data
PTD0 to PTD4 : Port D data
INC : Display data RAM address increment. 1: X direction, 0: Y direction
WLS : Word length select bit 1: 6 bits, 0: 8 bits
KT : Key scan period select bit 1: 10 ms, 0: 0.5 ms
SHL : Common driver shift direction select bit
1: COM10→COM1, 0: COM1→COM10
BE : Voltage doubler control bit 1: Voltage doubler enable
0: Voltage doubler disable

PE : Port enable/disable select bit 1: All ports enable
0: All ports go into high impedance for output
DTY0, DTY1 : Display duty select bits (1/8, 1/9, 1/10)
DISP : Display ON/OFF select bit 1: Display ON, 0: Display OFF
Q1 to Q4 : Rotary encoder switch count bits (2's complement)
CT0 to CT3 : Contrast adjustment bit
PW00 to PW07 : PWM0 setting bits
PW10 to PW17 : PWM1 setting bits
PW20 to PW2 : PWM2 setting bits
T1 to T5 : Bits for test instruction. Customers should not access these bits.

– : Don't Care

Instruction Code List (ML9092-02/03)

No.	Instruction	Instruction Code								Data								Description
		Fixed bit		R/W	Register No.													
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
0	Key scan register read	1	1	1	0	0	0	0	0	ST2	ST1	ST0	0	S3	S2	S1	S0	Reads scan read timing bits (ST0 to ST2) and key scan data (S0 to S4) of the key scan register.
1	Display data RAM write	1	1	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Writes display data (D0 to D7) in the display data RAM after setting the X address of Y address.
1	Display data RAM read	1	1	1	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Reads display data (D0 to D7) from the display data RAM after setting the X address of Y address.
2	X address register set	1	1	0	0	0	0	1	0	–	–	–	–	X3	X2	X1	X0	Sets the X address (X0 to X3) of the display data RAM.
3	Y address register set	1	1	0	0	0	0	1	1	–	–	–	–	Y3	Y2	Y1	Y0	Sets the Y address (Y0 to Y3) of the display data RAM.
4	Port register A set	1	1	0	0	0	1	0	0	–	–	–	–	–	–	–	PTA0	Controls the output of the general-purpose port A (PTA0).
8	Control register 1 set	1	1	0	0	1	0	0	0	INC	WLS	KT	SHL	(BE)	PE	DTY1	DTY0	Sets the address increment X or Y direction (INC), display data word length (WLS), key scan time (KT), common driver shift direction (SHL), voltage doubler control (BE) (only applies to ML9092-02), port control (PE), and display duty (DTY0, DTY1).
9	Control register 2 set	1	1	0	0	1	0	0	1	0	0	0	0	0	0	(STB)	DISP	Sets or releases standby mode (only applies to ML9092-03) and also sets display ON/OFF (DISP).
A	Rotary encoder read	1	1	1	0	1	0	1	0	Q4	Q4	Q4	Q4	Q4	Q3	Q2	Q1	Reads the counter bits (Q1 to Q4) of the rotary encoder.
B	Contrast ADJ set	1	1	0	0	1	0	1	1	–	–	–	–	CT3	CT2	CT1	CT0	Sets contrast adjustment values with the contrast adjustment bits (CT0 to CT3).
F	Test register set	1	1	0	0	1	1	1	1	–	–	–	T5	T4	T3	T2	T1	Test instruction exclusively used by manufacturer (T1 to T5). Customers should not use this instruction.

Notes:

R/W : Read/write select bit 1:Read, 0: Write
ST0 to ST2 : Key scan read count display bits
S0 to S3 : Key scan data
D0 to D7 : Write or read data of the display data RAM
X0 to X3 : X addresses of the display data RAM
Y0 to Y3 : Y addresses of the display data RAM
PTA0 : Port A data
INC : Display data RAM address increment. 1: X direction, 0: Y direction
WLS : Word length select bit 1: 6 bits, 0: 8 bits
KT : Key scan period select bit 1: 10 ms, 0: 0.5 ms
SHL : Common driver shift direction select bit
1: COM10→COM1, 0: COM1→COM10
BE (only applies to ML9092-02)
: Voltage doubler control bit 1: Voltage doubler enable
0: Voltage doubler disable

PE : Port enable/disable select bit 1: All ports enable
0: All ports go into high impedance for output
DTY0, DTY1 : Display duty select bits (1/8, 1/9, 1/10)
STB (only applies to ML9092-03) : Standby mode/normal mode select bit
1: Standby mode, 0: Normal mode
DISP : Display ON/OFF select bit 1: Display ON, 0: Display OFF
Q1 to Q4 : Rotary encoder switch count bits (2's complement)
CT0 to CT3 : Contrast adjustment bit
T1 to T5 : Bits for test instruction. Customers should not access these bits.
– : Don't Care

Instruction Code List (ML9092-04)

No.	Instruction	Instruction Code								Data								Description
		Fixed bit		R/W	Register No.													
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
0	Key scan register read	1	1	1	0	0	0	0	0	ST2	ST1	ST0	S4	S3	S2	S1	S0	Reads scan read timing bits (ST0 to ST2) and key scan data (S0 to S4) of the key scan register.
1	Display data RAM write	1	1	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Writes display data (D0 to D7) in the display data RAM after setting the X address of Y address.
1	Display data RAM read	1	1	1	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Reads display data (D0 to D7) from the display data RAM after setting the X address of Y address.
2	X address register set	1	1	0	0	0	0	1	0	–	–	–	–	X3	X2	X1	X0	Sets the X address (X0 to X3) of the display data RAM.
3	Y address register set	1	1	0	0	0	0	1	1	–	–	–	–	Y3	Y2	Y1	Y0	Sets the Y address (Y0 to Y3) of the display data RAM.
4	Port register A set	1	1	0	0	0	1	0	0	–	–	–	–	–	–	–	PTA0	Controls the output of the general-purpose port A (PTA0).
5	Port register B set	1	1	0	0	0	1	0	1	–	–	–	–	–	PTB2	PTB1	PTB0	Controls the output of the general-purpose port B (PTB0 to PTB2).
8	Control register 1 set	1	1	0	0	1	0	0	0	INC	WLS	KT	SHL	–	PE	DTY1	DTY0	Sets the address increment X or Y direction (INC), display data word length (WLS), key scan time (KT), common driver shift direction (SHL), port control (PE), and display duty (DTY0, DTY1).
9	Control register 2 set	1	1	0	0	1	0	0	1	0	0	0	0	0	0	STB	DISP	Sets or releases standby mode and also sets display ON/OFF (DISP).
A	Rotary encoder read	1	1	1	0	1	0	1	0	Q4	Q4	Q4	Q4	Q4	Q3	Q2	Q1	Reads the counter bits (Q1 to Q4) of the rotary encoder.
B	Contrast ADJ set	1	1	0	0	1	0	1	1	–	–	–	–	CT3	CT2	CT1	CT0	Sets contrast adjustment values with the contrast adjustment bits (CT0 to CT3).
C	PWM0 register set	1	1	0	0	1	1	0	0	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	Sets the pulse width to be output from general-purpose port B (PTB0) with the bits (PW00 to PW07) of PWM0.
D	PWM1 register set	1	1	0	0	1	1	0	1	PW17	PW16	PW15	PW14	PW13	PW12	PW11	PW10	Sets the pulse width to be output from general-purpose port B (PTB1) with the bits (PW10 to PW17) of PWM1.
E	PWM2 register set	1	1	0	0	1	1	1	0	PW27	PW26	PW25	PW24	PW23	PW22	PW21	PW20	Sets the pulse width to be output from general-purpose port B (PTB2) with the bits (PW20 to PW27) of PWM2.
F	Test register set	1	1	0	0	1	1	1	1	–	–	–	T5	T4	T3	T2	T1	Test instruction exclusively used by manufacturer (T1 to T5). Customers must not use this instruction.

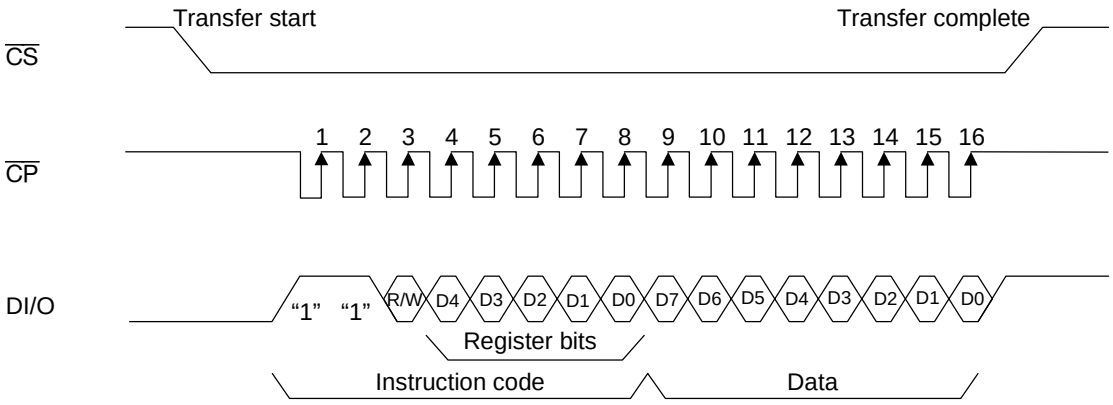
Notes:

R/W : Read/write select bit 1:Read, 0: Write
ST0 to ST2 : Key scan read count display bits
S0 to S4 : Key scan data
D0 to D7 : Write or read data of the display data RAM
X0 to X3 : X addresses of the display data RAM
Y0 to Y3 : Y addresses of the display data RAM
PTA0 : Port A data
PTB0 to PTB2 : Port B output control 1: Output enable, 0: Fixed at "L"
INC : Display data RAM address increment. 1: X direction, 0: Y direction
WLS : Word length select bit 1: 6 bits, 0: 8 bits
KT : Key scan period select bit 1: 10 ms, 0: 0.5 ms
SHL : Common driver shift direction select bit
1: COM10→COM1, 0: COM1→COM10

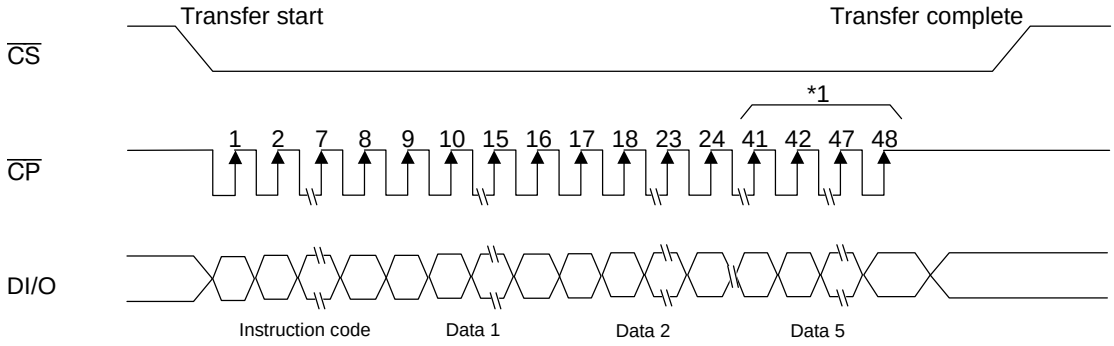
PE : Port enable/disable select bit 1: All ports enable
0: All ports go into high impedance for output
DTY0, DTY1 : Display duty select bits (1/8, 1/9, 1/10)
STB : Standby mode/normal mode select bit
1: Standby mode, 0: Normal mode
DISP : Display ON/OFF select bit 1: Display ON, 0: Display OFF
Q1 to Q4 : Rotary encoder switch count bits (2's complement)
CT0 to CT3 : Contrast adjustment bit
PW00 to PW07 : PWM0 setting bits
PW10 to PW17 : PWM1 setting bits
PW20 to PW2 : PWM2 setting bits
T1 to T5 : Bits for test instruction. Customers should not access these bits.

– : Don't Care

Clock Synchronous Serial Transfer Example (WRITE)

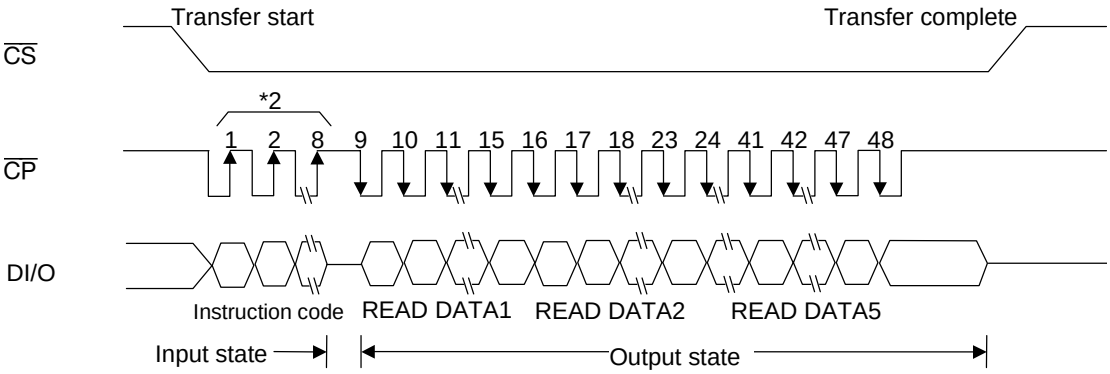


Clock Synchronous Serial Continuous Data Transfer Example (WRITE: Example of display data RAM write)



*1: Be sure to write data in 8 bits. If the $\overline{CS}$ signal falls when data input operation in 8 bits is not complete, the last 8-bit data write is invalid. (The previously written data is valid.)

Clock Synchronous Serial Continuous Data Transfer Example (READ)



*2: A reading state appears only when the R/W bit is “1”. The read data is valid only when the register is set to key scan read mode, rotary encoder read mode or display data read mode. Otherwise, the read data is invalid (undefined data will be read out).

Output Pin, I/O Pin and Register States When Reset Is Input

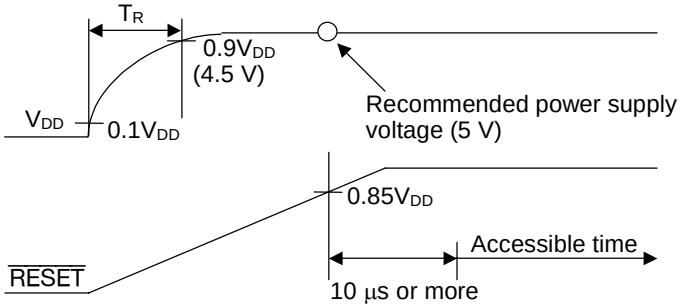
Pin and register states while the $\overline{\text{RESET}}$ input is pulled to a "L" level are listed below.

Output pin, I/O pin	State
DI/O	Input state
KREQ	"L" (V_{SS})
OSC2	Oscillating state
R0/C0 to R4/C4 (when these pins are used for key scanning in ML9092-01); R0 to R5 (ML9092-02/03); R0 toR4 (ML9092-04)	"L" (V_{SS})
R0/C0 to R4/C4 (when these pins are used as port C outputs in ML9092-01)	High impedance
C0/D0 to C4/D4 (when these pins are used as port D outputs in ML9092-01)	High impedance (any pull-up resistors are turned off)
PA0	High impedance
PB0 to PB2 (ML9092-01/04)	High impedance
SEG1 to SEG56 (ML9092-01); SEG1 to SEG60 (ML9092-02/03/04)	V_{SS}
COM1 to COM10	V_{SS}

Register	State
Key scan register	Reset to "0"
Display data register	Display data is retained
X address register	Reset to "0"
Y address register	Reset to "0"
Port A register	Reset to "0"
Port B register (ML9092-01/04)	Reset to "0"
Port C register (When KPS = "0" in ML9092-01)	Reset to "0"
Port D register (When KPS = "0" in ML9092-01)	Reset to "0"
Control register 1	Bits INC and KT are set to "1". Bits WLS, SHL, PE, DTY1 and DTY0 are reset to "0".
Control register 2	Display OFF, normal mode (Standby mode is released)
Rotary encoder read register	Reset to "0"
Contrast ADJ register	Set to "F"
PWM0 register (for ML9092-01/04)	Reset to "0"
PWM1 register (for ML9092-01/04)	Reset to "0"
PWM2 register (for ML9092-01/04)	Reset to "0"

Power-On Reset

The capacitance of an external capacitor that is connected to the $\overline{\text{RESET}}$ pin must be C_{RST} [μF] ≥ 12.5 × T_R [s], where T_R is the rise time taken until the power supply voltage to be supplied to the ML9092-01/02/03/04 reaches $0.9V_{DD}$ (4.5 V) from $0.1V_{DD}$, and C_{RST} is the capacitance of an external capacitor connected to the $\overline{\text{RESET}}$ pin.
(For example, if T_R = 10 [ms], then C_{RST} ≥ 0.125 [μF])
The pulse width when an external reset signal is input should be T_R or more.
Set an instruction at least 10 μs after the reset signal reaches $0.85V_{DD}$ or more.
Thereafter, this IC is accessible.



Serial Interface Operation

- Instruction code

A register that transfers display data, key scan data, etc. according to the content of the instruction code is selected (see below).

D7	D6	D5	D4	D3	D2	D1	D0
"1"	"1"	R/W	Register number				

(1) D7, D6 (fixed at "1")
When selecting the start byte register, always write a "1" to bits D7 and D6.

(2) D5 (R/W) (Read mode/write mode select bit)
1: Read mode is selected
0: Write mode is selected

(3) D4 to D0 (Register number)

The correspondence between the start byte contents and the registers and display data RAM is shown in the table below.

D7	D6	D5	D4	D3	D2	D1	D0	Register name
1	1	0	1	0	0	0	0	Key scan register
1	1	1	1/0	0	0	0	1	Display data RAM
1	1	0	0	0	0	1	0	X address register
1	1	0	0	0	0	1	1	Y address register
1	1	0	0	0	1	0	0	Port A register
1	1	0	0	0	1	0	1	Port B register
1	1	0	0	0	1	1	0	Port C register
1	1	0	0	0	1	1	1	Port D register
1	1	0	0	1	0	0	0	Control register1
1	1	0	0	1	0	0	1	Control register 2
1	1	1	0	1	0	1	0	Rotary encoder register
1	1	0	0	1	0	1	1	Contrast ADJ register
1	1	0	0	1	1	0	0	PWM0 register
1	1	0	0	1	1	0	1	PWM1 register
1	1	0	0	1	1	1	0	PWM2 register

Description of the Data Section in Instructions

- Key scan register (KR)—Read (for ML9092-01/04)

D7	D6	D5	D4	D3	D2	D1	D0
ST2	ST1	ST0	S4	S3	S2	S1	S0

(1) D7 to D5 (ST2 to ST0) (Key scan read count display bits)
25-bit key scan data is divided into 5 groups and read. The read count is indicated by bits ST2 to ST0.
Every time key scan data is read, these bits are automatically incremented over the range of "000" to "100". After counting to "100", this counter is reset to "000" and then again incremented from "000", thereafter repeating this cycle. If the $\overline{CS}$ signal is risen up during the cycle of counting, the scan read counter bits are returned to "000".
If the $\overline{RESET}$ pin is pulled to a "L" level, these bits are reset to "0".

(2) D4 to D0 (S4 to S0) (Key scan read data bits)
These bits are read as 25-bit serial data that expresses the key switch status (1 = ON, 0 = OFF). Data is divided into 5 groups and read. (For the read order, refer to the description below.) The read count is indicated by bits ST2 to ST0.
The correspondence between the scan read count data, key scan data and key matrix switches is shown below.
If the $\overline{RESET}$ pin is pulled to a "L" level, these bits are reset to "0".

ST2	ST1	ST0	S4	S3	S2	S1	S0	
0	0	0	SW04	SW03	SW02	SW01	SW00	R0
0	0	1	SW14	SW13	SW12	SW11	SW10	R1
0	1	0	SW24	SW23	SW22	SW21	SW20	R2
0	1	1	SW34	SW33	SW32	SW31	SW30	R3
1	0	0	SW44	SW43	SW42	SW41	SW40	R4

Note: SW00 to SW44 indicate the corresponding switches in Figure 1.

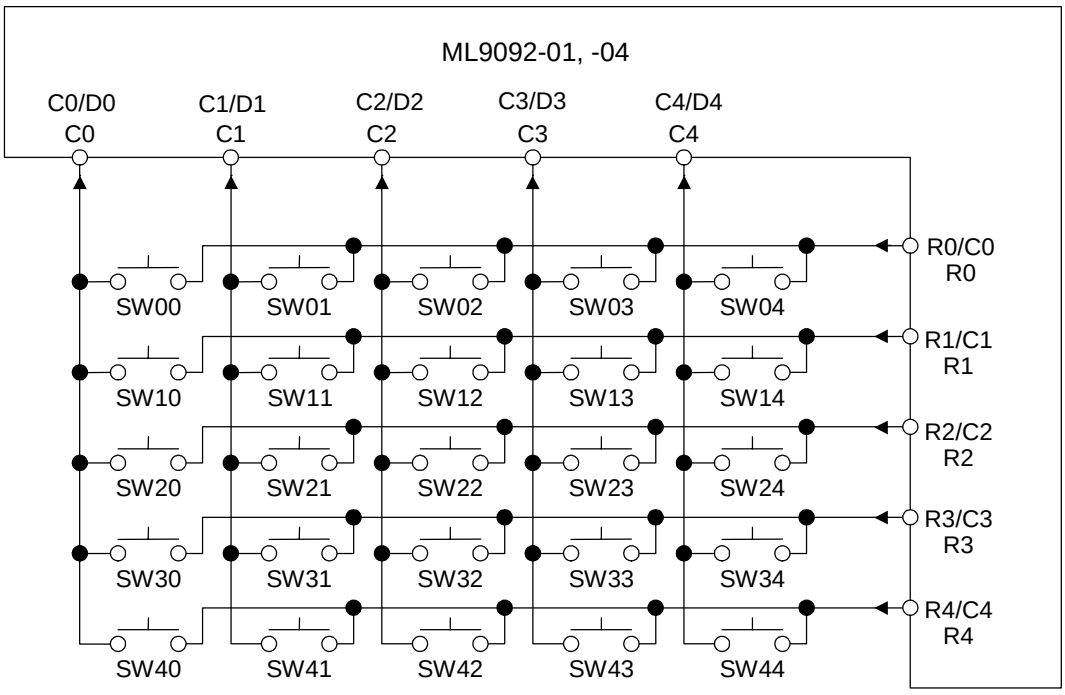
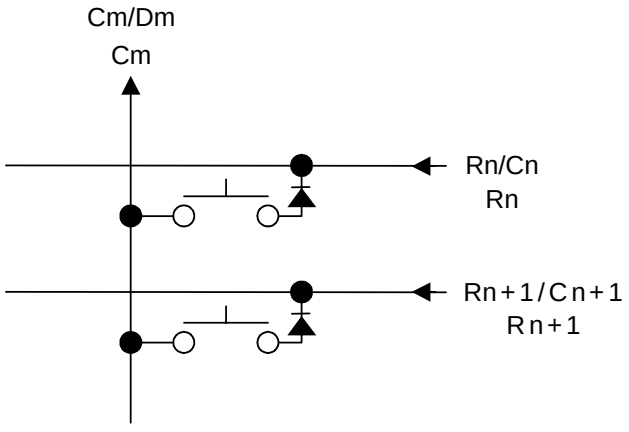


Figure 1

(Note) To recognize simultaneous depression of three or more key switches, add a diode in series to each key.



Connection with diodes

- Key scan register (KR)—Read (for ML9092-02/03)

D7	D6	D5	D4	D3	D2	D1	D0
ST2	ST1	ST0	0	S3	S2	S1	S0

(1) D7 to D5 (ST2 to ST0) (Key scan read count display bits)
24-bit key scan data is divided into 6 groups and read. The read count is indicated by bits ST2 to ST0.
Every time key scan data is read, these bits are automatically incremented over the range of "000" to "101". After counting to "101", this counter is reset to "000" and then again incremented from "000", thereafter repeating this cycle. If the $\overline{CS}$ signal is risen up during the cycle of counting, the scan read counter bits are returned to "000".
If the $\overline{RESET}$ pin is pulled to a "L" level, these bits are reset to "0".

(2) D3 to D0 (S3 to S0) (Key scan read data bits)
These bits are read as 24-bit serial data that expresses the key switch status (1 = ON, 0 = OFF). Data is divided into 6 groups and read. (For the read order, refer to the description below.) The read count is indicated by bits ST2 to ST0.
The correspondence between the scan read count data, key scan data and key matrix switches is shown below.
If the $\overline{RESET}$ pin is pulled to a "L" level, these bits are reset to "0".

ST2	ST1	ST0	S4	S3	S2	S1	S0	
0	0	0	0	SW03	SW02	SW01	SW00	R0
0	0	1	0	SW13	SW12	SW11	SW10	R1
0	1	0	0	SW23	SW22	SW21	SW20	R2
0	1	1	0	SW33	SW32	SW31	SW30	R3
1	0	0	0	SW43	SW42	SW41	SW40	R4
1	0	1	0	SW53	SW52	SW51	SW50	R5

Note: SW00 to SW53 indicate the corresponding switches in Figure 2.

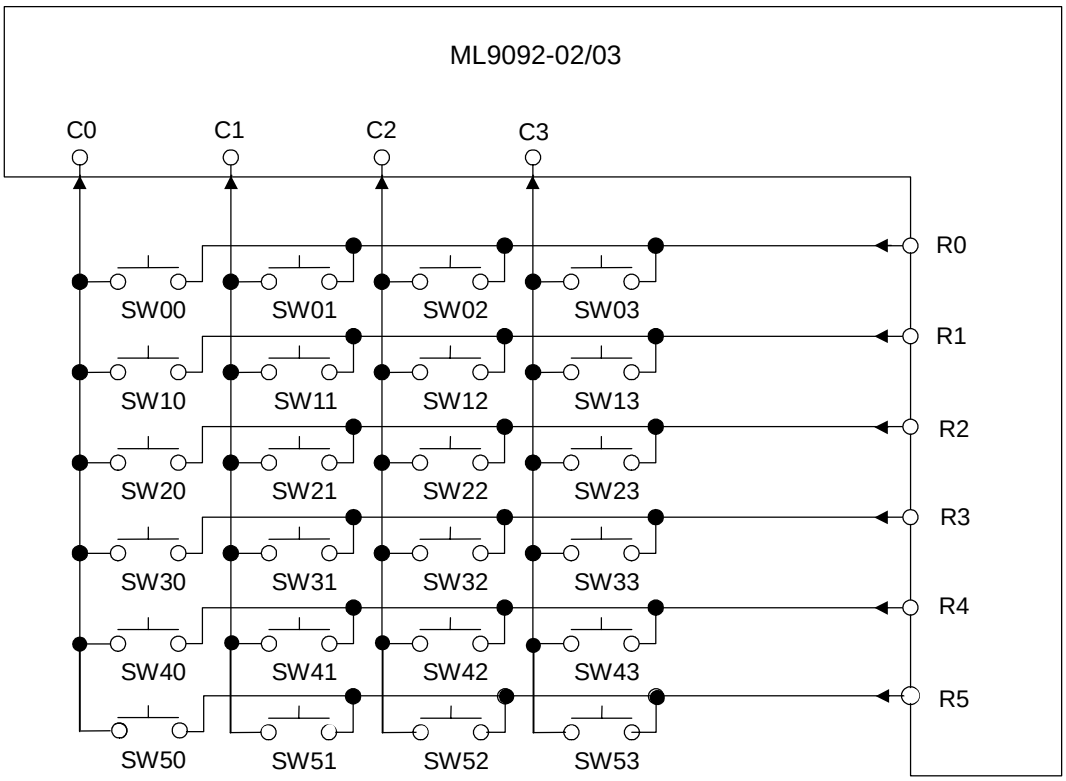
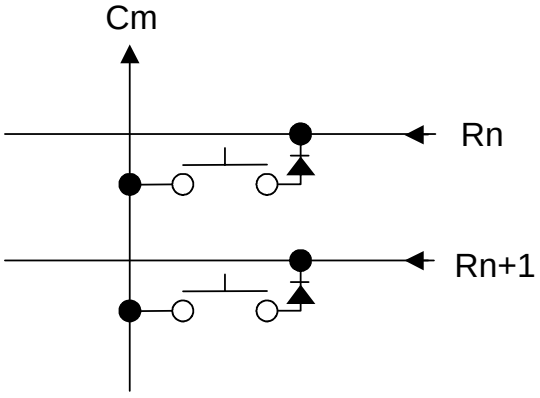


Figure 2

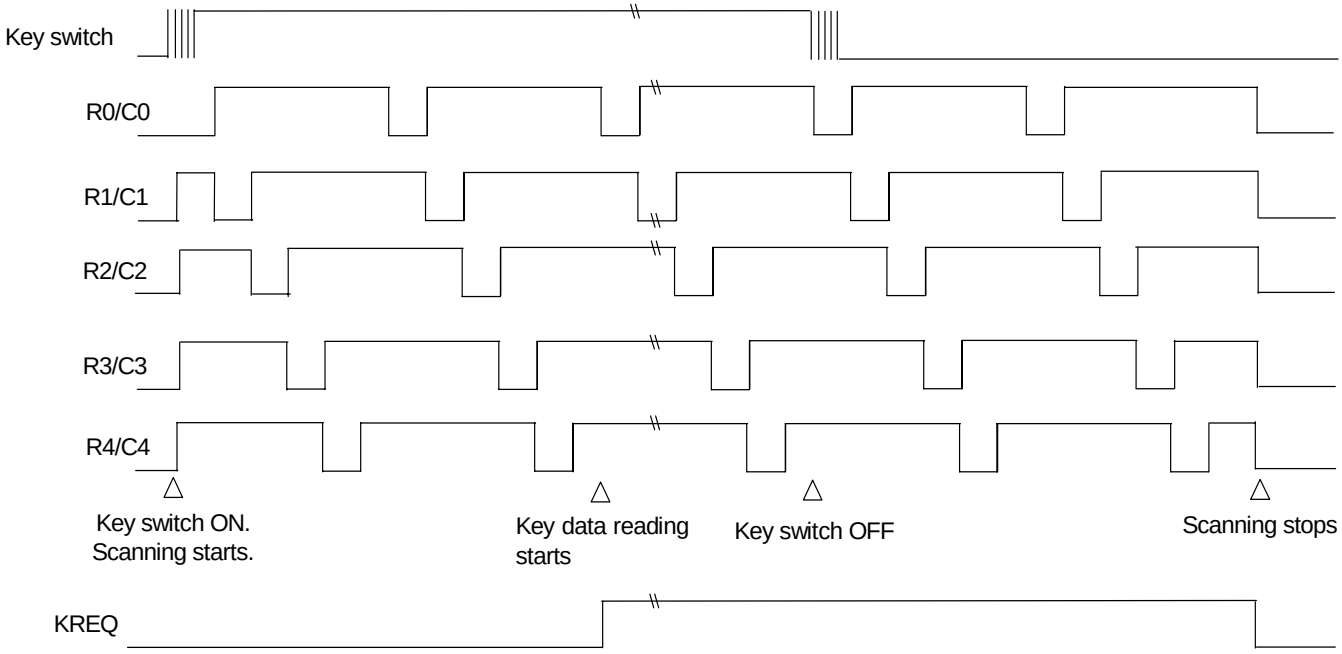
(Note) To recognize simultaneous depression of three or more key switches, add a diode in series to each key.



Connection with diodes

Key Scan

The key scanning starts when a key switch is pressed on and ends after all key switches are detected to be off. After the key switch is turned on, when the same key is pressed for two cycles or more, the level of the KREQ signal changes from a "L" to "H" level. In the same manner, the level of the KREQ signal changes from "H" to "L" two cycles after all key switches are turned off.
This signal can be used as a flag. To use it as a flag, start key-scan reading when the KREQ signal has changed from "L" to "H."
While the KREQ signal is at a "H" level, carry out key-scan reading periodically. Carry out key scan reading also when the KREQ signal has changed from "H" to "L".
The KREQ signal (the KREQ signal that is sent when the key switch is turned on) is reset when all key switches are detected to be off or when a "L" level is applied to the $\overline{\text{RESET}}$ pin.



Notes:
1. Even when the KREQ signal changes from "L" to "H", chattering for more than one key scan cycle is not absorbed. This should be handled by multiple data reads by software.
2. How simultaneous depression of two keys is processed should be handled by software.
3. When three or more key switches are pressed at the same time, the device may recognize that key(s) that has not been actually pressed has been pressed. Therefore, to recognize simultaneous depression of three or more key switches, add a diode in series to each key (see Figures 1 and 2). To ignore simultaneous depression of three or more key switches, a program may be required to ignore all key data which contains three or more consecutive "1" values.

- Display data RAM (DRAM) read/write

D7	D6	D5	D4	D3	D2	D1	D0
8-bit DATA							
0	0	6-bit DATA					

The display data RAM read/write instruction writes and reads display data to and from the liquid crystal display RAM. Data that is input to the address set by the X and Y address registers is written to or read from this register. The bit length of display data can be selected by the WLS bit of control register 1. If 6-bit data has been selected, writing to D7 and D6 is invalid, and if read, their values will always be "0". D7 is the MSB (D5 in the case of 6-bit data) and D0 is the LSB.
The X address and Y address should be set immediately before writing or reading display data (either X address or Y address may be set first). However, in the case of successive writings or readings, only one-time settings of X address and Y address are required immediately before the writing or reading, in which case X address and Y address are automatically incremented every time data is written or read (see the description under the heading "X•Y address Counter Auto Increment."
The contents of this register will not change even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

- X address register (XAD) set

D7	D6	D5	D4	D3	D2	D1	D0
—				XAD			

—: don't care

The X address register set instructions sets the X address for the liquid crystal display RAM.
The address setting range is 0 to 7 (00H to 07H) when 8-bit data is selected with the WLS bit (bit D6) of the control register 1 (WLS = "0"). In this case, this register starts incrementing the X address from the set value each time RAM is read or written. When the count value of this register returns to 0 from the maximum value 7, the Y address is automatically incremented as well. Thereafter, the Y address is counted in a loop fashion from 0 to 7.
The address setting range is 0 to 9 (00H to 09H) when 6-bit data is selected (WLS = "1"). In this case this register starts incrementing the X address from the set value. When the count value of this register returns to 0 from the maximum value 9, the Y address is automatically incremented as well. Thereafter, the Y address loops from 0 to 9. Proper operation is not guaranteed if values outside this range are set.
Writing to bits D7 through D4 is invalid. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

- Y address register (YAD) set

D7	D6	D5	D4	D3	D2	D1	D0
—				YAD			

—: don't care

The Y address register set instruction sets a Y address of RAM for the liquid crystal display.
The Y address setting range varies according to the setting of the DTY bits (bits D1 and D0) of the control register 1 (described later).
The relation between the internal RAM areas and the display RAM areas is shown in the Table below. RAM areas that are not displayed can be used as data RAM areas.
This register starts incrementing the Y address from the set value each time RAM is read or written. When the register count returns to 0 from the maximum value (09H), the X address is also incremented automatically.
Thereafter, the Y address is counted in a loop fashion as shown in the Table below. However, if RAM areas that are not displayed are used, the X address is not incremented automatically.

Duty	Y register setting range and loop range	Invalid address setting range
1/8	0 to 7 (00H to 07H)	0 to 7 (00H to 07H)
1/9	0 to 8 (00H to 08H)	0 to 8 (00H to 08H)
1/10	0 to 9 (00H to 09H)	0 to 9 (00H to 09H)

This register is reset to "0" when the $\overline{\text{RESET}}$ pin is made low.

- Port register A (PTA) set

D7	D6	D5	D4	D3	D2	D1	D0
—							PTA

—: don't care

The port register A set instruction sets the output of port A.
When the PTA bit is set to "1", a "H" level is output from the PA0 pin of general purpose port A. In the same way, when the PTA bit is set to "0", a "L" level is output from the PA0 pin. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the PE bit (bit D2) of the control register is reset to "0", this register is reset to "0", and the PA0 pin goes to high impedance.
After the reset state is released, if the PTA bit of this register is set to "1" or "0" and then the PE bit is set to "1", the PA0 pin is released from its high impedance state and a "H" or "L" level that corresponds to the set status of the PTA bit, is output from the PA0 pin.

- Port register B (PTB) set

D7	D6	D5	D4	D3	D2	D1	D0
—					PTB2	PTB1	PTB0

—: don't care

The port register B set instruction sets the output of port B. (Applies to the ML9092-01/04.)
When each bit of PTB0 to PTB2 is set to "1", the PWM signal set in the PWM0 to PWM2 registers is output from each of the PB0 to PB2 pins of the general purpose port B. In the same way, when each bit of PTB0 to PTB2 is set to "0", each of the PB0 to PB2 pins are pulled to a "L" level. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the PE bit (bit D2) of the control register is reset to "0", this register is reset to "0", and the PB0 to PB2 pins go to high impedance.
After the reset state is released, if the a PWM value is set in the PWM0 to PWM2 registers and then the PE bit is set to "1", the PB0 to PB2 registers are released from their high impedance state and a PWM waveform is output.

- Port register C (PTC) set

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	PTC4	PTC3	PTC2	PTC1	PTC0

—: don't care

The port register C set instruction sets the output of port C. (Applies to the ML9092-01 only.)
This register is enabled when a "L" level is applied to the KPS pin of ML9092-01 and the R0/C0 to R4/C4 pins are set as port C.
When each bit of PTC4 to PTC0 is set to "1", a "H" level is output from each of the R4/C4 to R0/C0 pins of the general purpose port C. In the same way, when each bit of PTC4 to PTC0 is set to "0", a "H" level is output from each of the R4/C4 to R0/C0 pins. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the PE bit (bit D2) of the control register is reset to "0", this register is reset to "0", and the R4/C4 to R0/C0 pins go to high impedance.
After the reset state is released, if the PTC4 to PTC0 bits of this register are set to "1" or "0" and then the PE bit is set to "1", the R4/C4 to R0/C0 pins are released from its high impedance state and a "H" or "L" level that corresponds to the set status of each bit of PTC4 to PTC0, is output from the R4/C4 to R0/C0 pins.

- Port register D (PTD) set

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	PTD4	PTD3	PTD2	PTD1	PTD0

—: don't care

The port register D set instruction sets the output of port D. (Applies to the ML9092-01 only.)
This register is enabled when a "L" level is applied to the KPS pin of ML9092-01 and the C0/D0 to C4/D4 pins are set as port C.
When each bit of PTD4 to PTD0 is set to "1", a "H" level is output from each of the C4/D4 to C0/D0 pins of the general purpose port D. In the same way, when each bit of PTD4 to PTD0 is set to "0", a "H" level is output from each of the C4/D4 to C0/D0 pins. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the PE bit (bit D2) of the control register is reset to "0", this register is reset to "0", and the C4/D4 to C0/D0 pins go to high impedance.
After the reset state is released, if the PTD4 to PTD0 bits of this register are set to "1" or "0" and then the PE bit is set to "1", the C4/D4 to C0/D0 pins are released from its high impedance state and a "H" or "L" level that corresponds to the set status of each bit of PTD4 to PTD0, is output from the C4/D4 to C0/D0 pins.

- Control register 1 (FCR1)

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	KT	SHL	BE	PE	DTY1	DTY0

(1) D7 (INC) Address increment direction
1: X direction address increment
0: Y direction address increment
This bit sets the address increment direction of the display RAM. The display RAM address is automatically incremented by 1 every time data is written to the display data register. Writing a "1" to this bit sets "X address increment," and writing a "0" sets "Y address increment." For further details regarding address incrementing, refer to the page entitled "X, Y Address Counter Auto Increment." This bit is set to "1" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

(2) D6 (WLS) (Word Length Select)

1: 6-bit word length select

0: 8-bit word length select

This bit selects the word length of data to be written to and read from the display RAM. If "1" is written to this bit, data will be read from and written to the display RAM in 6-bit units. If "0" is written to this bit, data will be read from and written to the display RAM in 8-bit units. This bit is reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

(3) D5 (KT) (Key scan time) Key scan time select bit

1: 10 ms

0: 5 ms

This bit selects the key scan cycle time. In the case of a 306 kHz oscillating frequency, writing a "1" to this bit sets the key scan cycle time at 10 ms (1/3072 divided frequency of the oscillating frequency), writing a "0" sets the key scan cycle time at 5 ms (1/1536 divided frequency of the oscillating frequency). This bit is set to "1" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

(4) D4 (SHL) (Common driver shift direction select bit)

This bit selects the shift direction of common drivers.

The relationship between this bit and shift directions are shown below.

This bit is reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

SHL	Duty	Shift direction
1	1/8	COM8 → COM1
	1/9	COM9 → COM1
	1/10	COM10 → COM1
0	1/8	COM1 → COM8
	1/9	COM1 → COM9
	1/10	COM1 → COM10

(5) D3 (BE) (Voltage doubler operation control bit)

This bit controls the operation of the voltage doubler. (Applies to ML9092-01/02.)

1: Voltage doubler enable

0: Voltage doubler disable

This bit is reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

(6) D2 (PE) (General-purpose port output enable/disable select bit)

This bit selects high impedance output or output enable for the general-purpose port outputs A, B, C and D (C and D apply to ML9092-01 only; B applies to ML9092-01/04).

1: Output enable

0: High-impedance output (output disable)

This bit is reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

(7) D1, D0 (DTY1, DTY0) (Display duty select bits)

These bits select the display duty. The correspondence between each bit and display duty is shown in the chart below. These bits are reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

DTY1	DTY0	Display duty
0	0	1/8
0	1	1/9
1	0	1/10
1	1	1/10

- Control register 2 (FCR2)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	STB	DISP

(1) D1 (STB) (Standby mode select bit)
This bit is used to control the standby and normal modes. (Applies to ML9092-03/04.)
1: Standby mode
0: Normal mode

This bit is reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.
The LSI internal status and pin status during standby mode are as follows:
- RAM data is retained.
- Common output and segment output are V_{SS} level.
- Electronic volume values are retained.
- Port output A is at a "L" level (applies to ML9092-03/04). The status before standby is maintained for port output B (applies to ML9092-04).
- RC oscillation is stopped. (Oscillation is started with key input, maintained while the KREQ output is at a "H" level, and stopped when all key switches are turned off and the KREQ output is at a "L" level.)
- Rotary encoder input signals (A and B) are ignored.
- Key input allowed.
- The microcontroller interface (CS, CP, DI/O, KREQ) is operable. (However, only with a KREQ signal from the key scan, will the KREQ pin output a "H" level.)
- V_{HIN} and V_O should be set to V_{SS} or the floating status.

Note: When there is a key input in a standby state, this IC will start oscillating and KREQ output will go to a "H" level. Execute key scan reading periodically during this "H" level period. Also, execute key scan reading when the KREQ signal changes from a "H" to "L" level.

(2) D0 (DISP) (Display ON/OFF mode bit)
1: Display ON mode
0: Display OFF mode

This bit selects whether the display is ON or OFF. Writing a "1" to this bit selects the display ON mode. Writing a "0" to this bit selects the display OFF mode. At this time, the COM and SEG pins will be at the V_{SS} level. Even if this bit is set to "0", the display RAM contents will not change. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0".

- Rotary encoder (RE) read

D7	D6	D5	D4	D3	D2	D1	D0
Q4	Q4	Q4	Q4	Q4	Q3	Q2	Q1

The rotary encoder read instruction is used to read the count value from the rotary encoder switch input signal. (Count values are in the 2's complement format.)

(1) D7 to D0 (Q4 to Q1) (Count value bit)
The phase difference between the A signal and the B signal is recognized, and the value that is counted by the edge of the signal with the slower phase is set. Count values range from negative 1000 (Q4, Q3, Q2, Q1) to positive 0111. If the count is less than negative 1000 or more than positive 0111, then it is ignored.
These bits are all reset to "0" when this instruction is executed or when the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

If counterclockwise rotation is input after the count value is incremented by clockwise rotation, then count value will be decremented. If counterclockwise rotation is further input after the count value reaches 0000, then the count value will change to 1111 and the count value will be decremented. (The count value will remain 1000 even if counterclockwise rotation is further input after the count value reaches negative 1000.)
After this, if clockwise rotation is input, then the count value will be incremented. If the count value reaches 1111 and clockwise rotation is further input, then the count value will become 0000 and the count value will be incremented. (Even if clockwise rotation is further input after the count value reaches positive 0111, the count value will maintain 0111.)

Functional Description of the Rotary Encoder Switch

As shown in Figure 3, the rotary encoder switch circuit is made up of phase detection circuit, an interrupt generation circuit, an up/down counter and a parallel-in/serial-out register.

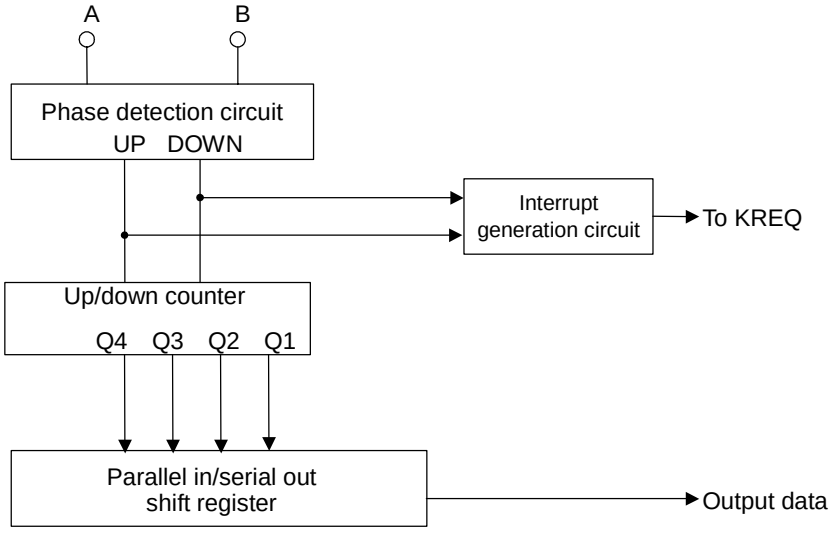


Figure 3 Rotary Encoder Switch Circuit

1) Phase Detection and Interrupt Generation Circuits

1-1) Clockwise Rotation

When the A and B signals are input as shown in Figure 4, the phase detection circuit outputs the UP signal after the chattering absorption period. At this time, the KREQ output goes to a high level, so that this signal can be used as the interrupt signal. The KREQ signal maintains a high level until the rotary encoder read instruction is executed.

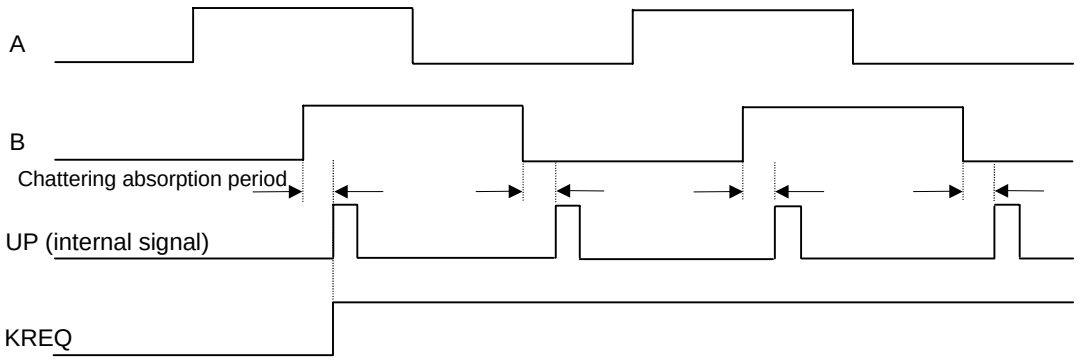


Figure 4 Input/Output Timing for Clockwise Rotation

1-2) Counterclockwise Rotation

When the A and B signals are input as shown in Figure 4, the phase detection circuit outputs the DOWN signal after the chattering absorption period. At this time, the KREQ output goes to a high level, so that this signal can be used as the interrupt signal. The KREQ signal maintains a high level until the rotary encoder read instruction is executed.

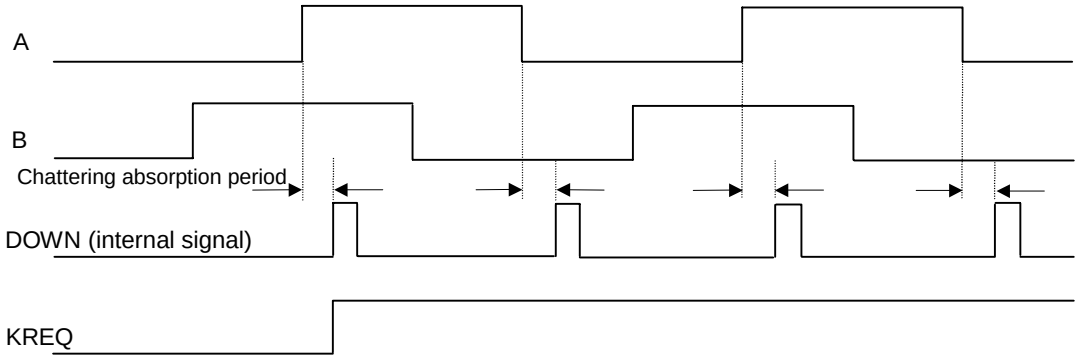


Figure 5 Input/Output Timing for Counterclockwise Rotation

2) UP/DOWN Counter

The UP/DOWN counter is incremented when an UP signal is input and decremented when a DOWN signal is input. However, if the counter reaches "0111" and an UP signal is input, the UP/DOWN counter will hold "0111". In the same manner, if the UP/DOWN counter is at "1000" and a DOWN signal is input, the UP/DOWN counter will hold "1000".

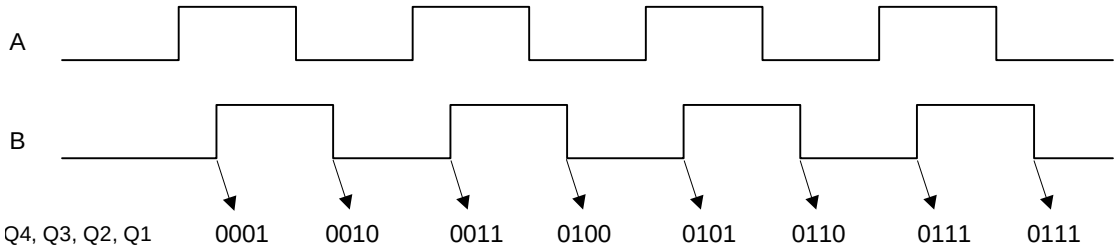


Figure 6 When the Up Counter Overflows

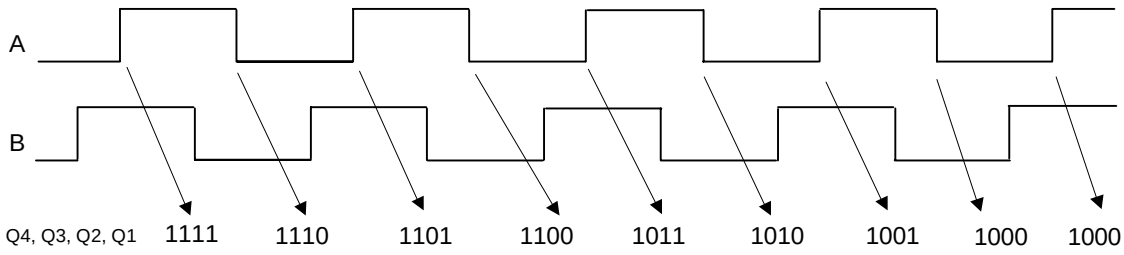


Figure 7 When the Down Counter Overflows

3) Parallel-in/Serial-out Shift Register

The KREQ signal goes to a low level when the rotary encoder read instruction is executed, when the UP/DOWN counter will be reset to "0".

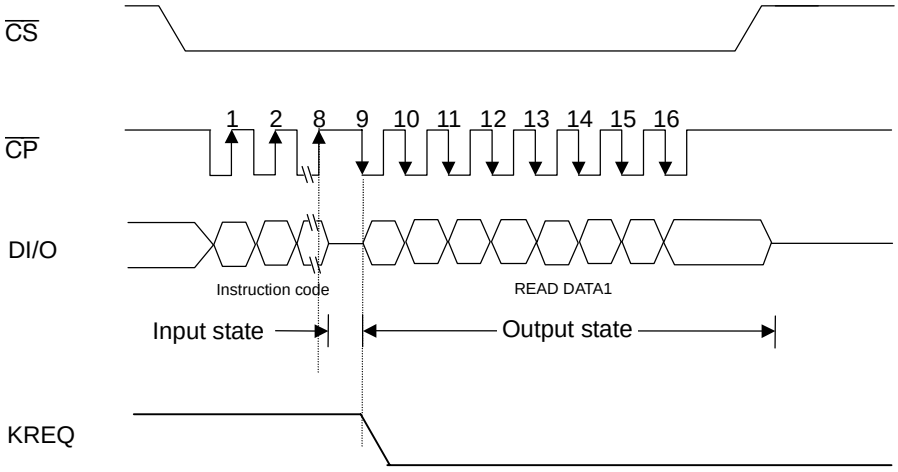
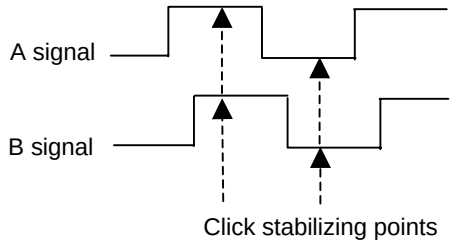


Figure 8 Operation of KREQ Output

Notes:

1. The KREQ signal is output by a logical OR of the KREQ signal generated by a key scan and the KREQ signal generated by the rotary encoder. The KREQ signal from the rotary encoder is reset by executing the rotary encoder read instruction; however, the KREQ signal generated by a key scan is not reset even if the key scan register read instruction is executed. Also, if the KREQ signal is generated by a key scan, it will not be reset even if the rotary encoder read instruction is executed. Although dependent on the components glued to this LSI, it is recommended that the rotary encoder read instruction and key scan register read instruction be executed as a set when the KREQ signal goes to a "H" level.
2. The maximum read cycle time for when the KREQ signal is at a "H" level is practically determined by the signal input from the rotary encoder and the 3-bit counter built into this LSI. Therefore, make the time taken before starting to execute the rotary encoder read instruction 12 ms or less.
3. Using a rotary encoder switch that has the click stabilizing points shown below is recommended.



Waveform of a Recommended Rotary Encoder Switch

- Contrast ADJ (CA) set

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	CT3	CT2	CT1	CT0

—: don't care

This instruction is for adjusting the liquid crystal display voltage.

(1) D3 to D0 (CT3 to CT0) (Contrast adjustment value setting bits)
When FH is written to these bits, the liquid crystal display voltage (voltage between the V_0 and V_{SS} pins) becomes a maximum.
When 0H is written, the liquid crystal display voltage becomes a minimum.
By setting the values from 0H to FH, the liquid crystal display voltage can be adjusted just like an electronic volume control.
These bits are all reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

V_0 Ouput Target Voltage for Contrast ADJ Setting Values

Contrast ADJ setting values				V_0 output target voltage	
CT3	CT2	CT1	CT0	ML9092-01/02	ML9092-03/04
1	1	1	1	$0.980V_{OUT}$	$0.980V_{HIN}$
1	1	1	0	$0.973V_{OUT}$	$0.973V_{HIN}$
1	1	0	1	$0.947V_{OUT}$	$0.947V_{HIN}$
1	1	0	0	$0.923V_{OUT}$	$0.923V_{HIN}$
1	0	1	1	$0.900V_{OUT}$	$0.900V_{HIN}$
1	0	1	0	$0.878V_{OUT}$	$0.878V_{HIN}$
1	0	0	1	$0.857V_{OUT}$	$0.857V_{HIN}$
1	0	0	0	$0.837V_{OUT}$	$0.837V_{HIN}$
0	1	1	1	$0.818V_{OUT}$	$0.818V_{HIN}$
0	1	1	0	$0.800V_{OUT}$	$0.800V_{HIN}$
0	1	0	1	$0.783V_{OUT}$	$0.783V_{HIN}$
0	1	0	0	$0.766V_{OUT}$	$0.766V_{HIN}$
0	0	1	1	$0.750V_{OUT}$	$0.750V_{HIN}$
0	0	1	0	$0.735V_{OUT}$	$0.735V_{HIN}$
0	0	0	1	$0.720V_{OUT}$	$0.720V_{HIN}$
0	0	0	0	$0.700V_{OUT}$	$0.700V_{HIN}$

• PWM0/1/2 register (PWMR) set

D7	D6	D5	D4	D3	D2	D1	D0
PWx7	PWx6	PWx5	PWx4	PWx3	PWx2	PWx1	PWx0

Note: "x" stands for 0 for PB0 (port B0), 1 for PB1 (port B1) and 2 for PB2 (port B2).

This instruction sets the pulse width of the PWM signal output from port B. (Applies to ML9092-01/04.)
PWx0 is LSB and PWx7 is MSB.
This instruction should be used with a PWM data write cycle of 5.0 ms or longer.
These bits are all reset to "0" if the $\overline{\text{RESET}}$ pin is pulled to a "L" level.

Note: When inputting multiple PWM data items, be sure to input them in succession (i.e., without intervals).

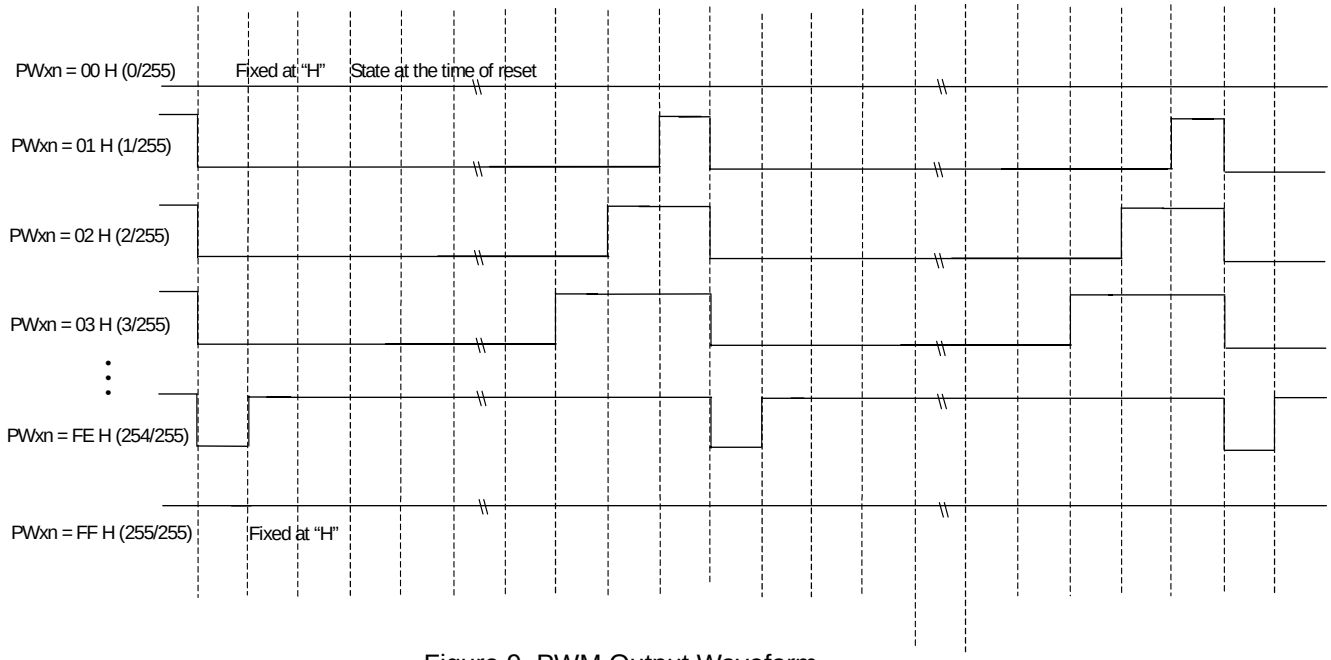


Figure 9 PWM Output Waveform

• Test register (TEST) set

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	T4	T3	T2	T1

—: don't care

This instruction is for testing by the manufacturer.
Customers should not use this register.

Display Screen and Memory Address Allocation

The ML9092-01/02/03/04 has an internal display data RAM (60 bits by 10 bits) of a bitmap type.
The allocation of memory addresses varies according to the selected word length (6 bits or 8 bits) as shown in Figure 10: 0 to 7 for selection of 8 bits per word or 0 to 9 for selection of 6 bits per word.
The X address 7 in the 6-bits/word mode has four display memory bits. The four bits (D7 to D4) starting from bit D7 of the display data register are written in memory and the other bits (D3 to D0) are ignored.

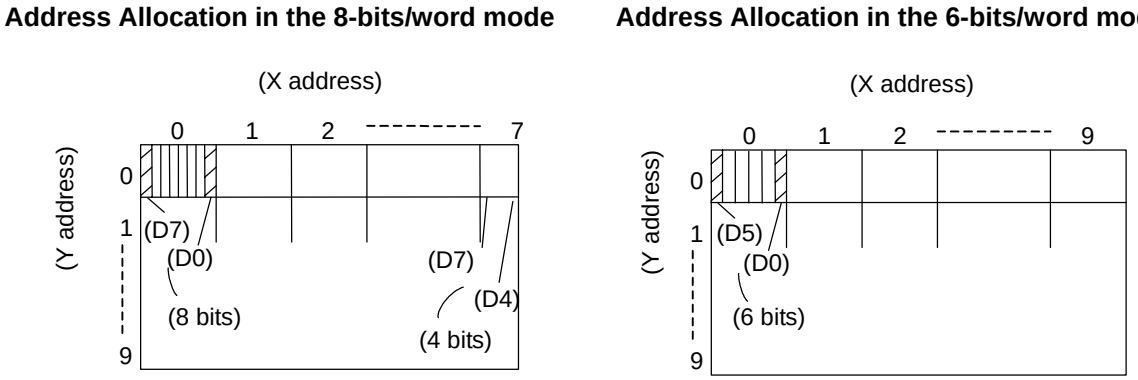


Figure 10 Display Memory Addresses

In the 8-bits/word mode, data to be displayed is written in display memory with the D7 data of the display data register at address (Xn, Yn) and the D0 data at address (Xn + 7, Yn). Similarly, In the 6-bits/word mode, data to be displayed is written in display memory with the D5 data of the display data register at address (Xn, Yn) and the D0 data at address (Xn + 5, Yn). See Figure 11.
Data "1" in display memory represents turning on the corresponding display segment and data "0" in display memory represents turning off the corresponding display segment.
Note: In the ML9092-01, the X address range in the 8-bits/mode will be 0 to 6

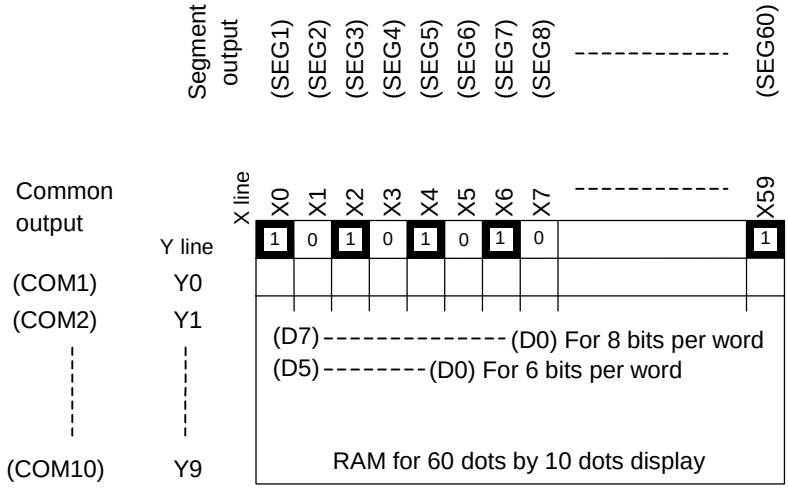


Figure 11 Display Screen Bit Allocation and Memory Addresses

X•Y address Counter Auto Increment

The liquid crystal display RAM has an X-address counter and a Y-address counter. Each address counter has an Auto Increment function.
When display data is read or written, this function increments either of these X- and Y-address counters (which is selected by the INC bit (D7 bit) of the control register 1).

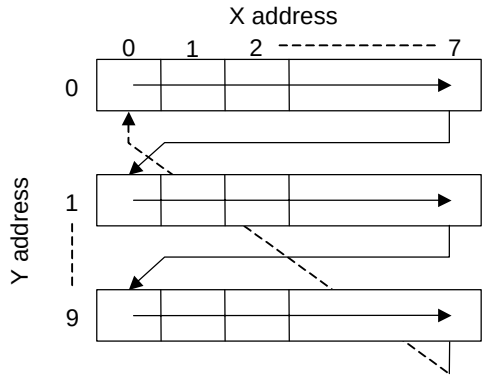
INC bit = "0" selects the Y-address counter.
INC bit = "1" selects the X-address counter.

The address counting cycle of the X address counter varies according to the selected word length (8 bits or 6 bits): X address range of 0 to 6 (ML9092-01) or 0 to7 (ML9092-02/03/04) in the 8-bits/word mode or X address range of 0 to 9 in the 6-bits/word mode.
When the X address count returns to 0 from a maximum value (6 (ML9092-01) or 7 (ML9092-02/03/04) in the 8-bits/word mode, or 9 in the 6-bits/word mode), the Y address is also incremented automatically.
The relationship between display duties and Y address count ranges is shown below.
When the Y-address counter returns to 0 from a maximum value, the X address is also incremented automatically.

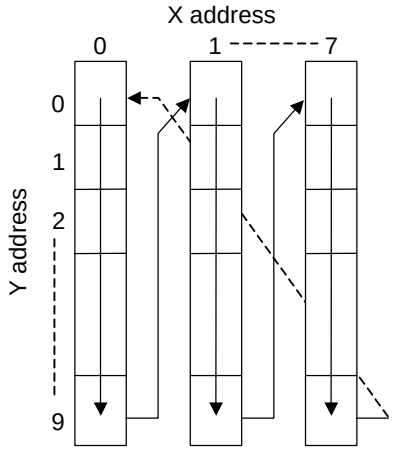
Model	Duty	Y-address count range (cycle)	Maximum Y address count
ML9092-01/02/03/04	1/8	0 to 7	7
	1/9	0 to 8	8
	1/10	0 to 9	9

Note: If an invalid address (outside the address count range) is given to the X- or Y- address counter, its counting will not be assured.

Example of incrementing the X-address
(8 bits per word and 1/10 duty)

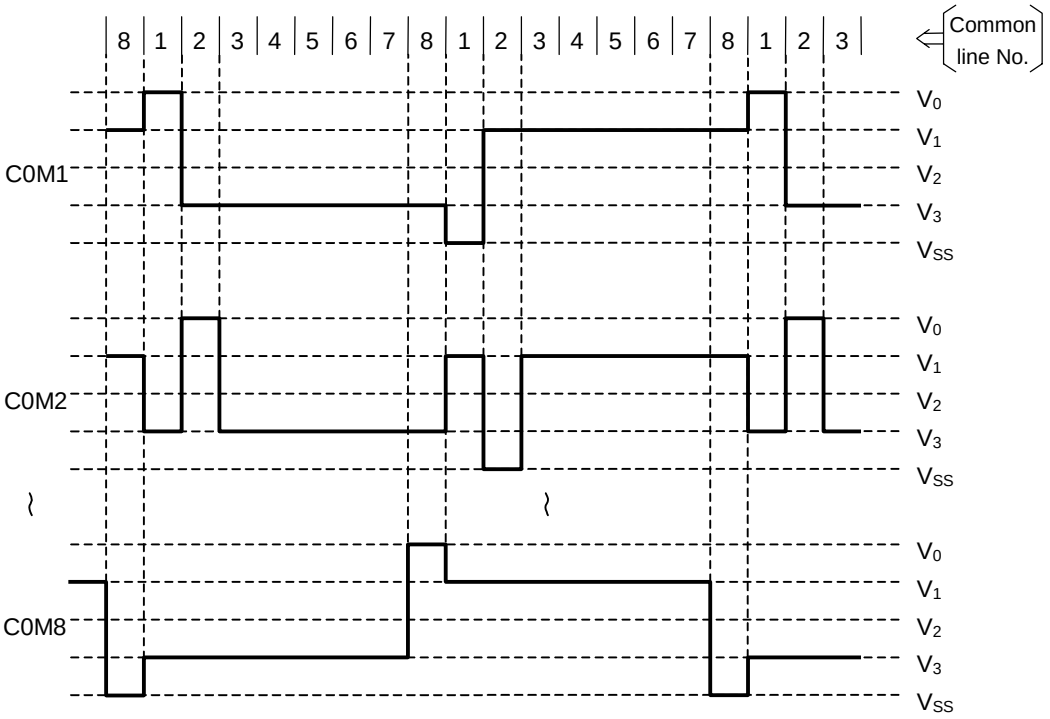


Example of incrementing the Y-address
(8 bits per word and 1/10 duty)

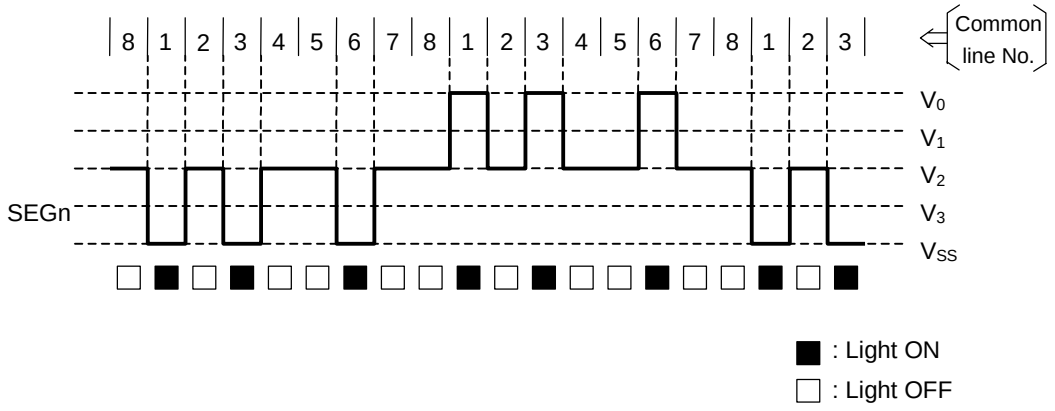


Liquid Crystal Driving Waveform Example (1)

1/8 duty (1/4 bias)

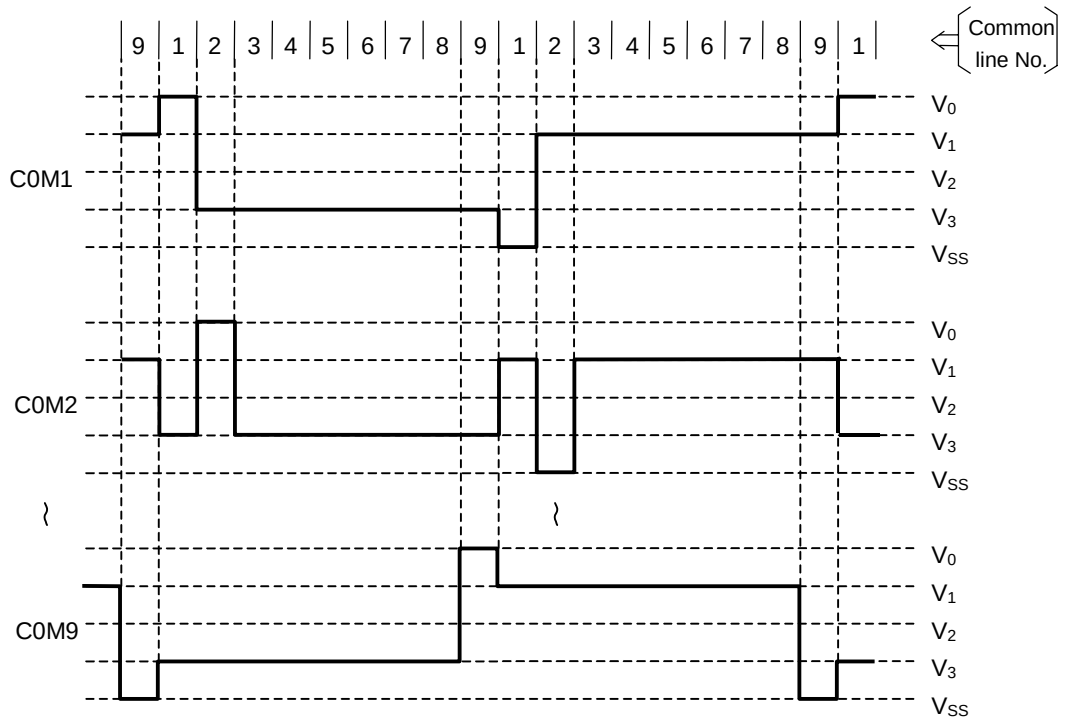


A non-selectable waveform is output from COM9 and COM10 outputs.

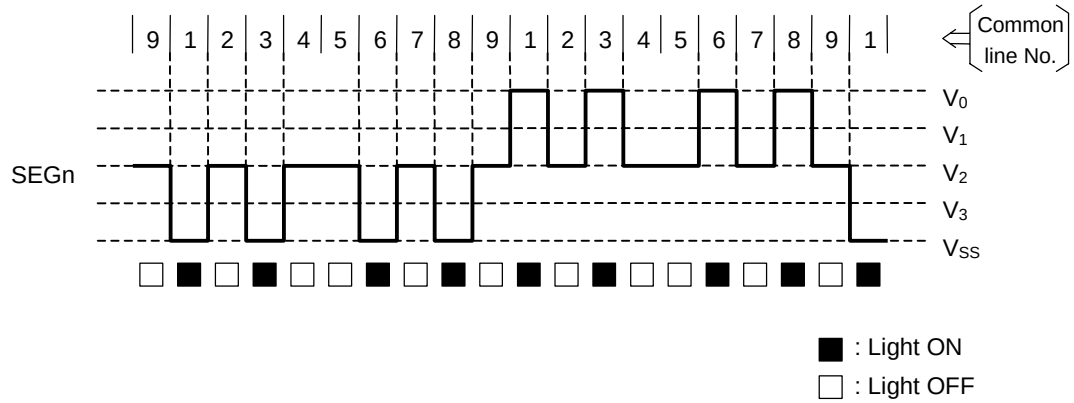


Liquid Crystal Driving Waveform Example (2)

1/9 duty (1/4 bias)

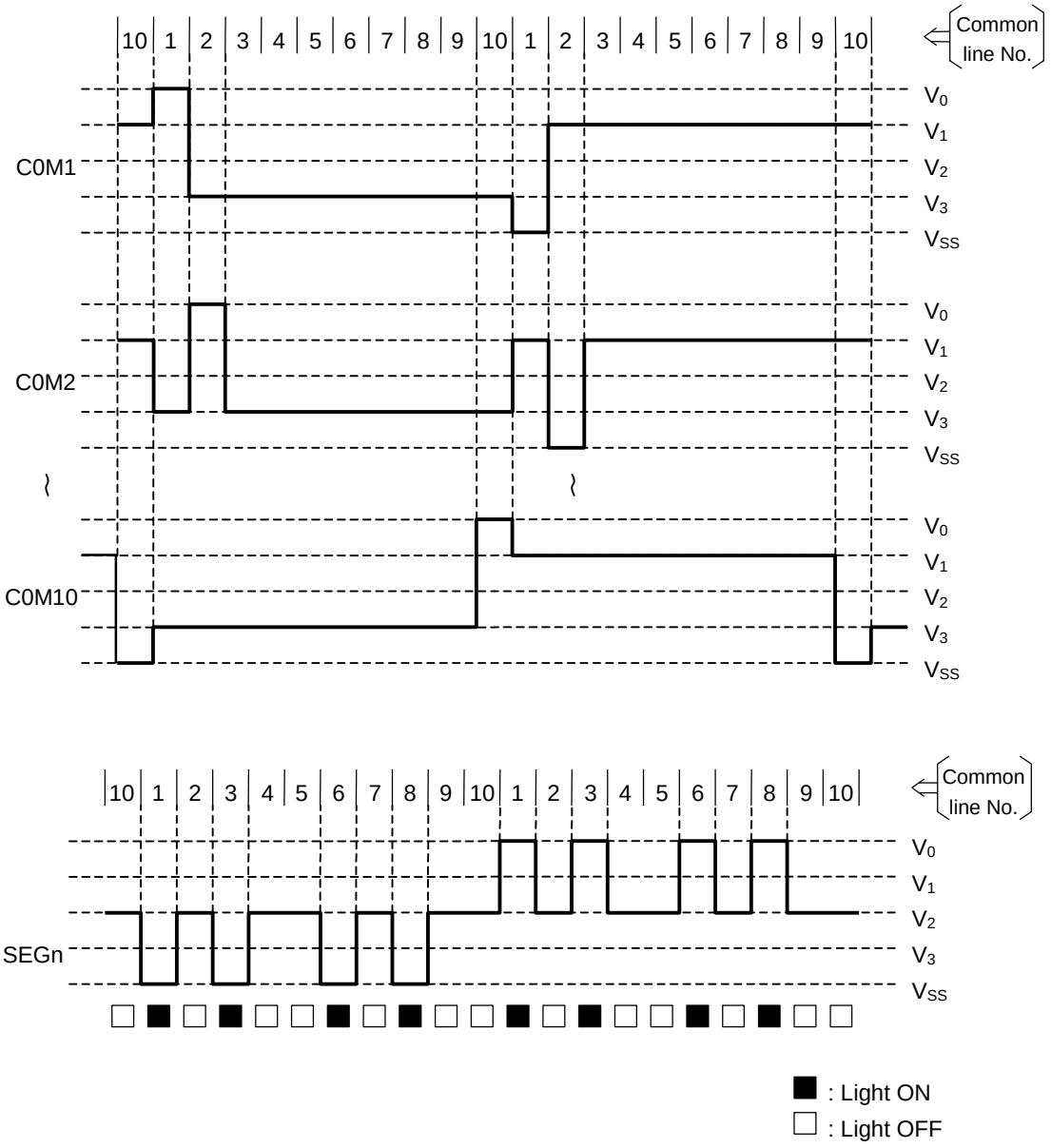


A non-selectable waveform is output from the COM10 output.

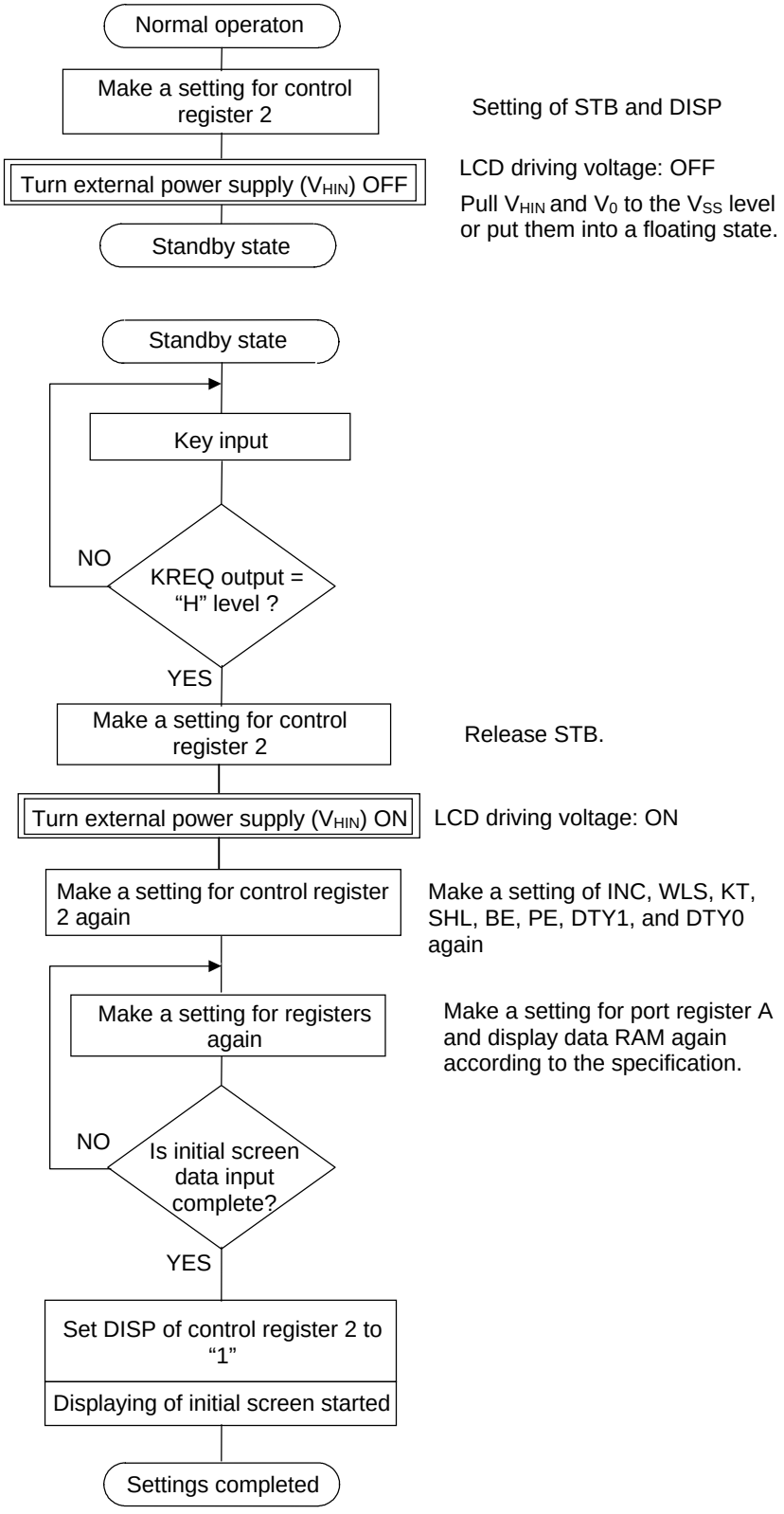


Liquid Crystal Driving Waveform Example (3)

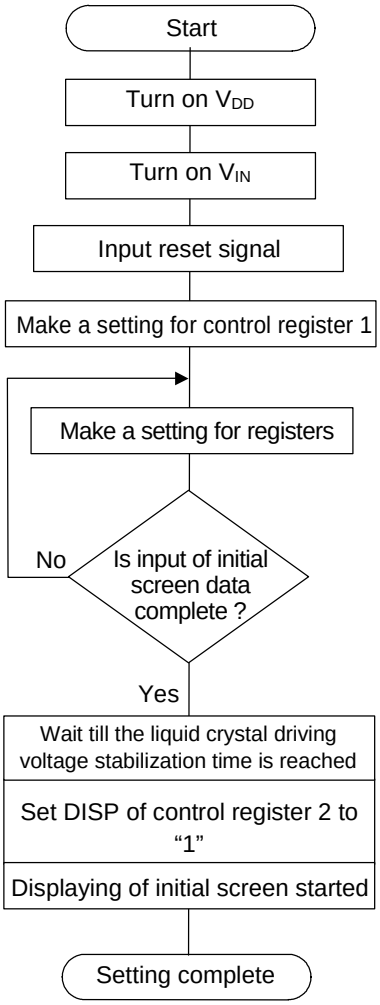
1/10 duty (1/4 bias)



Flowchart for Setting the Standby Mode and Releasing the Standby Setting with KREQ by Key Input
(Applies to the ML9092-03/04)



Power-On Flowchart



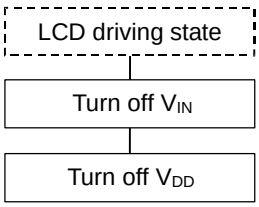
External reset or power-on reset

Make a setting for INC, WLS, KT, SHL, BE, PE, DTY1, and DTY0.

Make a setting for port register A, port register B, port register C, port register D, and display data RAM according to specifications.

Wait till the VOUT voltage stabilizes when the voltage doubler is used.

Power-Off Flowchart

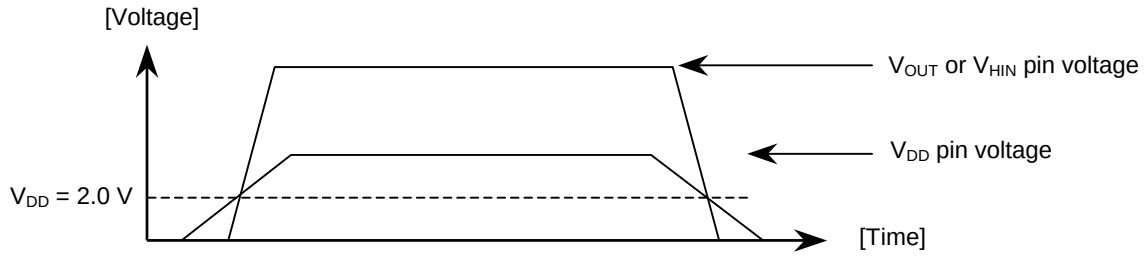


[Caution]

- The lines between output pins, and between output pins and other pins (input pins, I/O pins or power supply pins), should not be short circuited.

PRECAUTIONS WHEN TURNING ON THE POWER SUPPLY

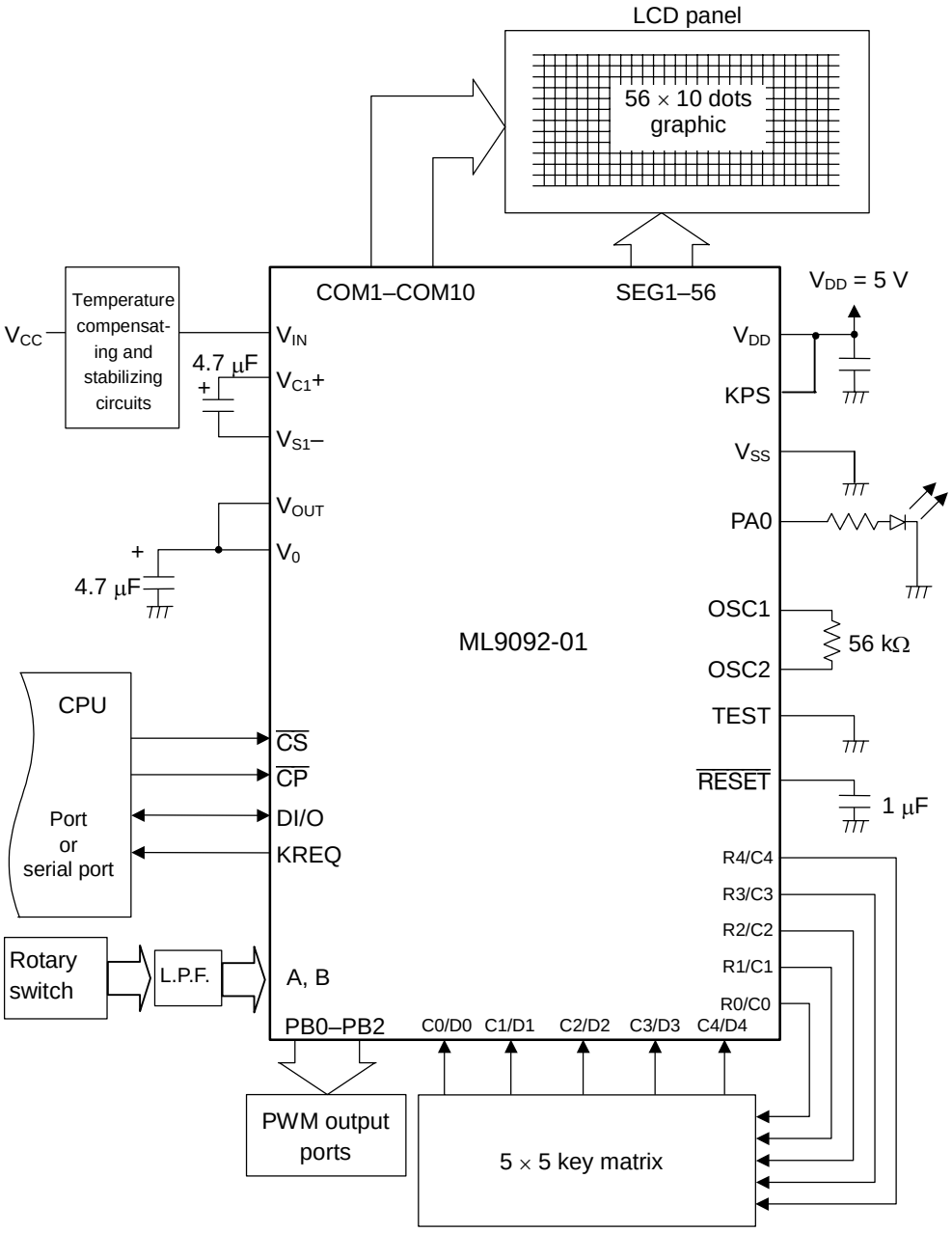
To prevent the device from malfunctioning, observe the following power-on/off sequence:
For power-on, first turn on the logic power supply (V_{DD}), then turn on the voltage doubler reference voltage (V_{IN}) or high voltage (V_{OUT} or V_{HIN}).
For power-off, first turn off the voltage doubler reference voltage (V_{IN}) or high voltage (V_{OUT} or V_{HIN}), then turn off the logic power supply (V_{DD}).



Power-On Sequence

APPLICATION CIRCUIT

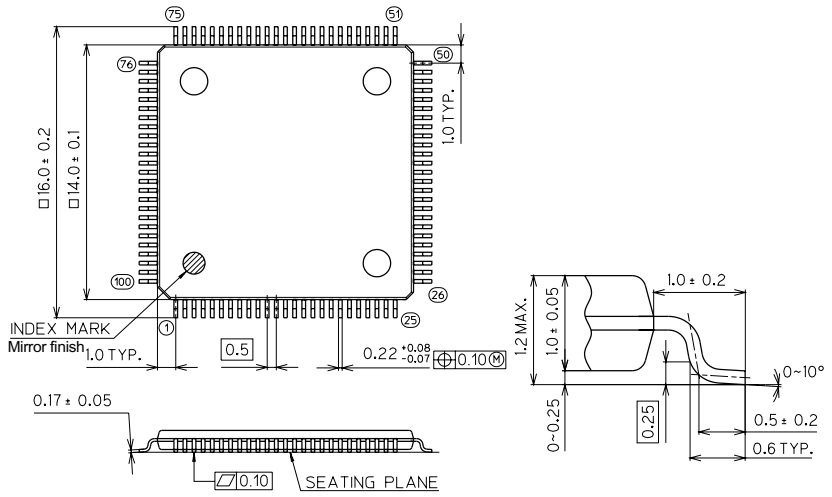
Application Example—1/10 duty, 1/4 bias, voltage doubler used (internal contrast adjustment not used)



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9092-01	Nov. 4, 2003	—	—	First edition

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.