National Semiconductor

MM5445, MM5446, MM5447, MM5448
VF Display Drivers

General Description

The MM5445 through MM5448 are monolithic MOS integrated circuits utilizing P-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. They are available in 40-pin molded dual-in-line packages. Each output can source up to 500 μA at 2.0V maximum output voltage. A single pin controls the VF display brightness by setting the positive output voltage level.

- Wide power supply operation
- TTL compatibility
- 33, 34 or 35 outputs, 500 μA source capability
- Alphanumeric capability
- Input data format compatible with MM5450, MM5451 LED drivers and MM5452, MM5453 LCD drivers

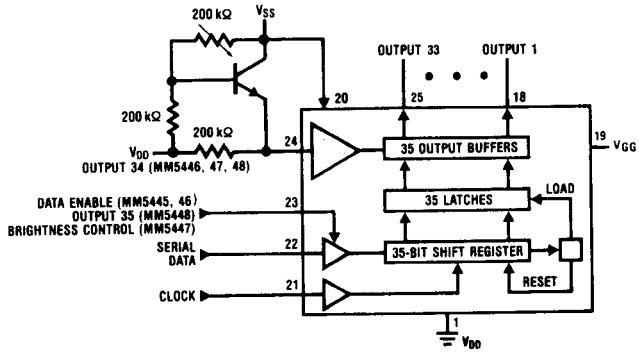
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5445 and MM5446)

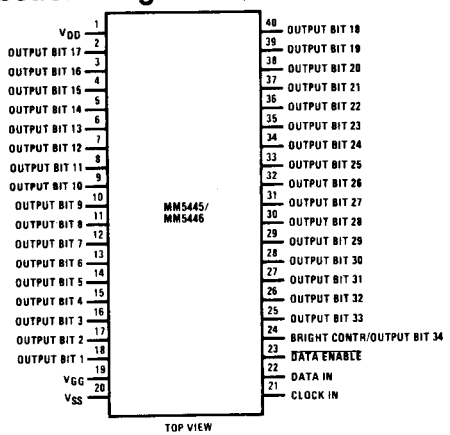
Applications

- COPS or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

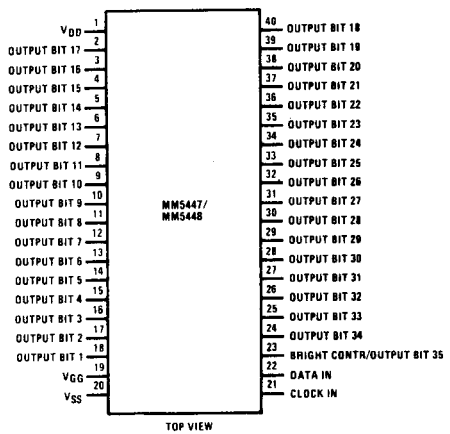


Connection Diagrams (Dual-In-Line Packages)



Order Number MM5445N, MM5446N
NS Package N40A

Figure 2a



Order Number MM5447N, MM5448N
NS Package N40A

Figure 2b

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Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}-30V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	560 mW at +85°C
	1W at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating range, $V_{DD}=0V$, $V_{SS}=4.5$ to 5.5V, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply					
V_{SS}		4.5	5.0	5.5	V
V_{GG}	$V_{SS}=5V$	−25		−7	V
V_{SS}	$V_{DD}=V_{GG}=0$	12		18	V
Power Supply Current					
I_{SS}	$V_{SS}=5V$, $V_{GG}=-25V$			9	mA
I_{GG}	$V_{DD}=0$	−2			mA
Brightness Control	With respect to V_{SS}	$(V_{SS}-V_{GG})/2$		V_{SS}	V
Input Logic Levels					
Logic "0" Level	$-25V \leq V_{GG} \leq -7V$	−0.3		0.7	V
Logic "1" Level	$-25V \leq V_{GG} \leq -7V$	2.2		$V_{SS}+0.3$	V
Logic "0" Level	$V_{DD}=V_{GG}=0$	−0.3		1	V
Logic "1" Level	$V_{DD}=V_{GG}=0$	$V_{SS}-1$		$V_{SS}+0.3$	V
Input Currents					
DATA IN and CLOCK		−10		10	μA
DATA ENABLE		−10		35	μA
BRIGHTNESS CONTROL	Excluding Output Loads (Note 2)			2	mA
Output Source Current					
Segment OFF	$V_{OUT}=(V_{SS}-V_{GG})/2$			−2	μA
Segment ON	$V_{OUT}=V_{SS}-2V$ (Notes 1 and 2)	500			μA
Input Clock Frequency		0		250	kHz
Duty Cycle		40	50	60	%
Output Matching	$I_{OUT}=500\mu A$	−0.5		0.5	V

Note 1: With Brightness Control tied to V_{SS} (MM5445 and MM5447) and $V_{GG}=-25V$.

Note 2: All output source current is provided from the Brightness Control input pin (MM5445 and MM5447).

Functional Description

The MM5445 Series are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Character generation is done external to the MM5445 Series. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the positive output voltage level.

A block diagram is shown in *Figure 1.*

Figure 2 shows the pin-out of the MM5445 series. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate VF display segment.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between data, clock and data enable. A maximum clock frequency of 250 kHz is assumed.

Typical Applications

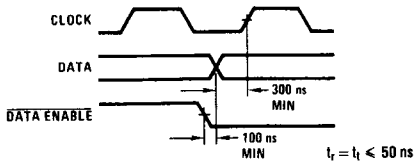


Figure 3

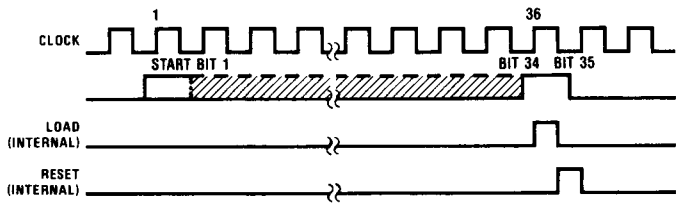
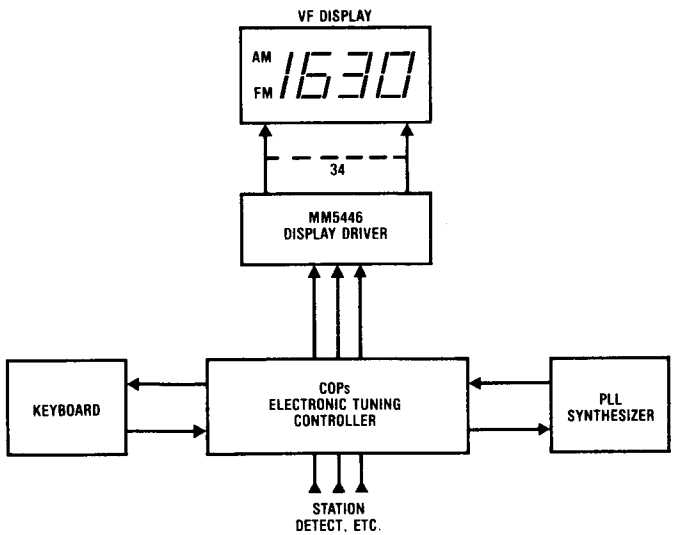


Figure 4. Input Data Format



Basic Electronically Tuned Radio System

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