Leiditech

MMBZ50VD

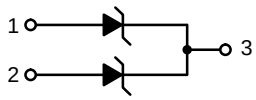
TVS Diode Array

Features

- Ultra low leakage: nA level
- Operating voltage: 48V
- Low clamping voltage
- Complies with following standards:
  - – IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±20kV
    - Contact discharge: ±15kV
  - – IEC61000-4-4 (EFT) 40A (5/50ns)
  - – IEC61000-4-5 (Lightning) 3.5A (8/20μs)
- RoHS Compliant

Dimensions SOT-23

Pin Configuration



PIN 1. ANODE
2. ANODE
3. CATHODE

Applications

- Cell Phone Handsets and Accessories
- Microprocessor based equipment
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops, and Servers
- Portable Instrumentation
- Networking and Telecom
- Serial and Parallel Ports.
- Peripherals

Mechanical Characteristics

- Package: SOT-23
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0
- Quantity Per Reel:3,000pcs
- Reel Size:7inch

Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppp	273	W
ESD per IEC 61000−4−2 (Air)	V_{ESD}	±20	Kv
ESD per IEC 61000−4−2 (Contact)		±15	
Operating Temperature Range	T_J	-55 to +125	℃
Storage Temperature Range	T_{STJ}	-55 to +150	℃

Electrical Characteristics(TA=25°C unless otherwise specified)

Part Number	Device Marking	V_{RWM} (V)	V_{BR} (V) (Typ.)	I_T (mA)	V_C @1A	Vc		I_R nA (Max)	C (Pf) (Typ.)
						(Max)	(@A)		
MMBZ50VD	SPP	48	49.5	1	62	78	3.5	1	22

TYPIC CHARACTERISTICS

Figure 1. 8 x 20 μs Waveform

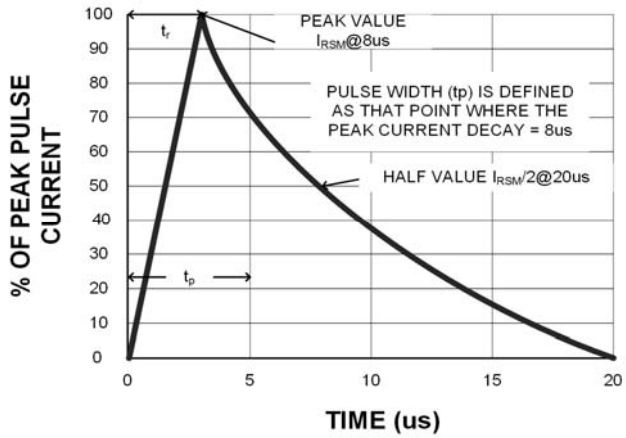


Figure 2. Power Derating Curve

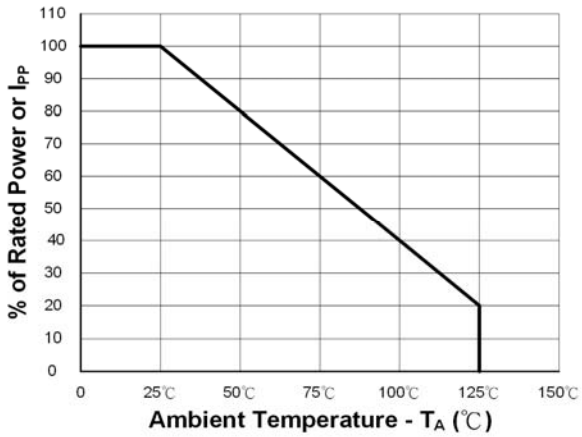
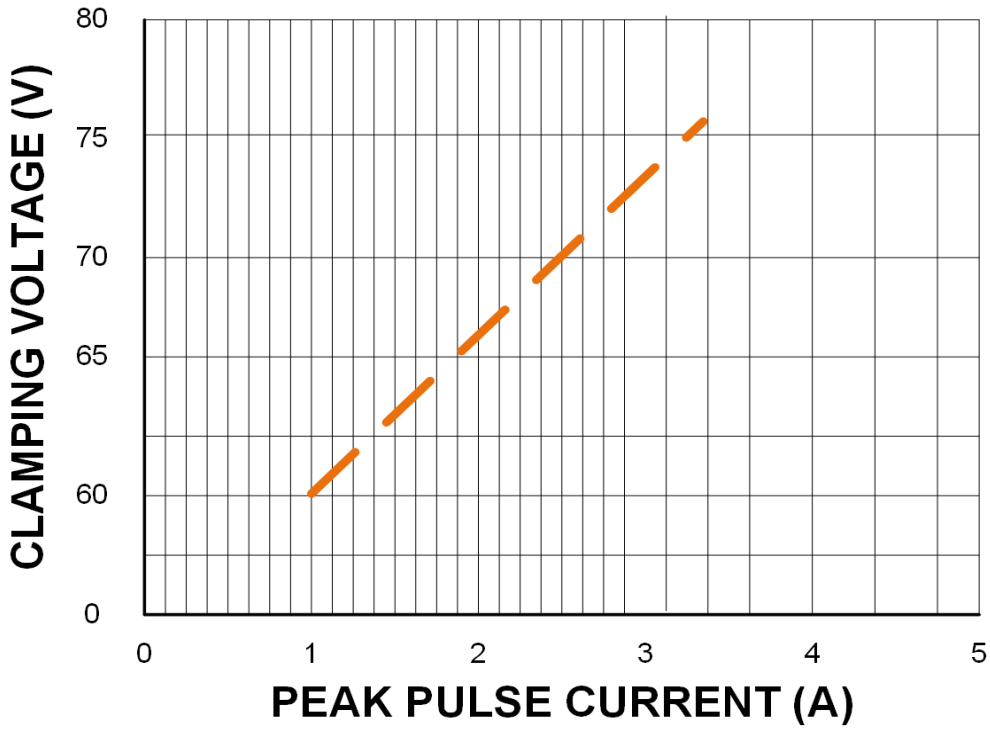


Figure 3. Clamping Voltage vs. Peak Pulse Current (tp=8/20 μs)



TYPIC CHARACTERISTICS

Figure 5. Typic Breakdown Voltage vs. Temperature

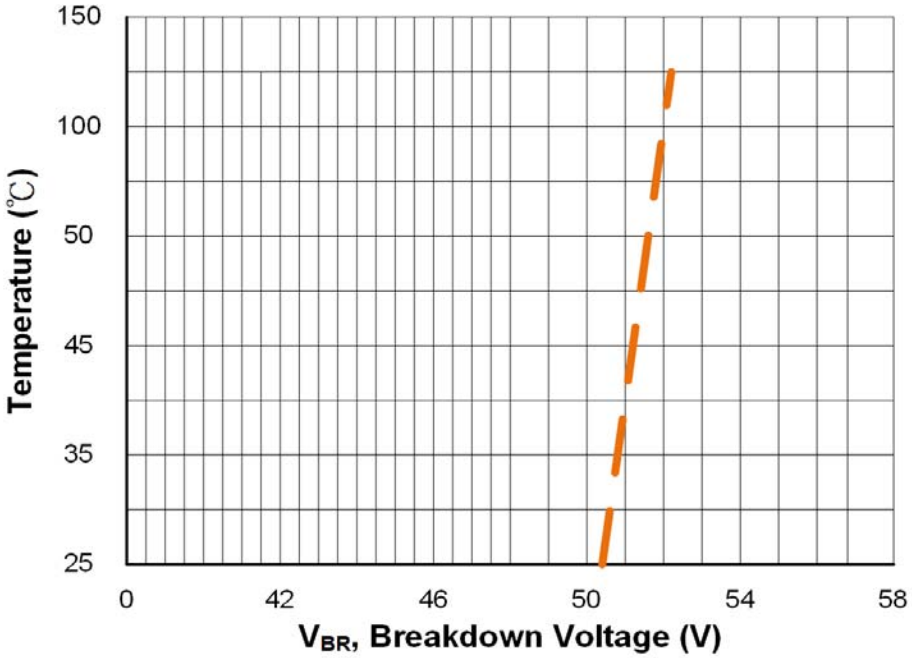
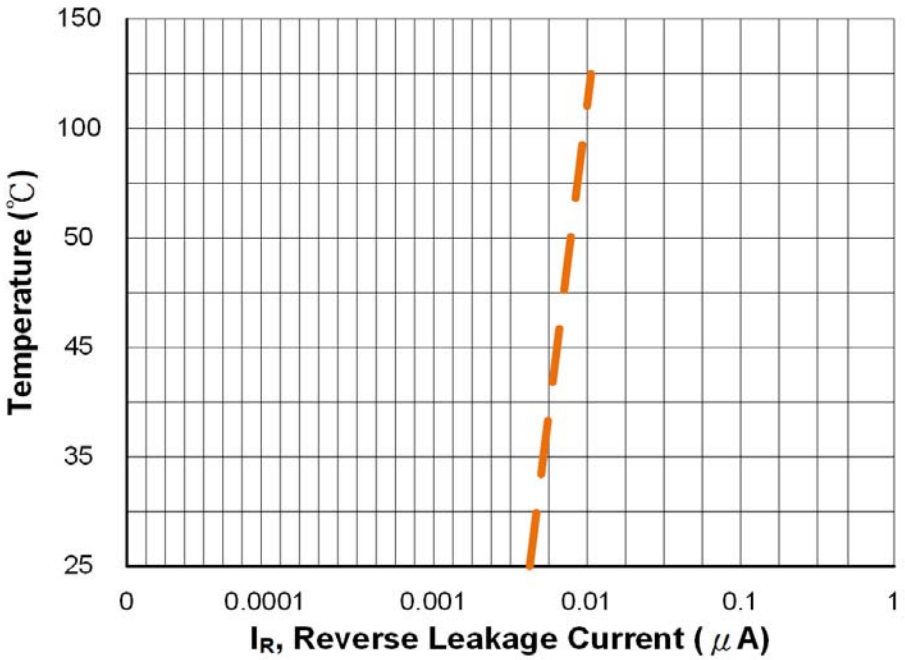
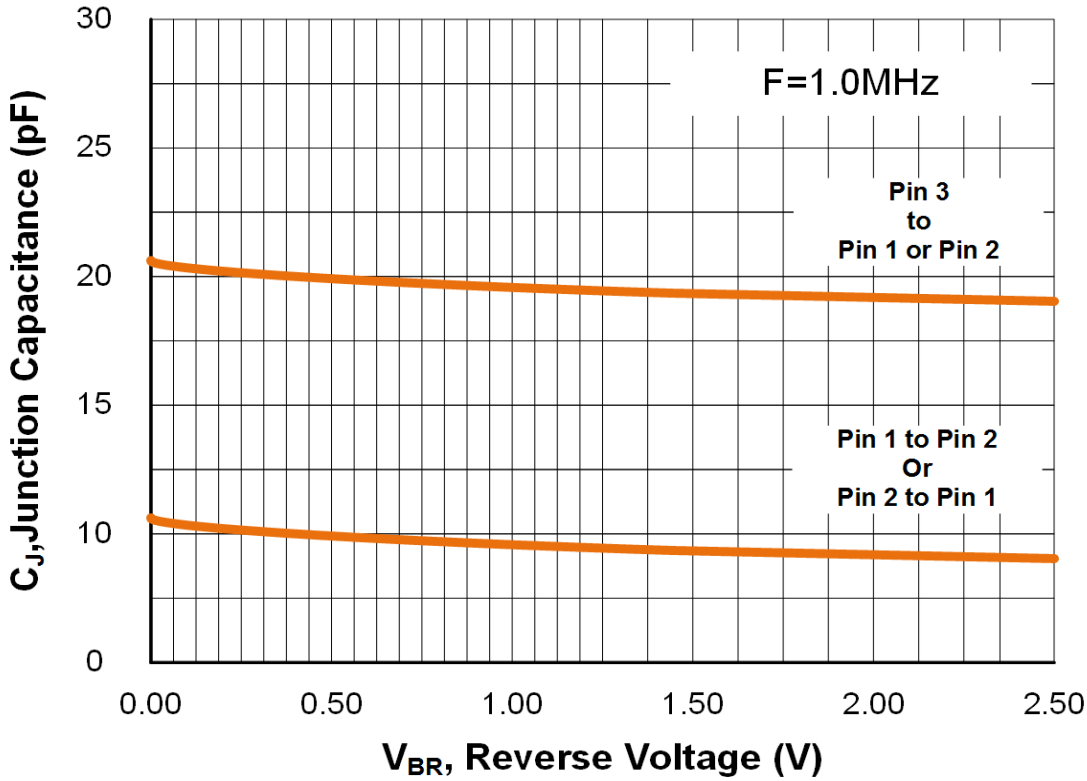


Figure 5. Typic Reverse Current vs. Temperature



TYPIC CHARACTERISTICS

Figure 6. Typic Capacitance vs. Reverse Voltage



APPLICATION INFORMATION

Figure 9. Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

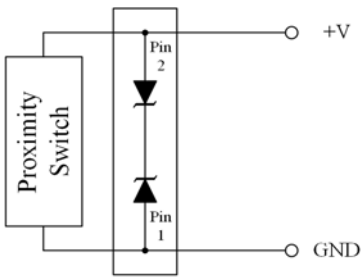
1.1. In Latchup Protection, the ESD protection device should be placed between the DC coupling capacitors and the I/O connector on the I/O differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

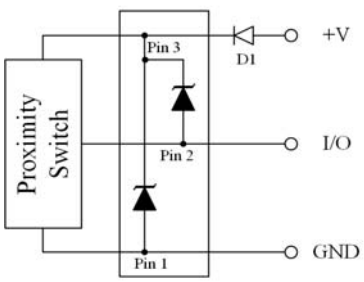
2.1. Use curved traces when possible to avoid unwanted reflections.

2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

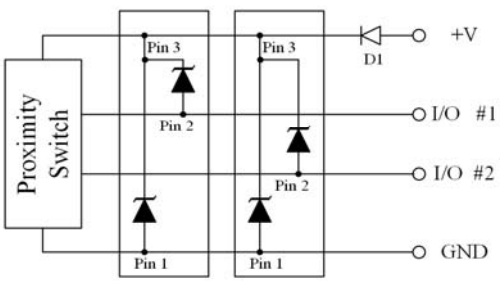
2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



2-Wire Sensor Circuit Protection

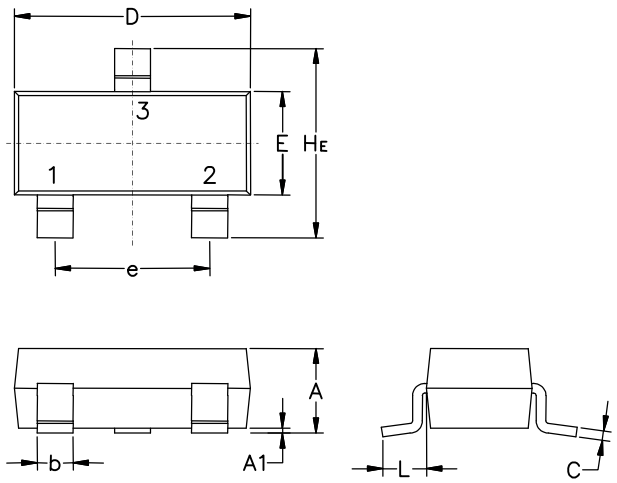


3-Wire Sensor Circuit Protection



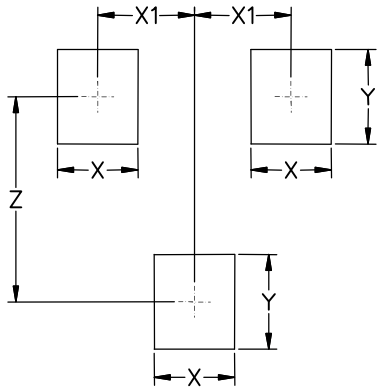
4-Wire Sensor Circuit Protection

SOT-23 Package Outline & Dimensions



Symbol	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.15	0.18	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

Soldering Footprint



Symbol	Millimeters	Inches
X	0.80	0.031
X1	0.95	0.037
Y	0.90	0.035
Z	2.00	0.079

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059