14-STAGE RIPPLE-CARRY BINARY COUNTER/ DIVIDER AND OSCILLATOR

GENERAL DESCRIPTION

The MMC 4060 is a monolithic i.c. processed in standard Al-gate CMOS technology. This device consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\varnothing_I$ (and $\varnothing_O$) A high level on the RESET line resets the counter to the all 0's state and disables the oscillator. Schmitt trigger action on the clock line permits unlimited clock rise and fall times. All inputs and outputs are fully buffered.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common reset

ABSOLUTE MAXIMUM RATINGS

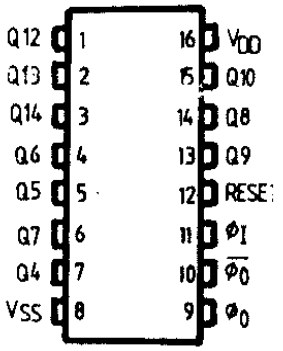
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_{IO}\|$ (μA)	V_{DD} (V)	VALUES T_{LOW} min.	T_{LOW} max.	25°C min.	25°C typ	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

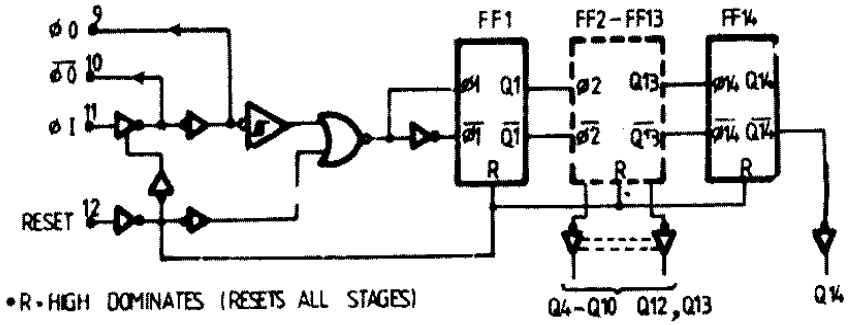
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	Min.	Typ.	Max.	
Input-pulse operation							
t_{PLH} t_{PHL}	Propagation delay time (Ø to Q4 Out)		5		370	740	ns
			10		150	300	
			15		100	200	
t_{PLH} t_{PHL}	Propagation delay time (Qn to Q_{n+1})		5		100	200	ns
			10		50	100	
			15		40	80	
t_{TLH} t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Input pulse width	f = 100 kHz	5		50	100	ns
			10		20	40	
			15		15	30	
t_r, t_f	Input rise and fall time		5	Unlimited			µs
			10				
			15				
f_{max}	Maximum clock input frequency		5	3.5	7		MHz
			10	8	16		
			15	12	24		
Reset operation							
t_{PLH}	Propagation delay time		5		180	360	ns
			10		80	160	
			15		50	100	
t_W	Reset pulse width		5		60	120	ns
			10		30	60	
			15		20	40	
RC operation							
Variation of frequency (Unit-to-Unit)		C_x = 200 pF R_S = 560 kΩ R_x = 50 kΩ	5	18	21.5	25	kHz
			10	20	23	26	
			15	21.1	24	27	
Variation of frequency with voltage (Same Unit)		C_x = 200 pF R_S = 560 kΩ R_x = 50 kΩ	5V to 10 V	–	–	2	
			10 V to 15 V	–	–	1	
R_x max		C_x = 10 µF	5	–	–	20	MΩ
		= 50 µF	10	–	–	20	
		= 10 µF	15	–	–	10	

PARAMETER	TEST CONDITIONS		VALUES			UNIT
		V_{DD}(V)	Min.	Typ.	Max.	
C_x max	R_x = 500 kΩ	5	–	–	1000	pF
	= 300 kΩ	10	–	–	50	
	= 300 kΩ	15	–	–	50	
Maximum Oscillator Frecquency*	R_x = 5 kΩ	10	530	650	810	kHz
	C_x = 15 pF	15	690	800	940	

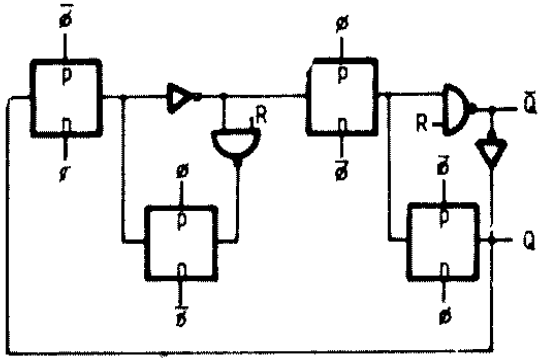
* RC oscillator applications are not recommended at supply voltages below 7 V for R_x = 50 kΩ

LOGIC DIAGRAM



•R = HIGH DOMINATES (RESETS ALL STAGES)
▲COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE-GOING TRANSITION OF ø I (AND ø 0)

Detail of tipical flip-flop stage



APPLICATIONS