❑ MN103004J / 04K / F04K

Type	**MN103004J / 04K / F04K**
Command ROM (×64-Bit)	192 KB / 128 KB / 256 KB (Flash)
Data RAM (×32-Bit)	4 KB / 10 KB / 12 KB
Minimum Instruction Execution Time	**MN103004J / 04K:** **30 ns (at 2.2 V, 33 MHz)** **MN103004J / 04K:** **25 ns (at 3.0 V, 40 MHz)** **MN1030F04K:** **36 ns (at 3.0 V, 28 MHz, 40 MHz (under development))**
Interrupts	• RESET • IRQ × 8 • NMI × 1 • Timer × 22 • Input Capture × 14 • PWM × 4 • SIF × 16 • DMAC × 4 • WDT • A/D • System error
Timer Counter	**Timer Counter 0 to 3: 32-Bit × 1** (Interval Timer, Event Count, Toggle Output, Interrupt, A/D Conversion Trigger) Clock Source: IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source: Underflow of Timer Counter 0, 1, 2, 3 **Timer Counter 4 to 7: 32-Bit × 1** (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing) Clock Source: IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source: Underflow of Timer Counter 4, 5, 6, 7 **Timer Counter 8 to B: 32-Bit × 1** (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing) Clock Source: IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source: Underflow of Timer Counter 8, 9, A, B * Each of Timer Counters 0 to 3, 4 to 7, and 8 to B can be Changed to an 8-, 16-, or 24-Bit Timer Counter **Timer Counter 10 to 13: 16-Bit × 4** (Interval Timer, Event Count, Toggle Output, Interrupt, DMA Start) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter 0, 1, 2 Interrupt Source . . . Underflow of Timer Counter 10, 11, 12, 13 **Timer Counter 14, 15: 16-Bit × 2** (Interval Timer, Event Count, Toggle Output, PMW Output, Interrupt, Input Capture (2 Lines), One-Shot Output, External Trigger Start, Generation of Timer Synchronous Output Timing, DMA Start) Clock Source . .. . IOCLK, IOCLK/8, External Clock Input (2 Lines), Underflow of Timer Counter 0, 1, 2-Phase Encode Interrupt Source: Overflow of Timer 14, 15, Underflow of Timer 14, 15, Coincidence of Compare Register with Binary Counter or at Capture **Watchdog Timer: 16- to 25-Bit × 1ch**
DMA Controller	Number of Channels 2 Unit of Transfer 8/16/32 bits Max Transfer Cycles 65535 Staring Factor External Interrupt, Timer Factor, PNM Factor, Serial Transmission/Reception Factor, A/D Conversion finish, Software Factor Transfer Method 2-Bus Cycle Transfer Adressing Modes Fixed, Increment, Decrement Transfer Modes Word Transfer, Burst Transfer, Intermittent Transfer
Serial Interface	**Serial 0, 1: 7-, 8-Bit × 2** (Clock Synchronous Mode, Start-Stop Synchronous Mode, I^2C Mode) **Serial 2: 7-, 8-Bit × 1** (Start-Stop Synchronous Mode) **Serial 3 to 7: 7-, 8-Bit × 5** (Clock Synchronous Mode) Clock Source: (Clock Synchronous Mode, Start-Stop Synchronous Mode) IOCLK, Underflow of Timer Counter, External Clock (I^2C Mode) IOCLK, Underflow of Timer Counter

I/O Pins	**I/O**	**155**	• Common use 137
	Input	**16**	• Common use 16
A/D Inputs	10-Bit × 16ch		
PWM	12-, 14-Bit resolution × 4ch (dedicated), 16-Bit resolution × 2ch (Common with Timer)		
ICR	28-Bit × 13ch + 16-Bit × 4ch (Common with Timer)		
OCR	16-Bit × 4ch (Common with Timer)		
Timer Synchronous Output	4-Bit (Synchronous Output) × 2ch		
Package	QFP208-P-2828A (MN103004J / 04K / F04K), FLGA239-C-1313 (MN103004K / F04K)		
Electrical Characteristics	MN103004J / 04K		

Supply Current

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating Supply Current	IDD1	VDDH, VDDB, VDD, PVDD, AVDD = 3.0 V VI = VDDH (VDDB) or VSS At internal = 40 MHz Output released			150	mA
Supply current at stopping	IDD4	VDD, PVDD, AVDD = 3.6 V VI = VDDH (VDDB) or VSS Fosc = Oscillation stopped Output released			150*	µA

***FLGA239-C-1313 (Ta = –20 °C to +85 °C)**

A/D Conversion Performance

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3.0 V A/D conversion clock = 5 MHz			±7	LSB
A/D conversion relative Error					±5	LSB
A/D conversion time			2.8			µs

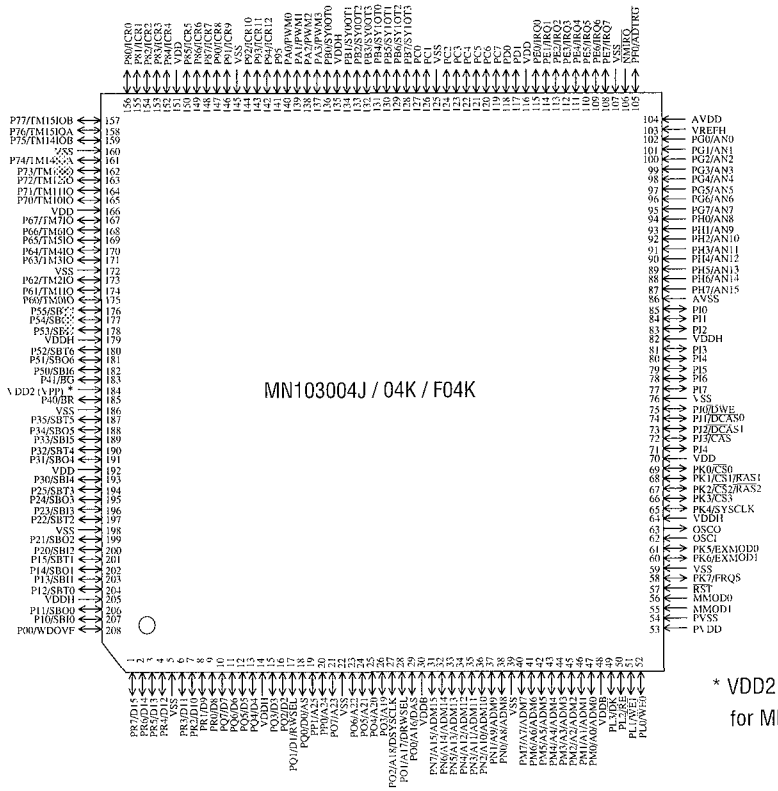
(Ta = –20 °C to +85 °C, AVDD = 3.0 V, AVSS = 0.0 V)

Support Tool

In-Circuit Emulator	PX-ICE103004

See the next page for pin assignment.

Pin Assignment



QFP208-P-2828A

* VDD2 for MN103004K or MN103004J and VPP for MN1030F04K

Perspective

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
T			PE7 IRQ7	$\overline{\text{NMIRQ}}$	PE1 IRQ1	PD0	PC4	PC1	PB1, SY0OT1	PA2, PWM2	P94 ICR12	P91, ICR9	P84 ICR4	P80, ICR0			T
R				PE5 IRQ5	PE3 IRQ3	VDD	PC2	PB7, SY1OT3	PB3, SY0OT3	PA0, PWM0	P92, ICR10	P85, ICR5	P82, ICR2				R
P	AVDD		P55, $\overline{\text{ADTRG}}$	VSS	PE4 IRQ4	PC6	PC5	VSS	PB5, SY1OT1	PB0 SY0OT0	VSS	VDD	P87, ICR7	P77 TM15IOB		P76, TM15IOA	P
N	PG2 AN2	PG0 AN0	VREFH	PE6, IRQ6	PE2, IRQ2	PD1	PC3	PB6, SY1OT2	VDDH	PA1, PWM1	P90, ICR8	P83, ICR3	P74, TM14IOA	P75, TM14IOB	P73, TM13IO	VSS	N
M	PG3, AN3	PG5 AN5	PG1 AN1	PG4, AN4	PE0, IRQ0	PC7	PC0	PB2, SY0OT2	PA3 PWM3	P95	P86, ICR6	P81, ICR1	P70, TM10IO	P72, TM12IO	VDD	P71, TM11IO	M
L	PG7 AN7	PH1 AN9	PH2, AN10	PG6 AN6	PH3, AN11	PH0 AN8	PB4, SY1OT0			P93 ICR11	P67 TM7IO	P63, TM3IO	P65, TM5IO	VSS	P66 TM6IO	P64 TM4IO	L
K	PH7, AN15	PH5, AN13	PH6, AN14	AVSS	PI0	PI4, AN12					P60 TM0IO	P54, SBO7	P62, TM2IO	P55, SBT7	P61, TM1IO	P53, SBI7	K
I	PI2	PI3	PI4	VDDH	PI1							P41 $\overline{\text{RG}}$	VDDH	P51 SBO6	P52, SBT6	P50, SBI6	I
H	PJ0, $\overline{\text{DWE}}$	PI7	VSS	PI5	PI6							P35, SBT5	P34, SBO5	P40 $\overline{\text{BR}}$	VDD2 (VPP)	VSS	H
G	PK2 $\overline{\text{CS2}}$, $\overline{\text{RAS2}}$	PK0 $\overline{\text{CS0}}$	PK1 $\overline{\text{CS1}}$, $\overline{\text{RAS1}}$	VDD	PJ4	PJ2, $\overline{\text{DCAS1}}$					P31 SBO4	P33, SBI5	P30, SBI4	P32, SBT4	VDD	P25, SBT3	G
F	OSCO	PK4 SYSCLK	VDDH	PK3 $\overline{\text{CS3}}$	PJ3, $\overline{\text{CAS}}$	PJ1, $\overline{\text{DCAS0}}$	PN5 A13, ADM13			PO5 A21	P24, SBO3	P21, SBO2	P22, SBT2	P15, SBT1	P23, SBI3	VSS	F
E	OSCI	VSS	PK7, FRQS	PK6, EXMOD1	PK5, EXMOD0	PN1 A9, ADM9	PN3 A11, ADM11	PO0 A16 DAS	PO2 A18, DSYSCLK	PP0 A24	PQ2 D2	PR1 D9	P13, SBI1	P20, SBI2	P14 SBO1	P12, SBT0	E
D	MMOD1	$\overline{\text{RST}}$	MMOD0	PVSS	PM4 A4, ADM4	PN0 A8, ADM8	PN4 A12, ADM12	PO7 A23	PO3 A19	PQ0 D0, AS	PQ5 D5	PQ7 D7	P10, SBI0	VDDH	P11, SBO0	P00 WDOVF	D
C	PVDD		PL1, $\overline{\text{WE1}}$	PL3 $\overline{\text{DK}}$	PM2 A2, ADM2	PM6 A6, ADM6	VSS	PN7 A15 ADM15	VSS	PQ3 D3	VDDH	PR3 D11	PR4 D12	PR6 D14			C
B			PL2 $\overline{\text{RE}}$	PM0 A0, ADM0	PM1 A1, ADM1	PM5 A5, ADM5	PN6 A14, ADM14	VDDB	PO6 A22	PP1 A25	PQ6 D6	PR0 D8	PR5 D13				B
A			PL0, $\overline{\text{WE0}}$	VDDB	PM3 A3, ADM3	PM7 A7, ADM7	PN2 A10, ADM10	PO1 A17, DRWSEL	PO4 A20	PQ1 D1, RWSEL	PQ4 D4	PR2 D10	VSS	PR7 D15			A

FLGA239-C-1313

* H2 is VDD2 for MN103004K and VPP for MN1030F04K