MP7545B

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

March 1998-3

FEATURES

- Full Four Quadrant Multiplication
- 12-Bit Resolution
- Gain Error Tempco (2 ppm/°C max.)
- Latch-Up Free
- Single +5 V to +15 V Supply
- TTL/15 V CMOS Compatible
- Rugged 2000 V ESD Protection
- 3 V Version: MP75L45
- TTL/5 V VMOS Version: MP7645B
- Guaranteed Monotonic

APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Disk Drive Servo Systems
- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratiometric A/D Conversion
- Function Generation
- Digitally Controlled Filters

GENERAL DESCRIPTION

The MP7545B is a 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The MP7545B is particularly suitable for single supply operation and applications with wide temperature variations.

The MP7545B can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for V_{DD} = +5 V.

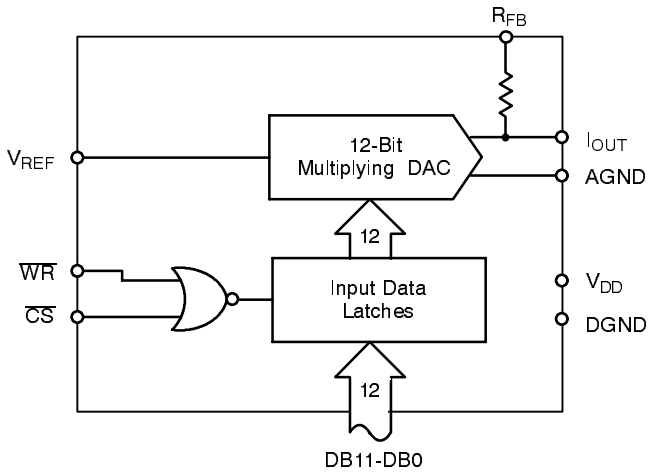

Figure 1. Simplified Block Diagram

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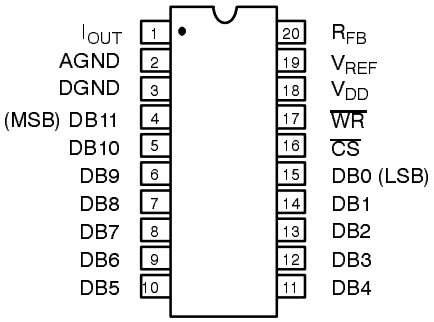
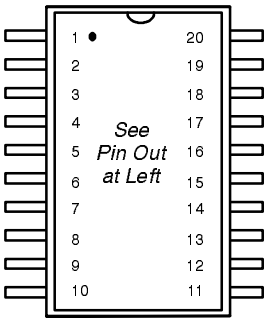
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7545BKN	±1	±1	±3
Plastic Dip	–40 to +85°C	MP7545BLN	±1/2	±1	±2
SOIC	–40 to +85°C	MP7545BKS	±1	±1	±3
SOIC	–40 to +85°C	MP7545BLS	±1/2	±1	±2
PLCC	–40 to +85°C	MP7545BKP	±1	±1	±3
PLCC	–40 to +85°C	MP7545BLP	±1/2	±1	±2

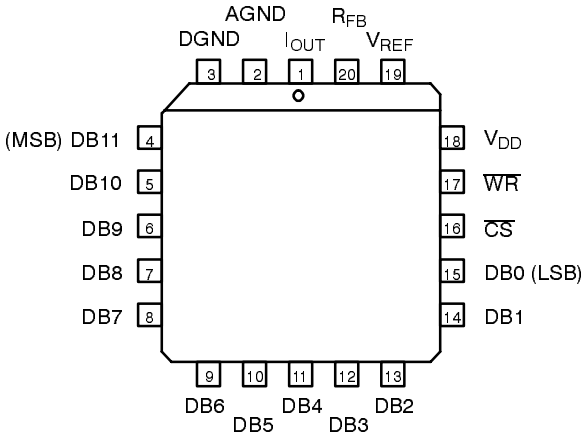
PIN CONFIGURATIONS



20 Pin PDIP (0.300")



20 Pin SOIC (Jedec, 0.300")



20 Pin PLCC

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All Grades Monotonic Over Full Temperature Range
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±3		±4		
L				±2		±3		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10		±50	nA	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			1		1	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Propagation Delay	t_{PD}		50				ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	
Control	C_{IN}			20		20	pF	
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		100				pF	DAC Inputs all 1's
	C_{OUT}		50				pF	DAC Inputs all 0's

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	100					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	
Write Pulse Width	t_{WR}	100					ns	

NOTES:

1 *Full Scale Range (FSR) is 10V for unipolar mode.*

2 *Guaranteed but not production tested.*

3 *Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.*

4 *See timing diagram.*

5 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±6		±7		
L				±5		±6		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
K, L				±10		±50		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			1		1	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20Vp-p sinewave.
Propagation Delay	t_{PD}		50				ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[2]								
DB0-DB11	C_{IN}			5		5	pF	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	C_{IN}			20		20	pF	V_{IN} = 0
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		100				pF	DAC Inputs all 1's
	C_{OUT}		50				pF	DAC Inputs all 0's

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	75					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	
Write Pulse Width	t_{WR}	75					ns	

NOTES:

1 *Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.*

2 *Guaranteed but not production tested.*

3 *Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.*

4 *See timing diagram.*

5 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +17 V

Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V

I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V

V_{REF} to GND ..... ±25 V

V_{RFB} to GND ..... ±25 V

AGND to DGND ..... ±0.5 V

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC, PLCC 900mW

Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 GND refers to AGND and DGND.

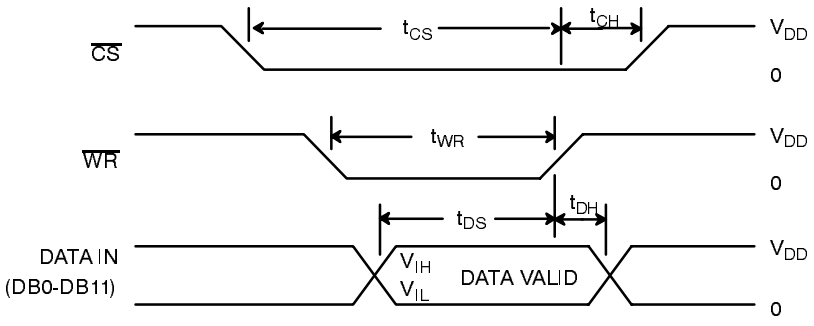


Figure 2. Write Cycle Timing Diagram

APPLICATION NOTES

Digital Section

Figure 3. shows the digital structure for one bit.

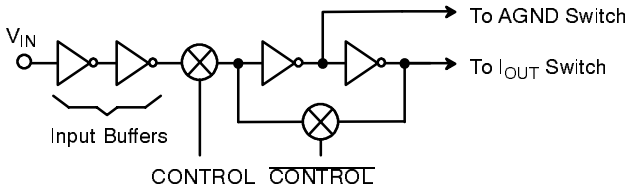


Figure 3. Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

The input buffers are simple CMOS inverters designed such that when the MP7545B is operated with V_{DD} = 5 V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The MP7545B may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15 V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

MICROPROCESSOR INTERFACING OF THE MP7545B

The MP7545B can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 4. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

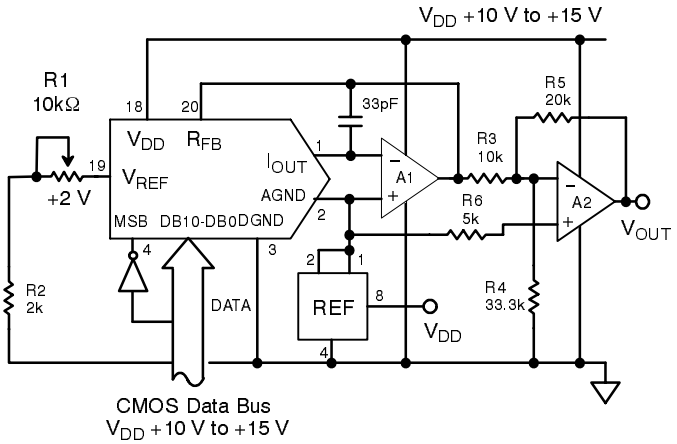


Figure 4. Single Supply "Bipolar" 2's Complement D/A Converter

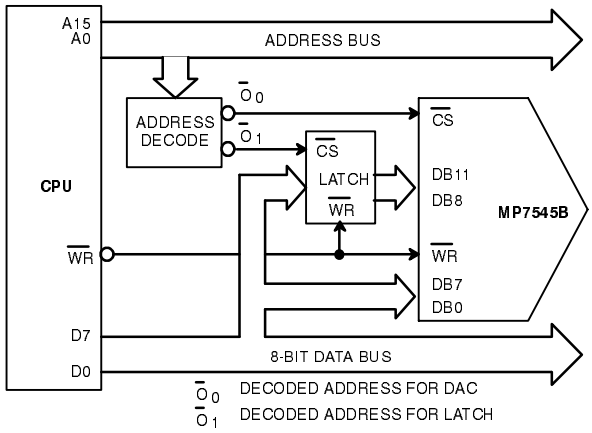


Figure 5. 8-Bit Processor to MP7545B Interface

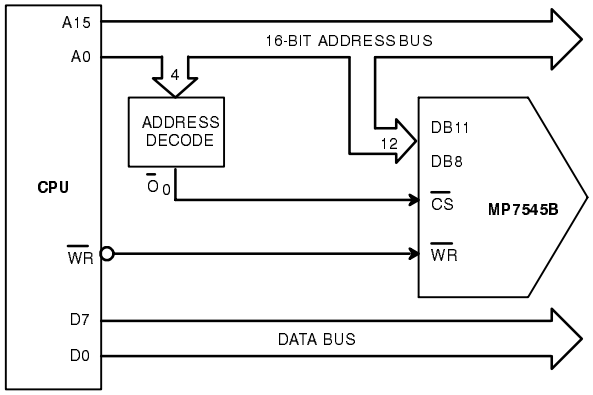
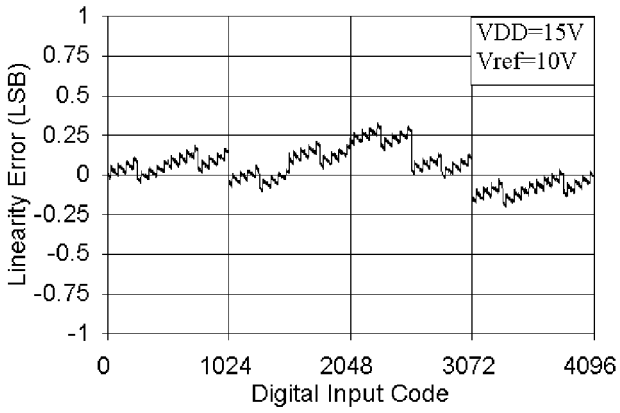


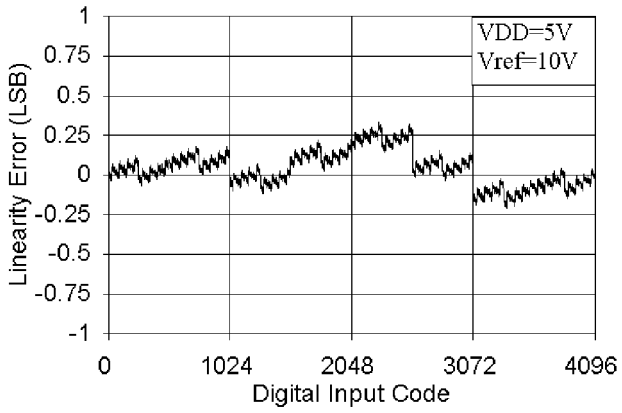
Figure 6. Connecting the MP7545B to 8-Bit Processors via the Address Bus

Figure 5. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bush such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each MP7545B connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

PERFORMANCE CHARACTERISTICS



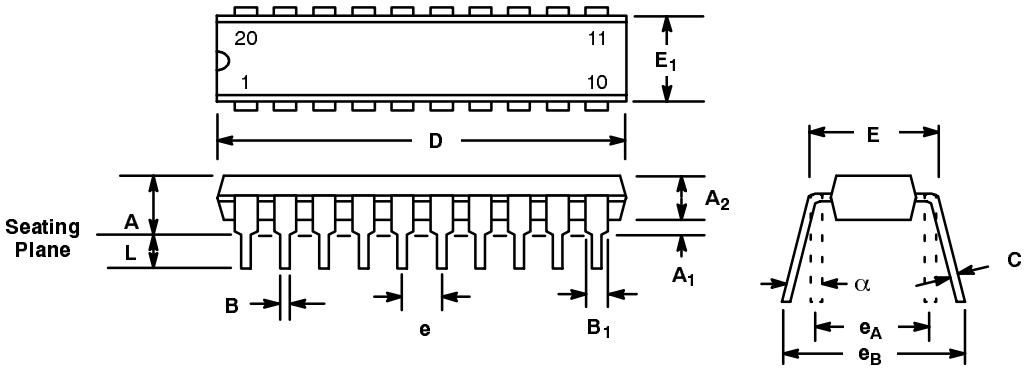
Graph 1. Linearity Error vs. Digital Input Code



Graph 2. Linearity Error vs. Digital Input Code

20 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

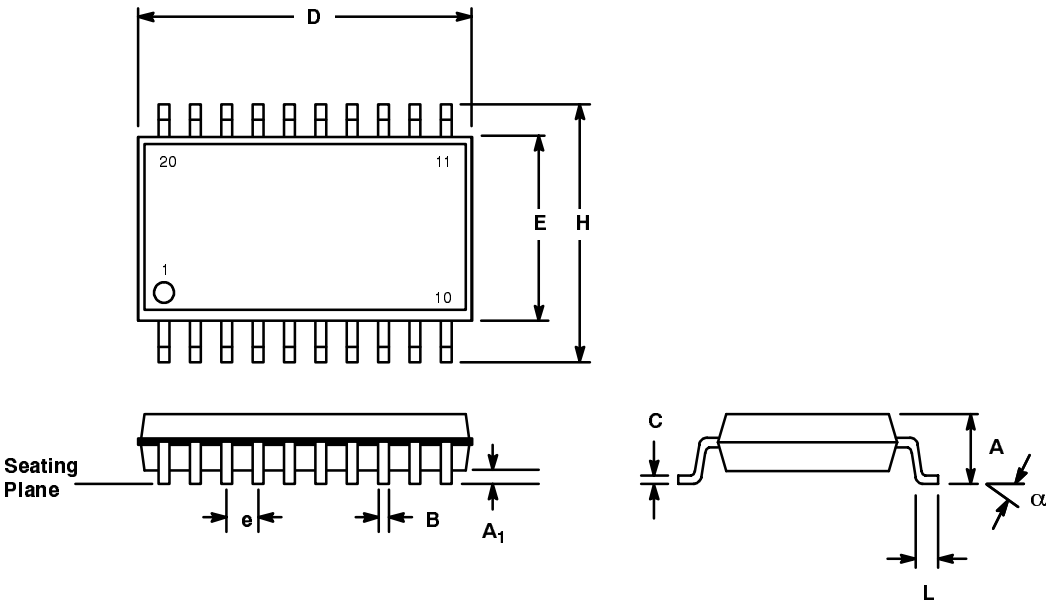


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.925	1.060	23.50	26.92
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)

Rev. 1.00

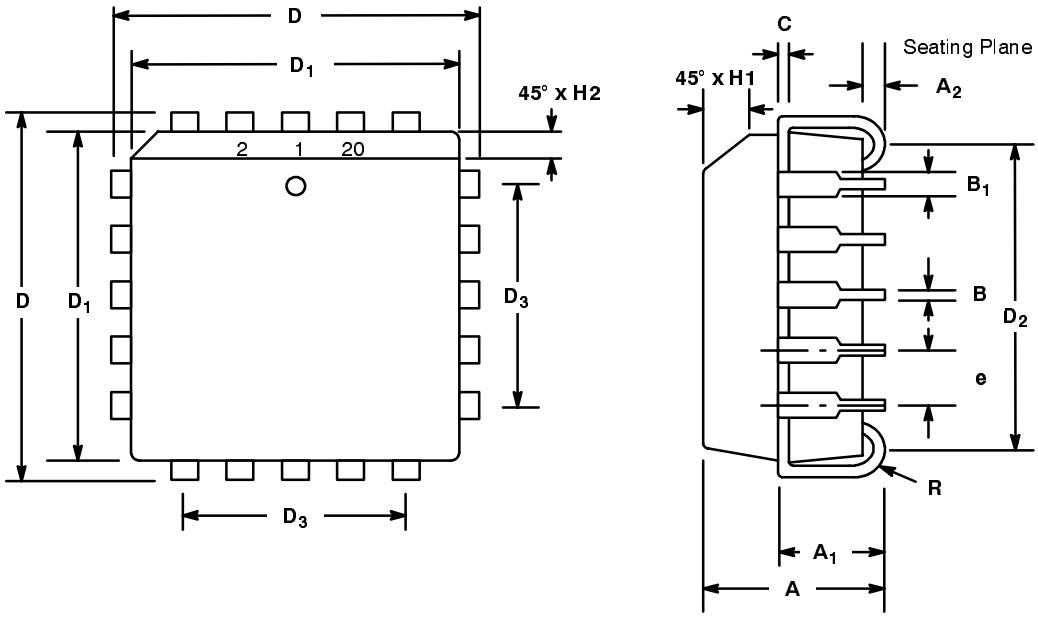


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.385	0.395	9.78	10.03
D_1	0.350	0.356	8.89	9.04
D_2	0.290	0.330	7.37	8.38
D_3	0.200 typ.		5.08 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column