MP7633

15 V CMOS
10-Bit Multiplying
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplying DAC**
- **Guaranteed Monotonic over Temperature**
- **Non-Linearity: ±1/2 LSB Achieved without Trimming**
- **Ultra Stable: 0.2 ppm/°C Max Linearity Tempco**
- **2 ppm/°C Max Gain Error Tempco**
- **Low Output Capacitance**
- **Low Sensitivity to Amplifier Offset 330 μV/mV**
- **Low Glitch Energy**
- **Low Feedthrough Error**
- **TTL/5 V CMOS Compatible**
- **Latch-Up Free**
- **Improved Replacement for AD7533, AD7520**
- **Low Cost**

APPLICATIONS

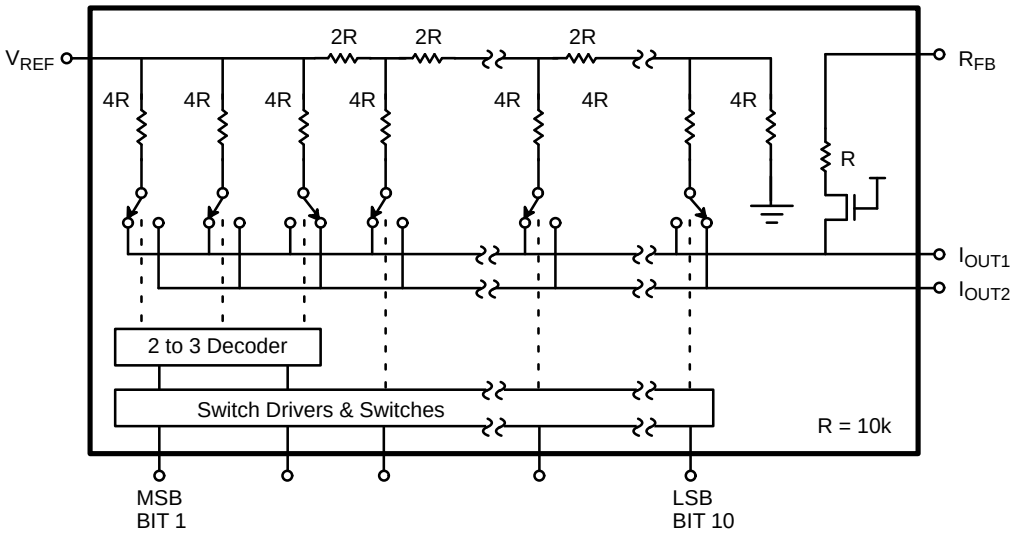
- **Digitally Controlled Attenuators**
- **Programmable Gain Amplifiers**
- **Function Generation**
- **Linear Automatic Gain Control**

GENERAL DESCRIPTION

The MP7633 is pin and functionally equivalent to industry's standard AD7533, AD7520 and AD7530. The MP7633 is recommended when lower output capacitance is required. The MP7633 incorporates a unique decoding technique yielding excellent accuracy and stability (0.2 ppm/°C linearity drift and 2 ppm/°C scale factor drift) over temperature and time.

The 2-3 bit decoding architecture of the MP7633 results in low output capacitances of 52/26pF at I_{OUT1} and 13/45pF at I_{OUT2}, low sensitivity to output amplifier offset of 330 μV per millivolt offset, eliminating the need for trim pots in many applications.

SIMPLIFIED BLOCK DIAGRAM



3 Segment D/A Converter with Termination to GND.
Logical "1" at Digital Input Steers Current to I_{OUT1}

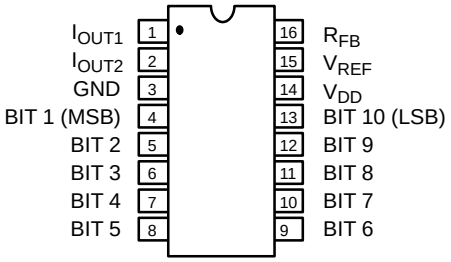
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7633JN	±2	±2	±0.4
Plastic Dip	–40 to +85°C	MP7633KN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP7633LN	±1/2	±1/2	±0.4
SOIC	–40 to +85°C	MP7633JS	±2	±2	±0.4
SOIC	–40 to +85°C	MP7633KS	±1	±1	±0.4
SOIC	–40 to +85°C	MP7633LS	±1/2	±1/2	±0.4
PLCC	–40 to +85°C	MP7633JP	±2	±2	±0.4
PLCC	–40 to +85°C	MP7633KP	±1	±1	±0.4
PLCC	–40 to +85°C	MP7633LP	±1/2	±1/2	±0.4
Ceramic Dip	–40 to +85°C	MP7633AD	±2	±2	±0.4
Ceramic Dip	–40 to +85°C	MP7633BD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP7633CD	±1/2	±1/2	±0.4
Ceramic Dip	–55 to +125°C	MP7633SD*	±2	±2	±0.4
Ceramic Dip	–55 to +125°C	MP7633TD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP7633UD*	±1/2	±1/2	±0.4

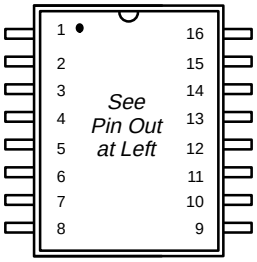
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

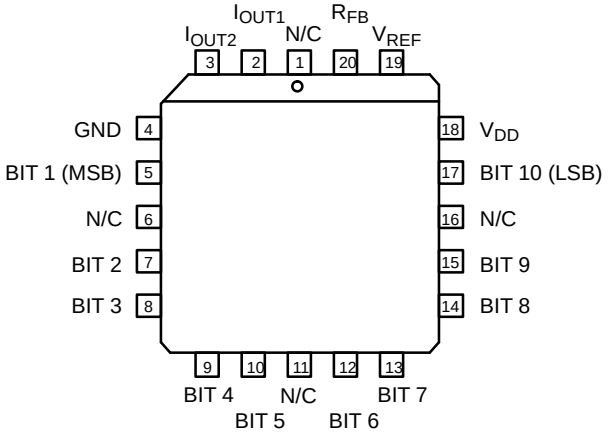
See Packaging Section for Package Dimensions



16 Pin CDIP, PDIP (0.300”)
D16, N16



16 Pin SOIC (Jedec, 0.300”)
S16



20 Pin PLCC
P20

PIN OUT DEFINITIONS

16 Pin CDIP, PDIP, SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10 (LSB)
14	V_{DD}	Positive Power Supply
15	V_{REF}	Reference Input Voltage
16	R_{FB}	Internal Feedback Resistor

20 Pin PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I_{OUT1}	Current Output 1
3	I_{OUT2}	Current Output 2
4	GND	Ground
5	BIT 1	Data Input Bit 1 (MSB)
6	N/C	No Connection
7	BIT 2	Data Input Bit 2
8	BIT 3	Data Input Bit 3
9	BIT 4	Data Input Bit 4
10	BIT 5	Data Input Bit 5
11	N/C	No Connection
12	BIT 6	Data Input Bit 6
13	BIT 7	Data Input Bit 7
14	BIT 8	Data Input Bit 8
15	BIT 9	Data Input Bit 9
16	N/C	No Connection
17	BIT 10	Data Input Bit 10 (LSB)
18	V_{DD}	Positive Power Supply
19	V_{REF}	Reference Input Voltage
20	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	10			10		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Gain Error	GE		±0.3	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$, ΔV_{DD} = ±5%
Output Leakage	I_{OUT}		<1	±10		±200	nA	I_{OUT1} V_{IN} = 0 V I_{OUT2} V_{IN} = V_{DD}
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		500	1000			ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T			1			mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
Voltage Input Range[2]			±10	±25			V	
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical “0” Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	V_{IN} = 0 V and V_{DD}
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}			52			pF	DAC Inputs all 1’s
	C_{OUT1}			26			pF	DAC Inputs all 0’s
	C_{OUT2}			13			pF	DAC Inputs all 1’s
	C_{OUT2}			45			pF	DAC Inputs all 0’s
Scale Factor[2]			100				$\mu A/V_{REF}$	
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V, 15 V

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

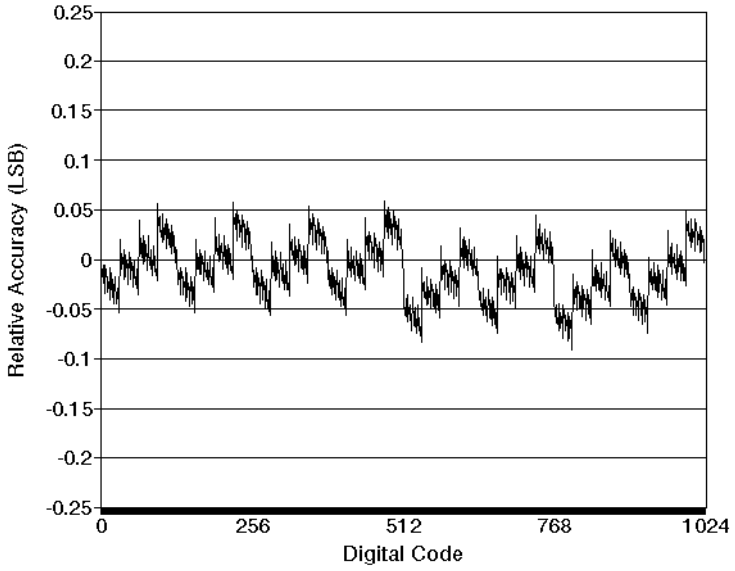
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... –0.5, +17 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND (2) ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

PERFORMANCE CHARACTERISTICS

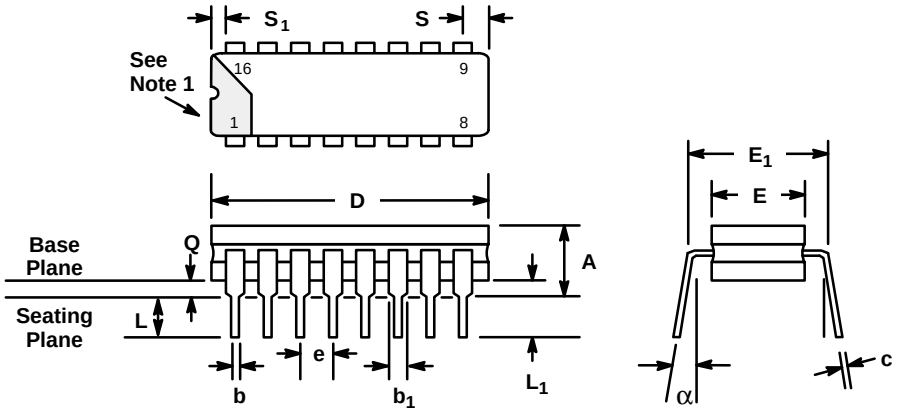


Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

16 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D16

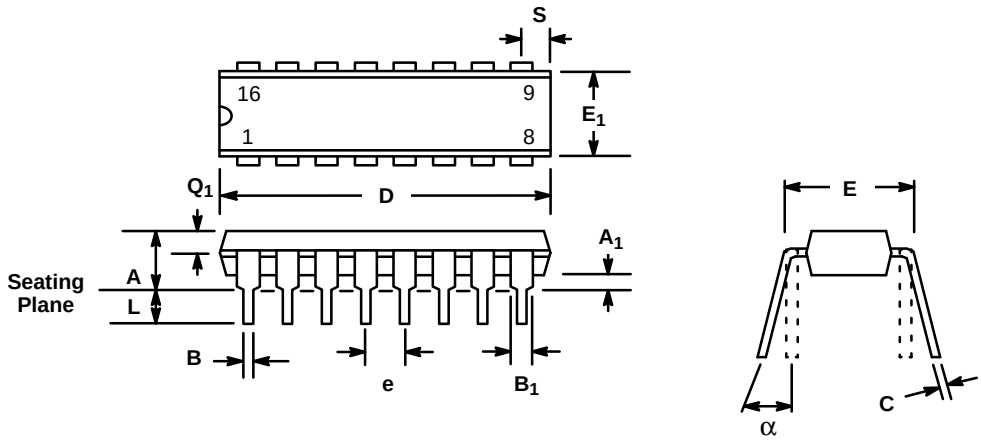


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

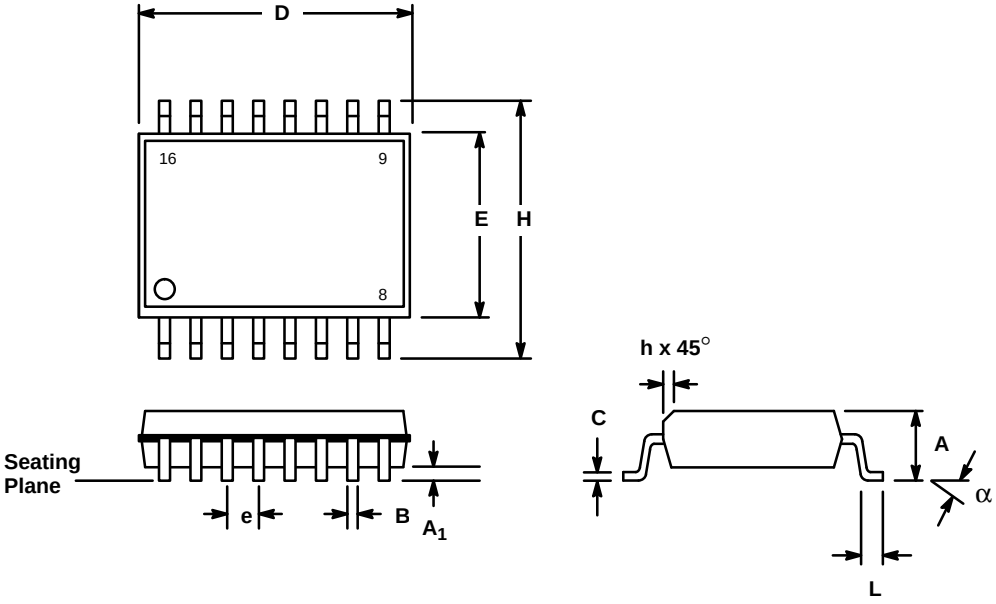
16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.745	0.785	18.92	19.94
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.080	0.51	2.03

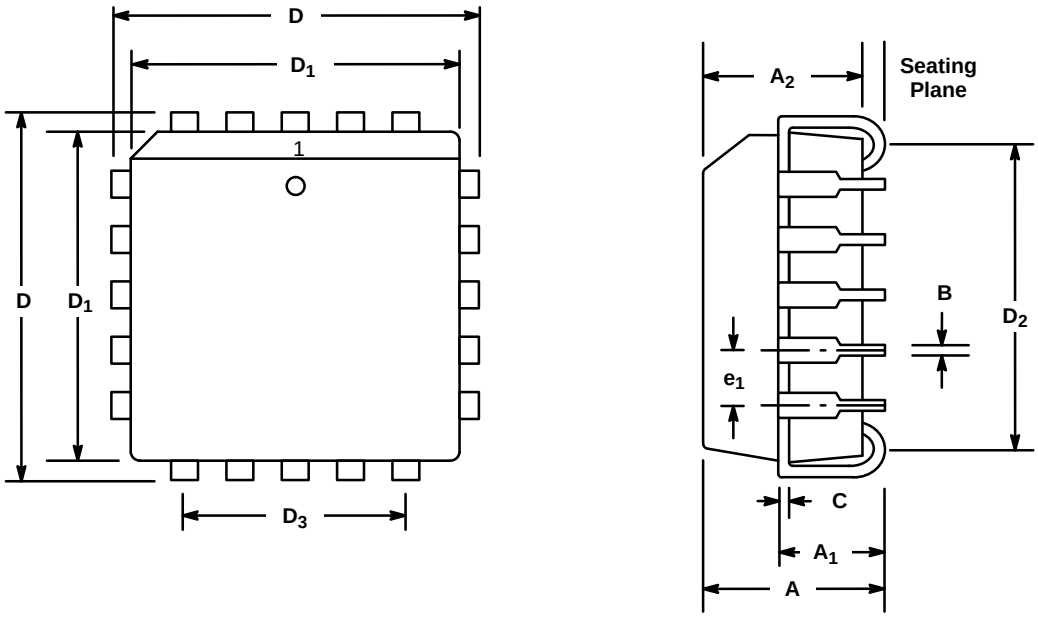
Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.46	2.64
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.482
C	0.0091	0.0125	0.231	0.318
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

Notes

Notes

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