

**Power Products Division**  
**HIGH AND LOW SIDE DRIVER**

The MPIC2112 is a high voltage, high speed, power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

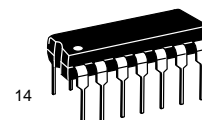
- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- Separate Logic Supply
- Operating Supply Range from 5 to 20 V
- Logic and Power Ground Operating Offset Range from -5 to +5 V
- CMOS Schmitt-triggered Inputs with Pull-down
- Cycle by Cycle Edge-triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs in Phase with Inputs

**PRODUCT SUMMARY**

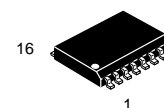
<b>V<sub>OFFSET</sub></b>	<b>600 V MAX</b>
<b>I<sub>O+/-</sub></b>	<b>200 mA/400 mA</b>
<b>V<sub>OUT</sub></b>	<b>10 – 20 V</b>
<b>t<sub>on/off</sub> (typical)</b>	<b>125 &amp; 105 ns</b>
<b>Delay Matching</b>	<b>30 ns</b>

**MPIC2112**

**HIGH AND LOW  
SIDE DRIVER**



1  
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



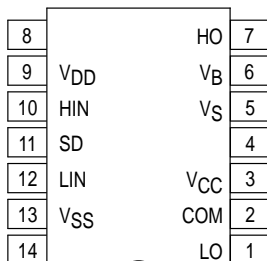
16  
**DW SUFFIX**  
PLASTIC PACKAGE  
CASE 751G-02  
SOIC – WIDE

**ORDERING INFORMATION**

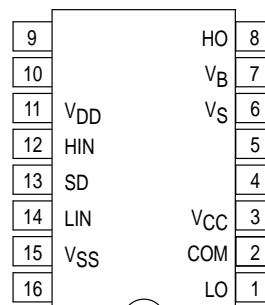
Device	Package
MPIC2112DW	SOIC WIDE
MPIC2112P	PDIP

**PIN CONNECTIONS**

(TOP VIEW)

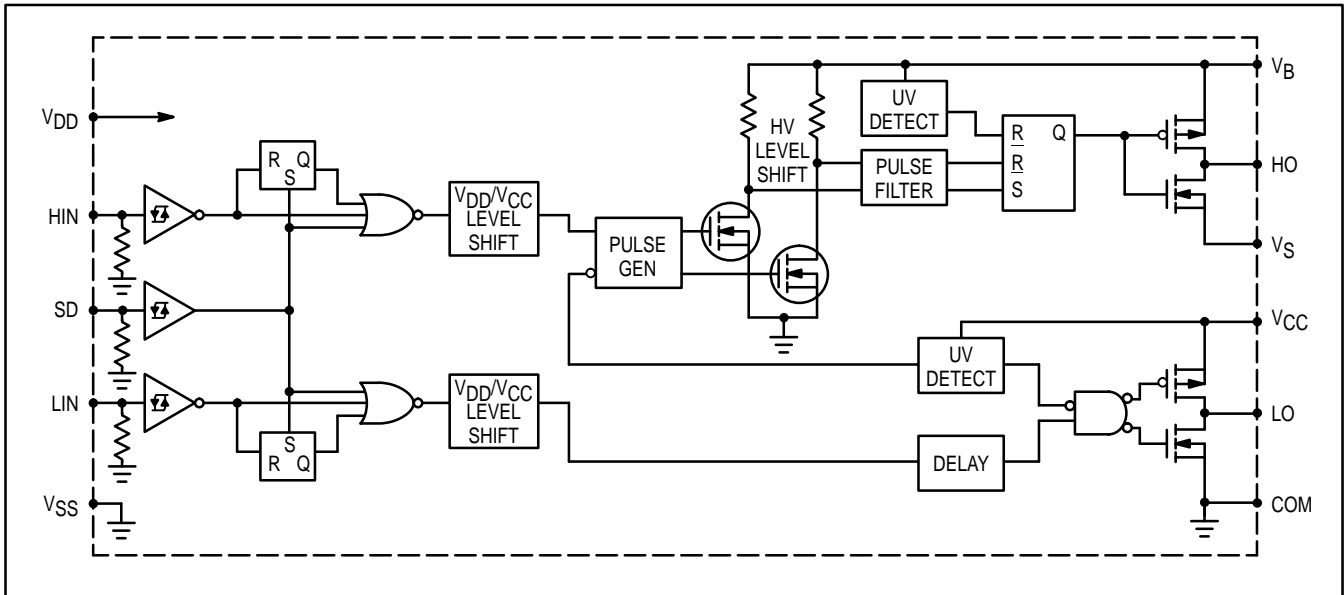


14 LEADS PDIP MPIC2112P



16 LEADS SOIC (WIDE BODY)  
MPIC2112DW

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Absolute Voltage	$V_B$	-0.3	625	$V_{DC}$
High Side Floating Supply Offset Voltage	$V_S$	$V_B-25$	$V_B+0.3$	
High Side Floating Output Voltage	$V_{HO}$	$V_S-0.3$	$V_B+0.3$	
Low Side Fixed Supply Voltage	$V_{CC}$	-0.3	25	
Low Side Output Voltage	$V_{LO}$	-0.3	$V_{CC}+0.3$	
Logic Supply Voltage	$V_{DD}$	-0.3	$V_{SS}+25$	
Logic Supply Offset Voltage	$V_{SS}$	$V_{CC}-25$	$V_{CC}+0.3$	
Logic Input Voltage (HIN, LIN & SD)	$V_{IN}$	$V_{SS}-0.3$	$V_{DD}+0.3$	
Allowable Offset Supply Voltage Transient	$dV_S/dt$	-	50	V/ns
*Package Power Dissipation @ $T_A \leq +25^\circ C$	$P_D$	-	1.6	Watt
	-	-	1.25	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	-	75	$^\circ C/W$
		-	100	
Operating and Storage Temperature	$T_j, T_{stg}$	-55	150	$^\circ C$
Lead Temperature for Soldering Purposes, 10 seconds	$T_L$	-	260	$^\circ C$

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset ratings are tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	$V_B$	$V_S+10$	$V_S+20$	V
High Side Floating Supply Offset Voltage	$V_S$	Note 1	600	
High Side Floating Output Voltage	$V_{HO}$	$V_S$	$V_B$	
Low Side Fixed Supply Voltage	$V_{CC}$	10	20	
Low Side Output Voltage	$V_{LO}$	0	$V_{CC}$	
Logic Supply Voltage	$V_{DD}$	$V_{SS}+5$	$V_{SS}+20$	
Logic Supply Offset Voltage	$V_{SS}$	-5	5	
Logic Input Voltage (HIN, LIN & SD)	$V_{IN}$	$V_{SS}$	$V_{DD}$	
Ambient Temperature	$T_A$	-40	125	$^\circ C$

Note 1: Logic operational for  $V_S$  of -5 to +600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$ .

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise specified)

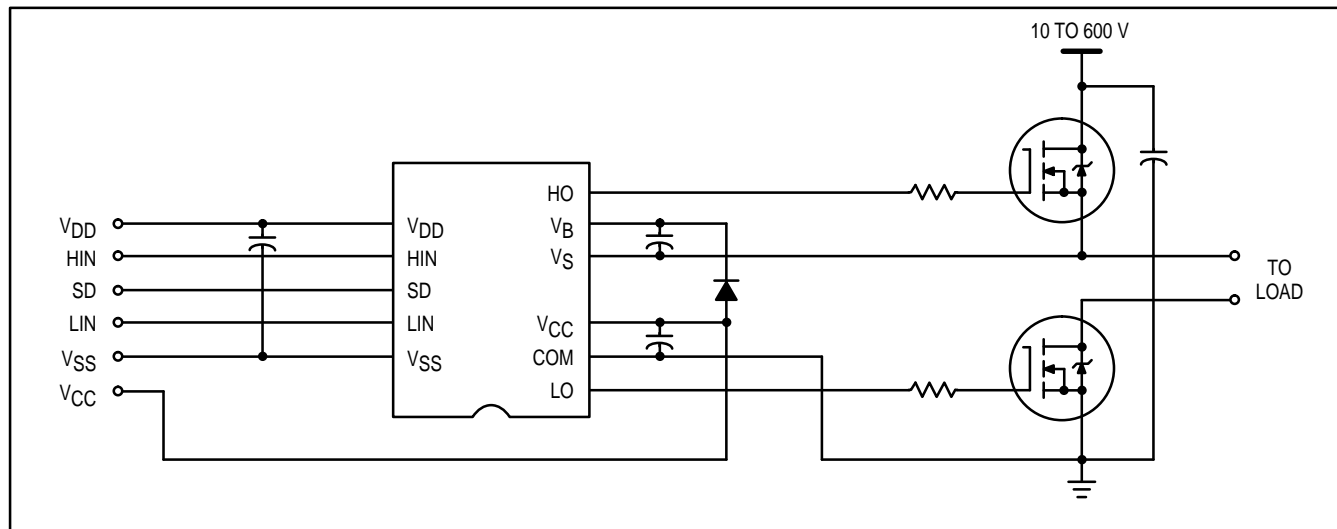
Characteristic	Symbol	Min	Typ	Max	Unit
<b>STATIC ELECTRICAL CHARACTERISTICS – SUPPLY CHARACTERISTICS</b>					
V <sub>BIAS</sub> (V <sub>CC</sub> , V <sub>BS</sub> , V <sub>DD</sub> ) = 15 V and V <sub>SS</sub> = COM unless otherwise specified. The V <sub>IN</sub> , V <sub>TH</sub> and I <sub>IN</sub> parameters are referenced to V <sub>SS</sub> and are applicable to all three logic input leads: HIN, LIN and SD. The V <sub>O</sub> and I <sub>O</sub> parameters are referenced to COM or V <sub>SS</sub> and are applicable to the respective output leads: HO or LO.					
Logic "1" Input Voltage	V <sub>IH</sub>	9.5	–	–	V
Logic "0" Input Voltage	V <sub>IL</sub>	–	–	6.0	
High Level Output Voltage, V <sub>BIAS</sub> –V <sub>O</sub> @ V <sub>IN</sub> = V <sub>IH</sub> , I <sub>O</sub> = 0 A	V <sub>OH</sub>	–	–	100	mV
Low Level Output Voltage, V <sub>O</sub> @ V <sub>IN</sub> = V <sub>IL</sub> , I <sub>O</sub> = 0 A	V <sub>OL</sub>	–	–	100	
Offset Supply Leakage Current @ V <sub>B</sub> = V <sub>S</sub> = 600 V	I <sub>LK</sub>	–	–	50	μA
Quiescent V <sub>BS</sub> Supply Current @ V <sub>IN</sub> = 0 V or V <sub>DD</sub>	I <sub>QBS</sub>	–	25	60	
Quiescent V <sub>CC</sub> Supply Current @ V <sub>IN</sub> = 0 V or V <sub>DD</sub>	I <sub>QCC</sub>	–	80	180	
Quiescent V <sub>DD</sub> Supply Current @ V <sub>IN</sub> = 0 V or V <sub>DD</sub>	I <sub>QDD</sub>	–	2.0	5.0	
Logic "1" Input Bias Current @ V <sub>IN</sub> = 15 V	I <sub>IN+</sub>	–	20	40	
Logic "0" Input Bias Current @ V <sub>IN</sub> = 0 V	I <sub>IN–</sub>	–	–	1.0	
V <sub>BS</sub> Supply Undervoltage Positive Going Threshold	V <sub>B</sub> SUV+	7.4	–	9.6	V
V <sub>BS</sub> Supply Undervoltage Negative Going Threshold	V <sub>B</sub> SUV–	7.0	–	9.2	
V <sub>CC</sub> Supply Undervoltage Positive Going Threshold	V <sub>CC</sub> UV+	7.6	–	9.6	
V <sub>CC</sub> Supply Undervoltage Negative Going Threshold	V <sub>CC</sub> UV–	7.2	–	9.2	
Output High Short Circuit Pulsed Current @ V <sub>OUT</sub> = 0 V, V <sub>IN</sub> = 15 V, PW ≤ 10 μs	I <sub>O+</sub>	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V <sub>OUT</sub> = 15 V, V <sub>IN</sub> = 0 V, PW ≤ 10 μs	I <sub>O–</sub>	420	500	–	

**DYNAMIC ELECTRICAL CHARACTERISTICS**

V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>, V<sub>DD</sub>) = 15 V and V<sub>SS</sub> = COM unless otherwise specified. T<sub>A</sub> = 25°C.

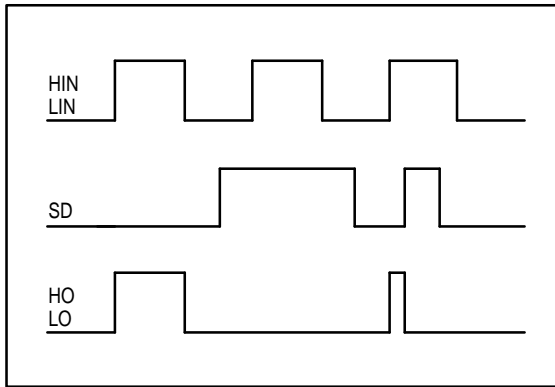
Turn-On Propagation Delay @ V <sub>S</sub> = 0 V	t <sub>on</sub>	–	125	180	ns
Turn-Off Propagation Delay @ V <sub>S</sub> = 600 V	t <sub>off</sub>	–	105	160	
Shutdown Propagation Delay @ V <sub>S</sub> = 600 V	t <sub>sd</sub>	–	105	160	
Turn-On Rise Time @ C <sub>L</sub> = 1000 pF	t <sub>r</sub>	–	80	130	
Turn-Off Fall Time @ C <sub>L</sub> = 1000 pF	t <sub>f</sub>	–	40	65	
Delay Matching, HS & LS Turn-On/Off	MT	–	–	30	

**TYPICAL CONNECTION**

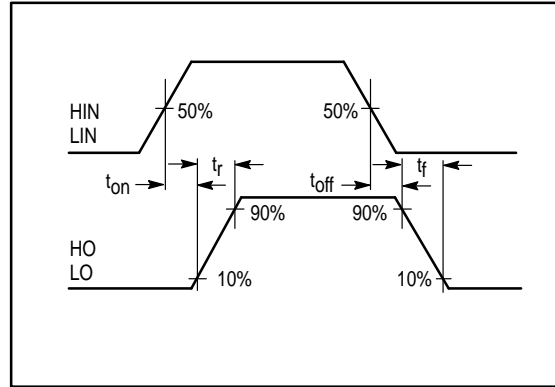


**LEAD DEFINITIONS**

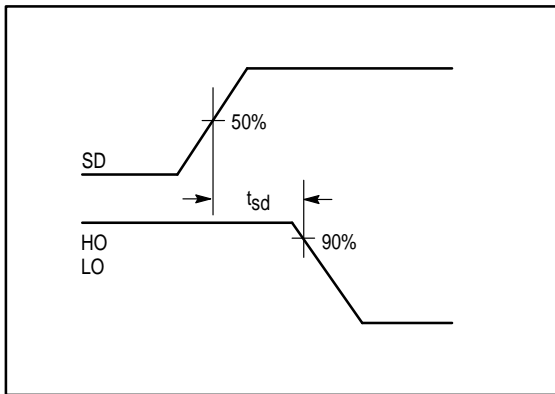
Symbol	Lead Description
V <sub>DD</sub>	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V <sub>SS</sub>	Logic Ground
V <sub>B</sub>	High Side Floating Supply
HO	High Side Gate Drive Output
V <sub>S</sub>	High Side Floating Supply Return
V <sub>CC</sub>	Low Side Supply
LO	Low Side Gate Drive Output
COM	Low Side Return



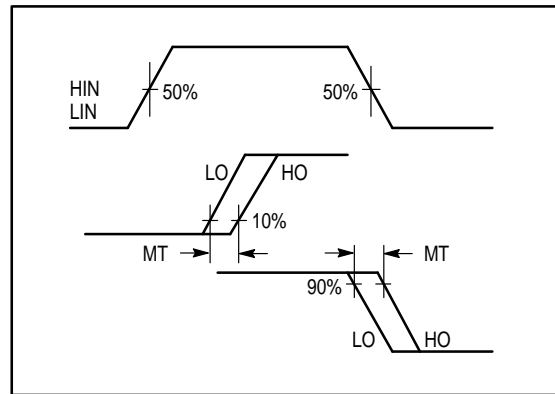
**Figure 1. Input / Output Timing Diagram**



**Figure 2. Switching Time Waveform Definitions**

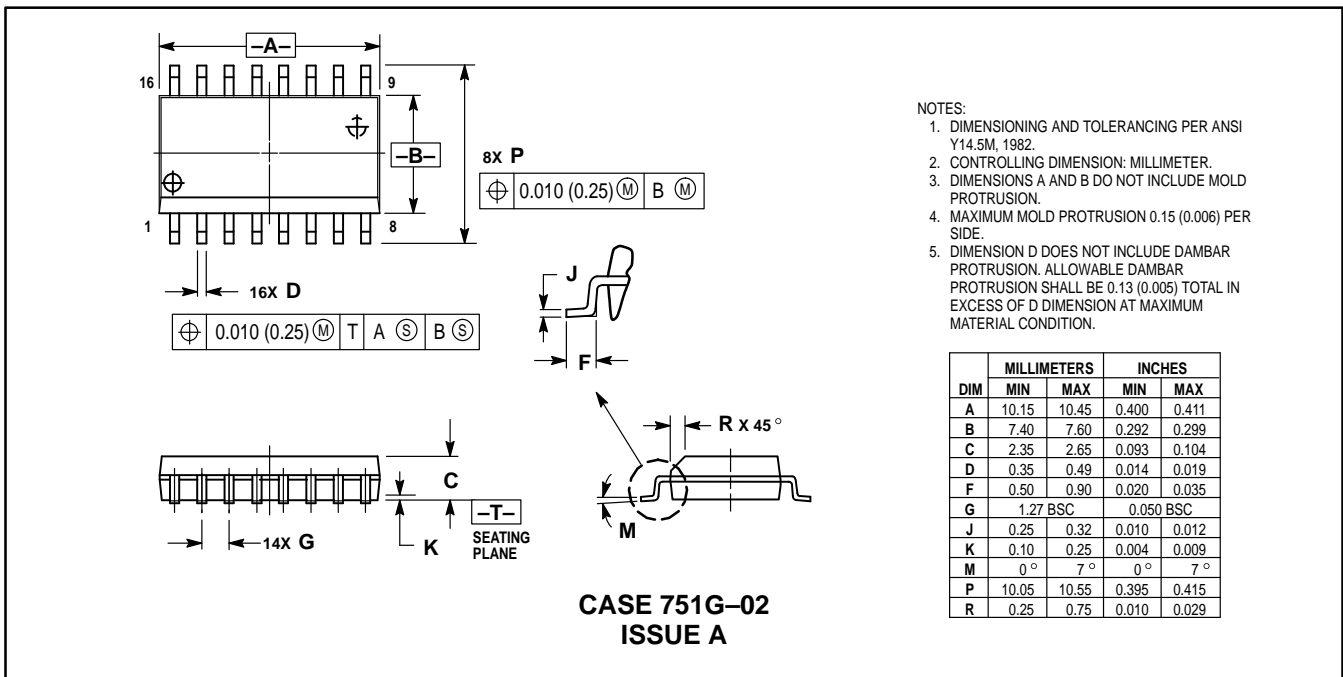
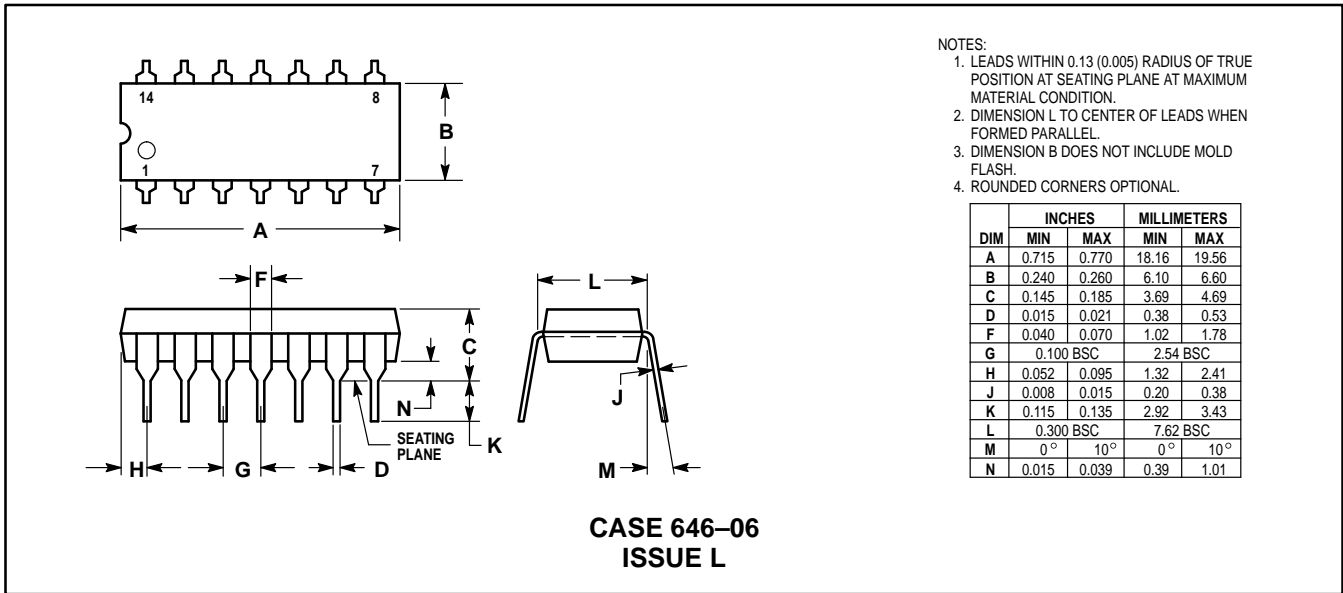



**Figure 3. Deadtime Waveform Definitions**



**Figure 4. Delay Matching Waveform Definitions**

PACKAGE DIMENSIONS



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