The MRFIC Line

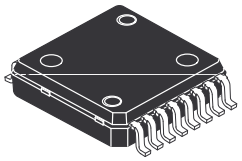
900 MHz GaAs Integrated Power Amplifier

MRFIC0913

900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.8 watts output power and 48% minimum power added efficiency under GSM signal conditions at 4.8 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal performance through a solderable backside contact.

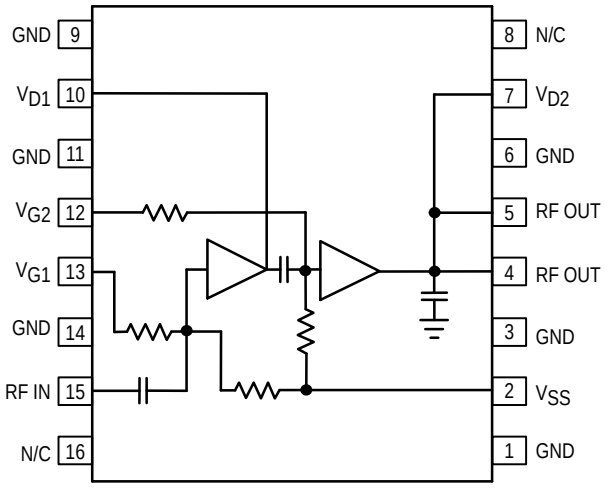
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power:
  36.0 dBm @ 5.8 Volts
  35.0 dBm @ 4.8 Volts
  31.5 dBm @ 3.6 Volts
- 48% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0913R2 for Tape and Reel Option.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0913



CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	9	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

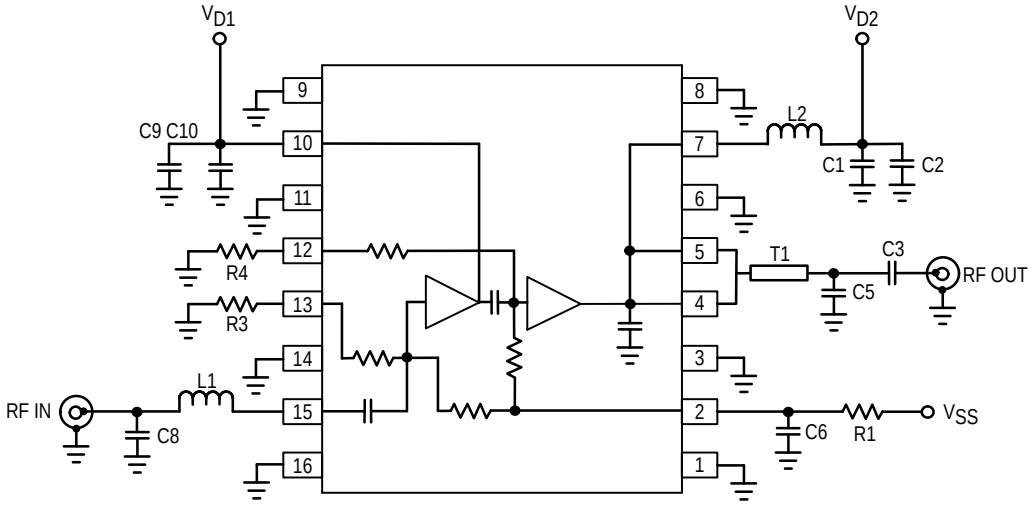
MOTOROLA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 7.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

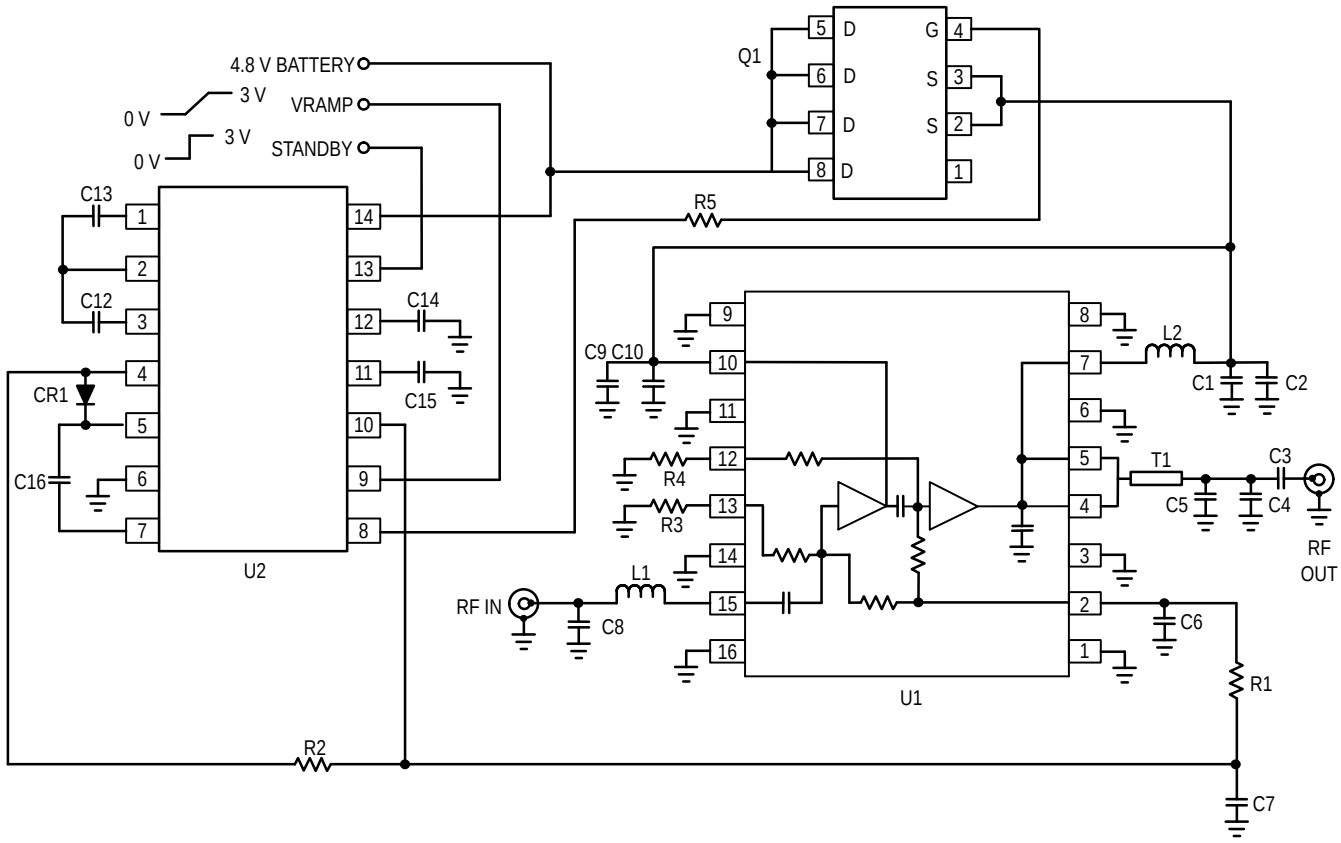
ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.8 V, V_{SS} = –4 V, P_{in} = 10 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34.5	35	—	dBm
Power Added Efficiency	48	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at Low voltage (V_{D1}, V_{D2} = 4.0 V)	33.3	33.5	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 6 V)	1	—	—	MHz
Negative Supply Current	—	—	1.25	mA



C1, C3, C10	47 pF, ATC	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C2, C9	47 nF, Vitramon	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C5	10 pF, ATC		Coilcraft 1606–10	T1	5 mm 30 Ω Microstrip Line
C6	22 nF, Vitramon	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45
C8	6.8 pF, ATC				

Figure 1. 900 MHz Reference Circuit



C1	33 pF, 0603 NPO/COG	CR1	MMBD701LT1	R2	100 Ω
C2, C9	33 nF	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C3	47 pF, 0603 NPO/COG	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C4, C5, C8	6.8 pF, 0603 NPO/COG		Coilcraft 1606–10 (for	R5	470 Ω
C6	33 nF		improved harmonic rejection	T1	5 mm 30 Ω Microstrip Line
C7	220 nF		only)	U1	MRFIC0913
C10	33 pF, 0603 NPO/COG	Q1	MMSF4N01HD	U2	MC33169 (–4 V Version)
C12 – C16	1 μF	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45

Note: Use of a Schottky diode such as MMBD701LT1 for CR1 is mandatory below 3.6 V.
A general purpose silicon diode can be used above 3.6 V.

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

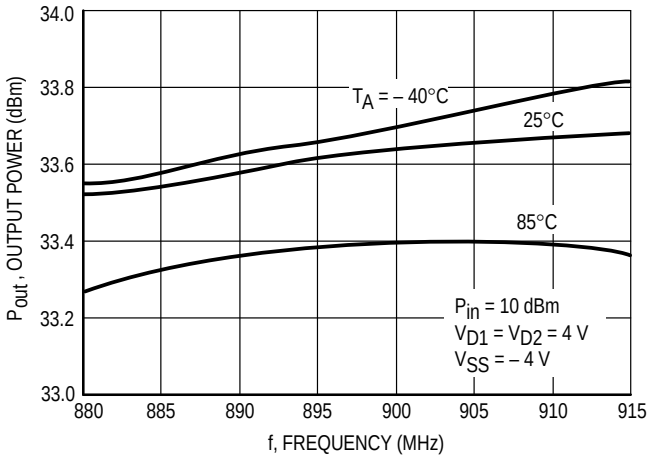


Figure 3. Output Power versus Frequency

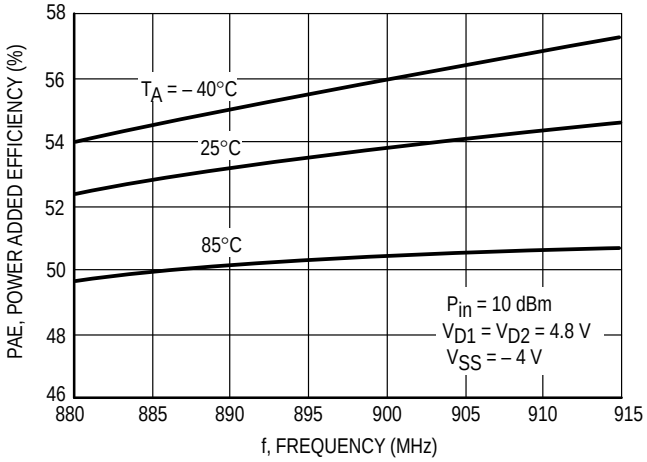


Figure 4. Power Added Efficiency versus Frequency

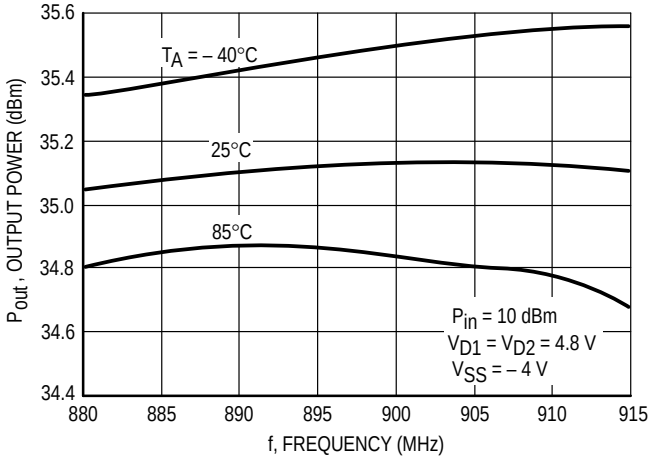


Figure 5. Output Power versus Frequency

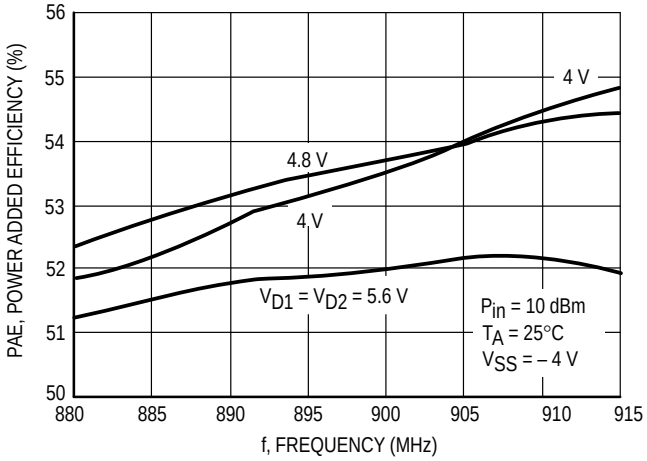


Figure 6. Power Added Efficiency versus Frequency

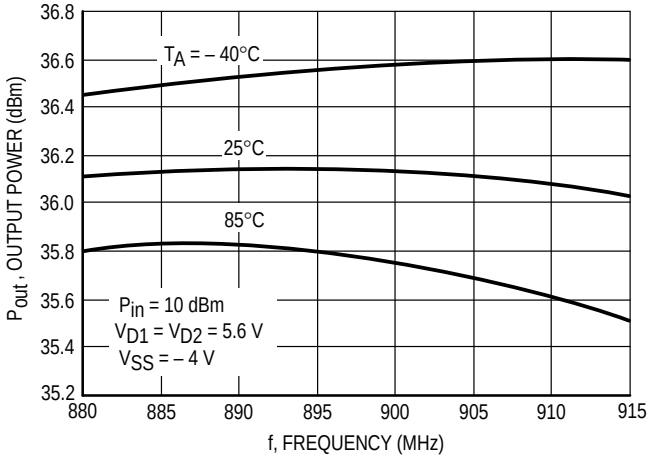


Figure 7. Output Power versus Frequency

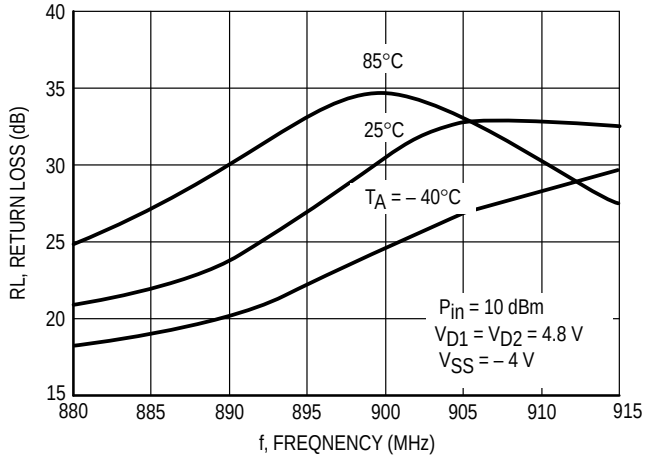


Figure 8. Input Return Loss versus Frequency

TYPICAL CHARACTERISTICS

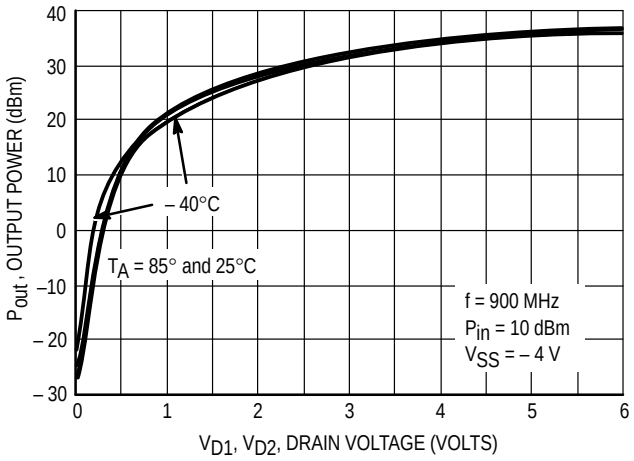


Figure 9. Output Power versus Drain Voltage

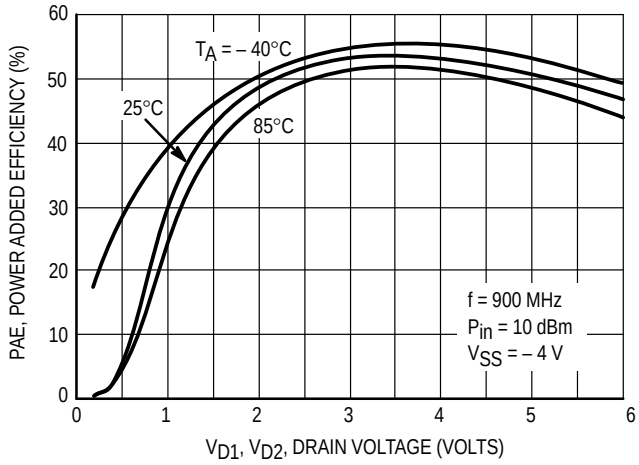


Figure 10. Power Added Efficiency versus Drain Voltage

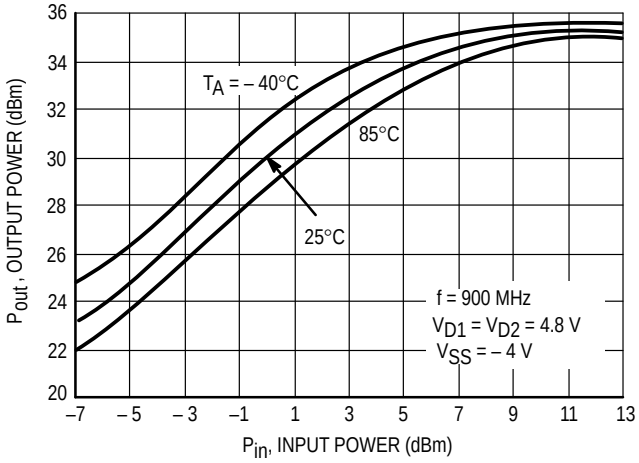


Figure 11. Output Power versus Input Power

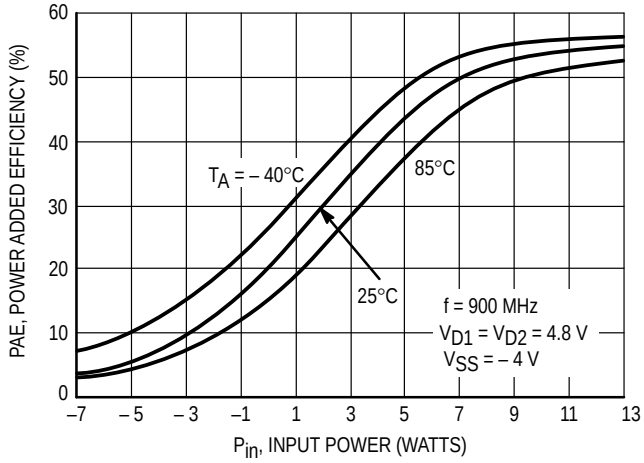


Figure 12. Power Added Efficiency versus Input Power

f	Z_{in} Ohms		Z_{OL}^* Ohms	
(MHz)	R	jX	R	jX
880	13.65	–44.05	3.15	5.06
885	13.64	–44.74	3.13	4.97
890	13.65	–45.44	3.10	4.89
895	13.64	–46.14	3.08	4.80
900	13.64	–46.84	3.06	4.71
905	13.65	–47.55	3.04	4.63
910	13.66	–48.27	3.02	4.54
915	13.66	–49.00	3.00	4.45

Table 1. Device Impedances Derived from Circuit Characterization

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0913 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 4.8 V operation. With matching circuit modifications, it is also applicable for use in GSM Class IV 6 V and Class V 3.6 V equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range. Typical performance at different battery voltages is:

- 36.0 dBm @ 5.8 V
- 35.0 dBm @ 4.8 V
- 31.5 dBm @ 3.6 V

This capability makes the MRFIC0913 suitable for portable cellular applications such as:

- 6 and 4.8 V GSM Class IV
- 3.6 V GSM Class V
- 3.6 V, 1.2 W Analog Cellular

RF Circuit Considerations

The MRFIC0913 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 3Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel, as shown in Figure 2, to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 80 to 160 mA for the first stage and 400 to 800 mA for the second stage.

For linear modes of operation which are required for PDC, DAMPS and CDMA, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.25 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 6 V linear operation are 100 mA ±5% for the first stage, and 500 mA ±5% for the second stage.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0913 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 300 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

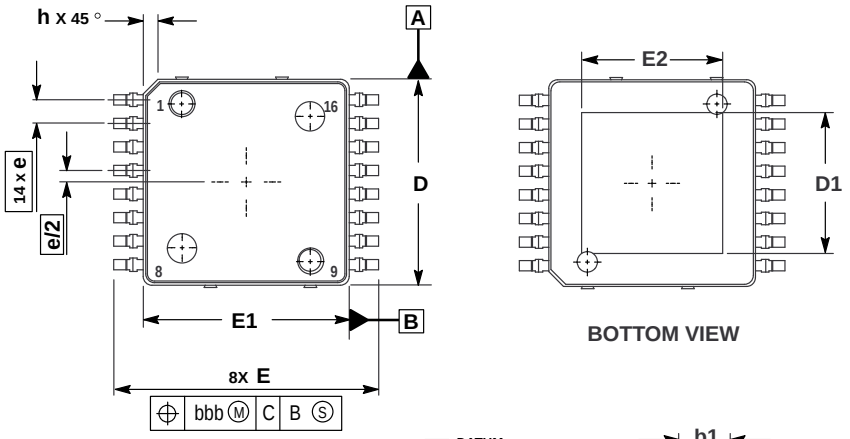
Conclusion

The MRFIC0913 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

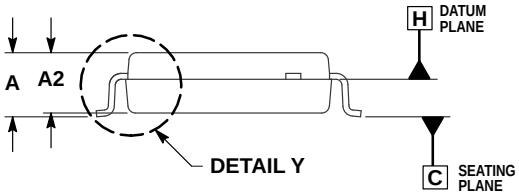
Evaluation Boards

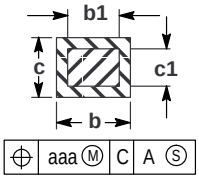
Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS

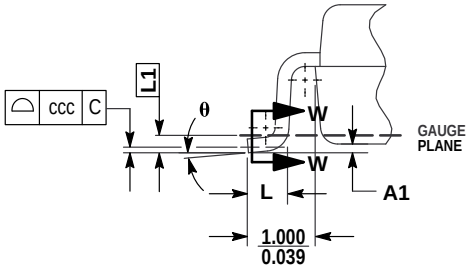


BOTTOM VIEW





SECT W–W



DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.350
A1	0.025	0.152
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	—	0.600
θ	0 °	7 °
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–02
ISSUE A

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