The MRFIC Line

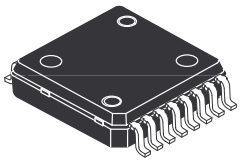
900 MHz GaAs Integrated Power Amplifier

MRFIC0917

900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.5 Watts output power and 43% minimum power added efficiency under GSM signal conditions at 3.6 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Pack package which gives excellent thermal performance through a solderable backside contact.

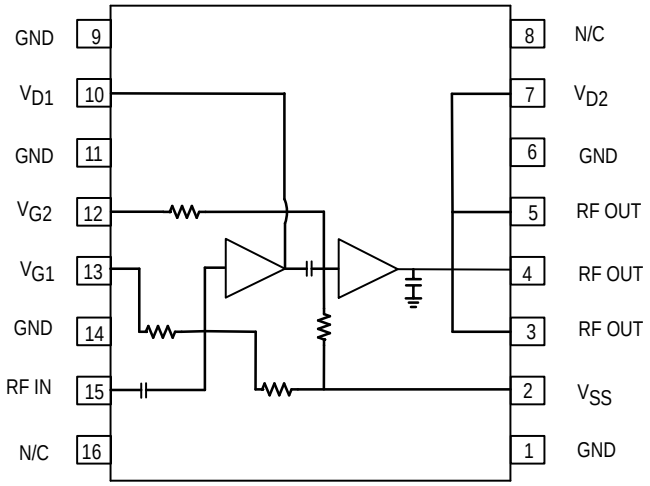
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power: 34.5 dBm @ 3.6 Volts
- 43% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0917R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0917



CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage, Normal Conditions	V_{D1}, V_{D2}	6	Vdc
Supply Voltage under Load Stress	V_{D1}, V_{D2}	4.5	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	15	°C/W



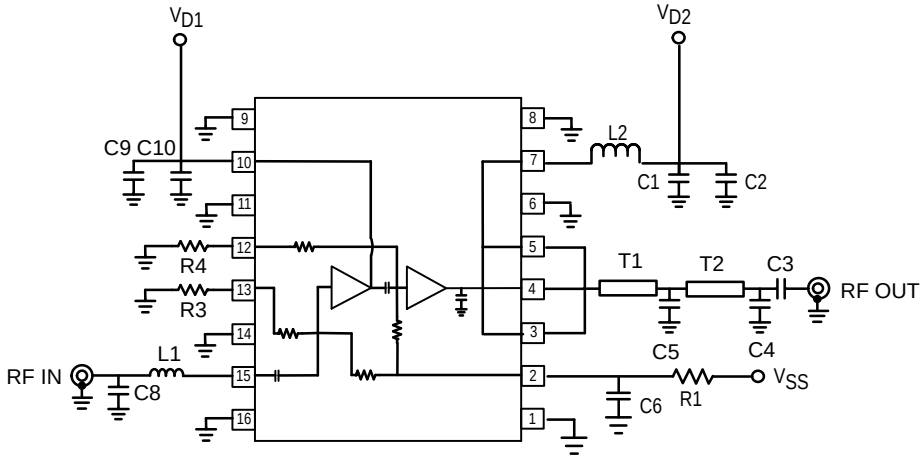
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 5.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

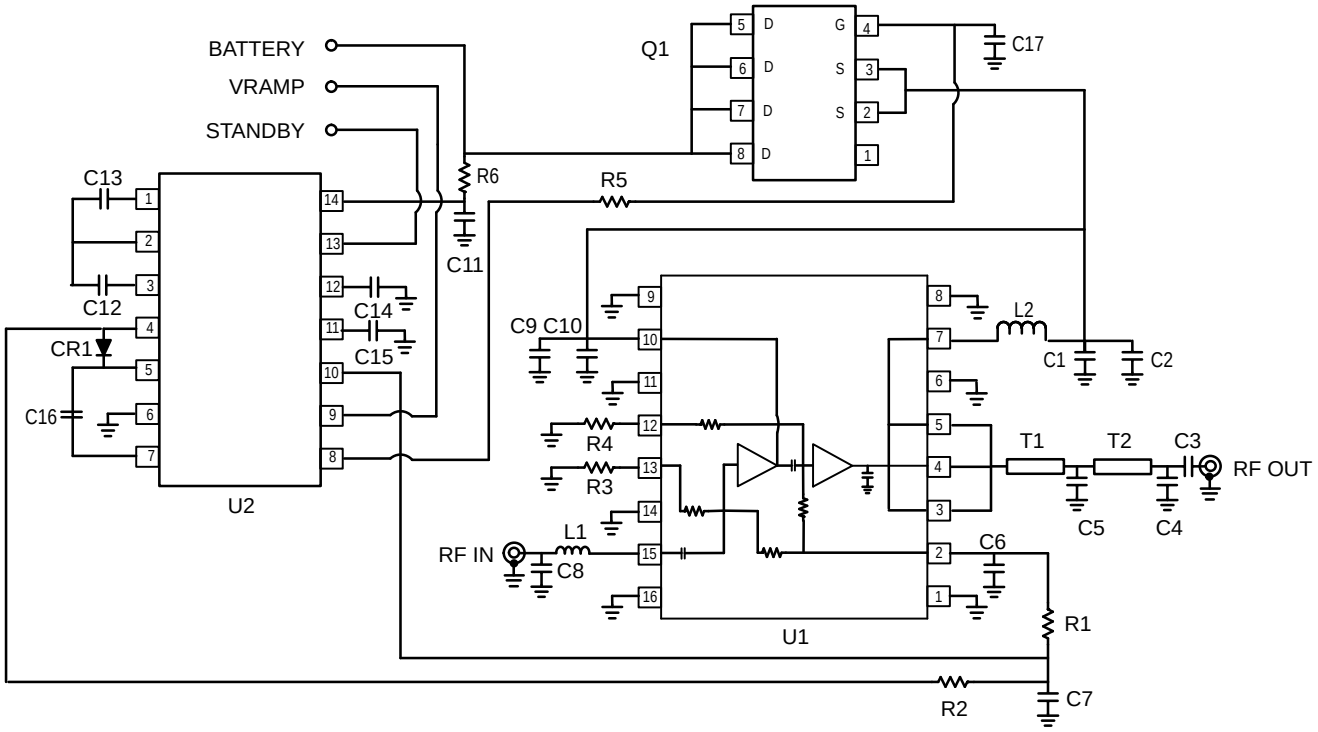
ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 3.6 V, V_{SS} = –4 V, P_{in} = 12 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Circuit Configuration Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34	34.5	—	dBm
Power Added Efficiency	43	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at low voltage (V_{D1}, V_{D2} = 3.0 V)	32.5	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch Stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 4.5 V)	1	—	—	MHz
Negative Supply Current	—	—	1	mA



C1, C3, C10	33 pF	C8	6.8 pF	R1, R3	330 Ω
C2, C6, C9	33 nF	L1	5.6 nH	R4	1 kΩ
C4	4.7 pF	L2	10 Turn MicroSpring,	T1	2 mm 30 Ω MICROSTRIP
C5	10 pF		Coilcraft 1606–10 or	T2	3.5 mm 30 Ω MICROSTRIP
			18 mm 50 Ω MICROSTRIP	BOARD MATERIAL	FR4

Figure 1. 900 MHz Reference Circuit



C1, C3, C10	33 pF	CR1	MMBD701LT1	R4	1 kΩ
C2, C6, C9	33 nF	L1	5.6 nH	R5	470 Ω
C4	4.7 pF	L2	10 Turn MicroSpring,	R6	22 Ω
C5	10 pF		Coilcraft 1606–10 or 18 mm	T1	2 mm 30 Ω MICROSTRIP
C7	220 nF		50 Ω MICROSTRIP	T2	3.5 mm 30 Ω MICROSTRIP
C8	6.8 pF	Q1	MMSF4N01HD	U1	MRFIC0917
C11 to C16	1 μF	R1, R3	330 Ω	U2	MC33169 (–4 V Version)
C17	0 to 5 nF Depending on control bandwidth	R2	100 Ω	BOARD MATERIAL	FR4

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

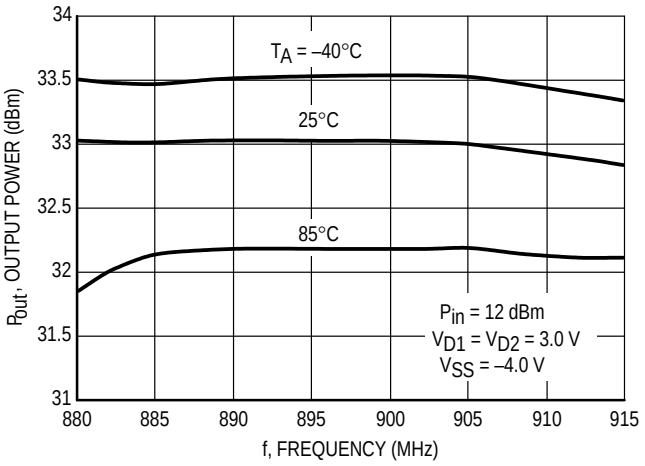


Figure 3. Output Power versus Frequency

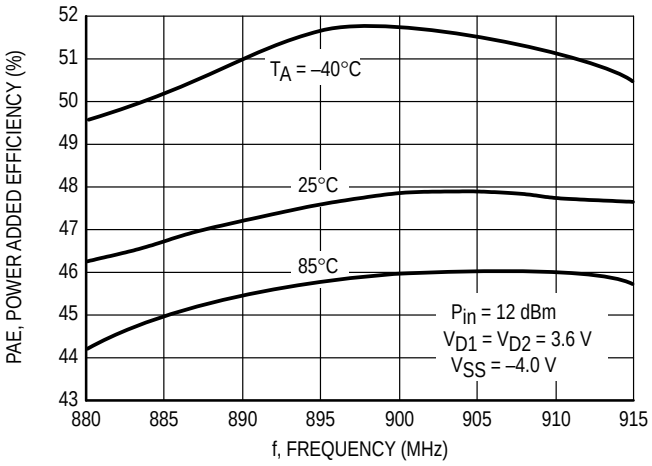


Figure 4. Power Added Efficiency versus Frequency

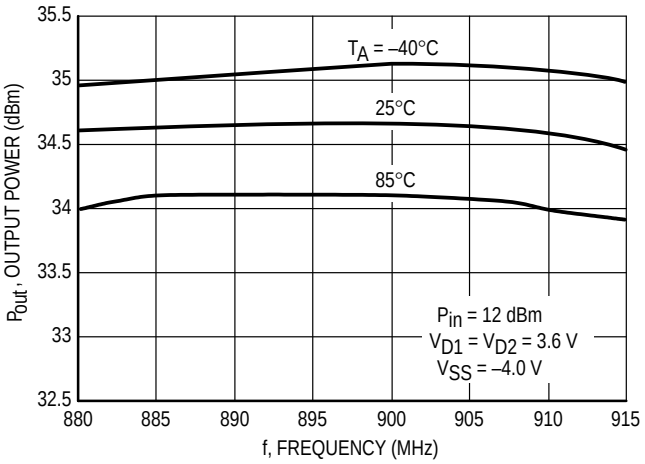


Figure 5. Output Power versus Frequency

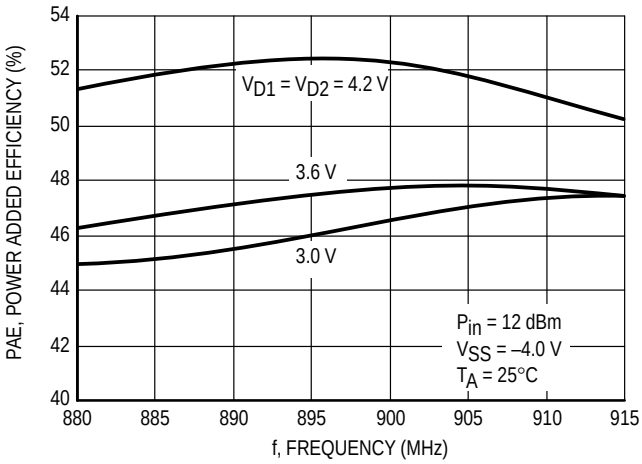


Figure 6. Power Added Efficiency versus Frequency

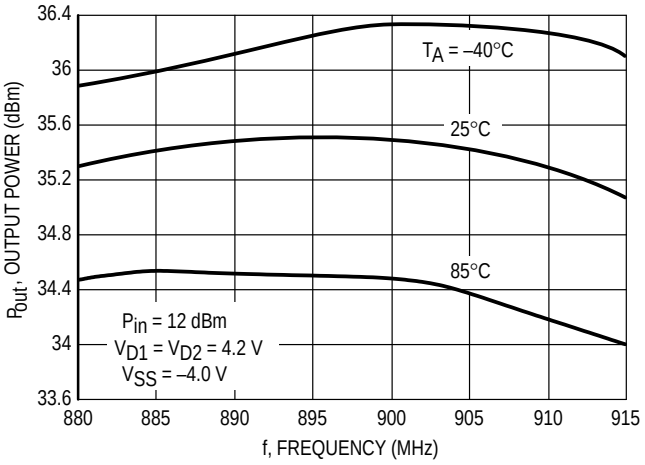


Figure 7. Output Power versus Frequency

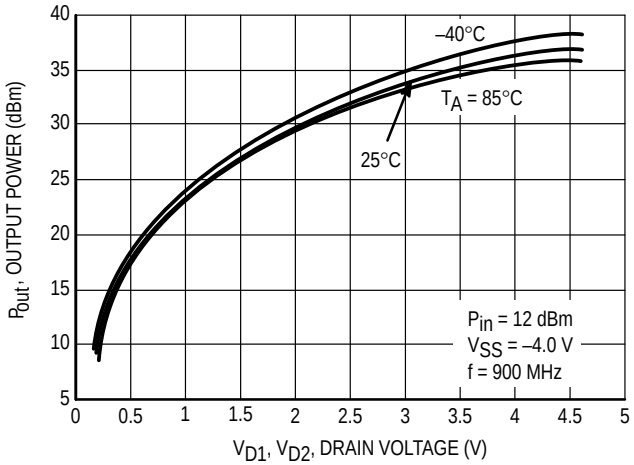


Figure 8. Output Power versus Drain Voltage

TYPICAL CHARACTERISTICS

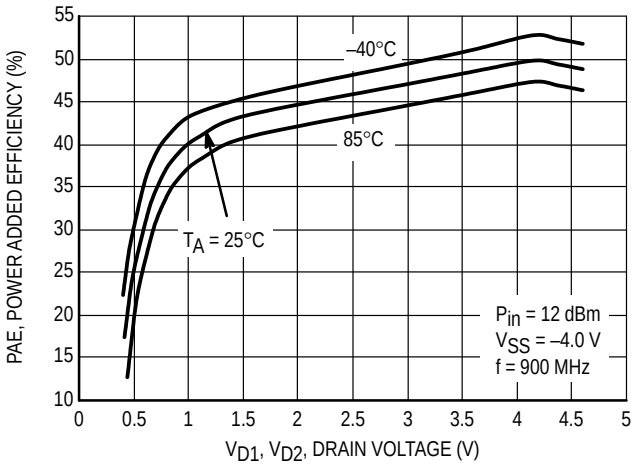


Figure 9. Power Added Efficiency versus Drain Voltage

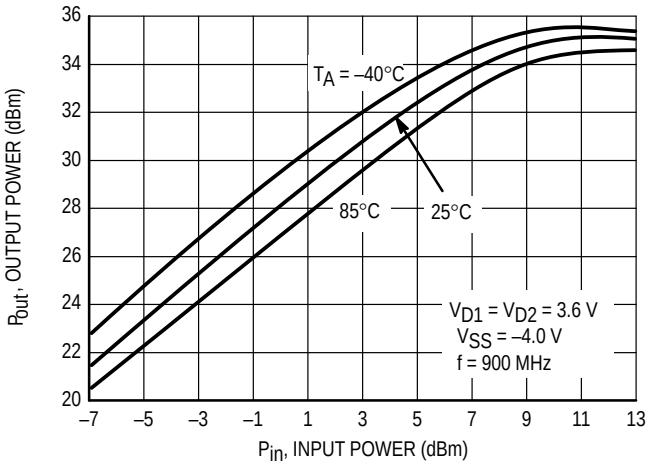


Figure 10. Output Power versus Input Power

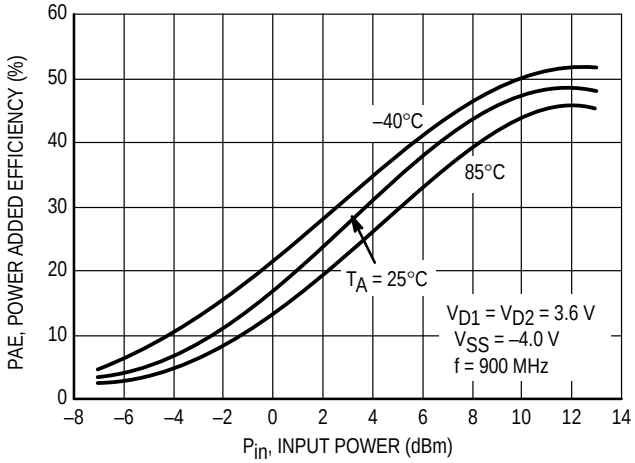


Figure 11. Power Added Efficiency versus Input Power

f	Z_{in} (Ω)		Z_{OL}^* (Ω)	
MHz	R	jX	R	jX
880	20.2	8.63	2.49	7.04
885	20.5	8.57	2.48	6.98
890	20.8	8.5	2.45	6.91
895	21.2	8.42	2.43	6.81
900	21.5	8.36	2.42	6.74
905	21.9	8.3	2.4	6.64
910	22.3	8.23	2.37	6.58
915	22.6	8.17	2.36	6.51

Table 1. Device Impedances Derived from Circuit Characterization

Table 2. Scattering Parameters

(V_{DD} = 3 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
500	0.738	–86	12.71	–82	0.002	147	0.891	173
600	0.786	–83	5.05	–102	0.003	132	0.874	170
700	0.799	–113	11.56	–79	0.004	153	0.858	173
800	0.681	–115	8.44	–113	0.005	138	0.885	171
820	0.671	–116	7.93	–115	0.005	138	0.887	170
840	0.669	–117	7.54	–117	0.005	133	0.885	170
860	0.668	–118	7.30	–119	0.005	130	0.888	170
880	0.673	–119	7.18	–121	0.006	129	0.885	169
900	0.672	–120	7.07	–123	0.006	131	0.883	169
920	0.672	–122	6.90	–127	0.006	130	0.883	168
940	0.672	–123	6.65	–130	0.006	130	0.882	168
960	0.673	–124	6.37	–133	0.007	127	0.881	168
980	0.682	–126	6.10	–136	0.007	130	0.88	168
1000	0.679	–127	5.83	–138	0.006	123	0.881	167
1100	0.685	–134	4.81	–145	0.007	120	0.874	166
1200	0.705	–143	4.67	–152	0.008	121	0.868	165
1300	0.703	–152	4.06	–165	0.010	113	0.855	164
1400	0.704	–161	3.69	–175	0.011	106	0.838	163
1500	0.646	–174	3.19	160	0.011	86	0.826	166

Table 3. Scattering Parameters

(V_{DD} = 3.6 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
500	0.737	–85	14.12	–84	0.002	135	0.887	174
600	0.792	–83	5.47	–103	0.002	130	0.866	170
700	0.799	–112	12.69	–80	0.004	157	0.853	174
800	0.687	–115	9.13	–115	0.005	131	0.881	171
820	0.681	–116	8.56	–117	0.005	131	0.882	171
840	0.680	–117	8.12	–119	0.005	132	0.882	170
860	0.678	–118	7.83	–121	0.005	131	0.883	170
880	0.680	–119	7.69	–123	0.005	129	0.882	170
900	0.681	–120	7.53	–125	0.006	133	0.882	169
920	0.680	–122	7.36	–129	0.006	127	0.879	169
940	0.681	–123	7.09	–132	0.006	130	0.878	169
960	0.681	–125	6.77	–135	0.006	121	0.878	168
980	0.688	–126	6.47	–137	0.006	123	0.878	168
1000	0.684	–128	6.18	–139	0.006	123	0.876	168
1100	0.690	–135	5.08	–147	0.007	116	0.870	166
1200	0.707	–143	4.90	–153	0.007	123	0.862	165
1300	0.701	–153	4.24	–167	0.009	112	0.852	164
1400	0.704	–162	3.83	–176	0.010	107	0.833	164
1500	0.643	–174	3.26	160	0.010	84	0.828	167

Table 4. Scattering Parameters

(V_{DD} = 4.2 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
500	0.740	–85	15.59	–86	0.002	139	0.880	174
600	0.798	–84	5.71	–103	0.002	135	0.859	171
700	0.802	–112	13.82	–81	0.004	154	0.851	174
800	0.694	–116	9.82	–116	0.005	137	0.879	171
820	0.688	–116	9.20	–119	0.005	132	0.883	171
840	0.684	–117	8.70	–121	0.004	137	0.877	171
860	0.688	–119	8.37	–123	0.005	133	0.879	170
880	0.684	–120	8.20	–125	0.005	129	0.879	170
900	0.686	–121	8.03	–127	0.005	127	0.879	169
920	0.685	–123	7.82	–131	0.006	130	0.879	169
940	0.682	–124	7.53	–134	0.005	127	0.875	169
960	0.687	–126	7.18	–137	0.006	126	0.874	169
980	0.694	–127	6.84	–139	0.006	124	0.875	168
1000	0.686	–129	6.53	–141	0.006	123	0.873	168
1100	0.692	–137	5.34	–149	0.006	116	0.866	167
1200	0.704	–145	5.12	–155	0.007	122	0.861	165
1300	0.698	–154	4.41	–168	0.009	113	0.847	165
1400	0.695	–163	3.94	–178	0.010	104	0.835	164
1500	0.638	–175	3.34	159	0.009	84	0.828	167

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0917 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 3.6 V operation. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range.

This capability makes the MRFIC0917 suitable for portable cellular applications such as:

- 3.6 V 900 MHz DAMPS
- 3.6 V 900 MHz PDC

RF Circuit Considerations

The MRFIC0917 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a two–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 2Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0917 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 100 to 200 mA for the first stage and 600 to 1200 mA for the second stage.

For linear modes of operation, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.0 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 3.6 V linear operation are 150 mA ±5% for the first stage, and 750 mA ±5% for the second stage.

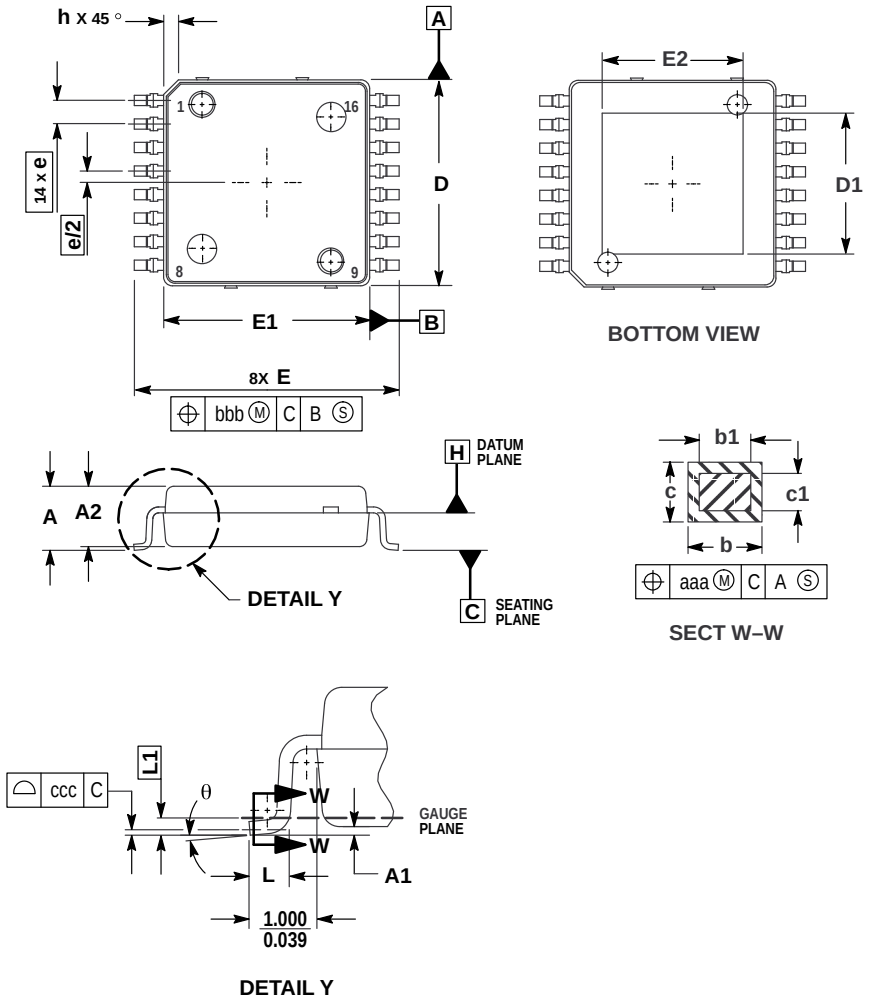
Conclusion

The MRFIC0917 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.350
A1	0.025	0.152
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	—	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–02
ISSUE A

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