

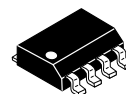
The MRFIC Line 900 MHz 2 Stage PA

The MRFIC2006 is an Integrated PA designed for linear operation in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2006 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

- 50 Ω Input and Output Impedance
- Typical Gain = 23 dB @ 900 MHz
- Bias Current Externally Adjustable
- Bias Pin can be used to Ramp or Disable
- Class A or AB Linear Operation
- Unconditionally Stable
- SO-8 Leaded Plastic Package
- Order MRFIC2006R2 for Tape and Reel.
R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2006

MRFIC2006

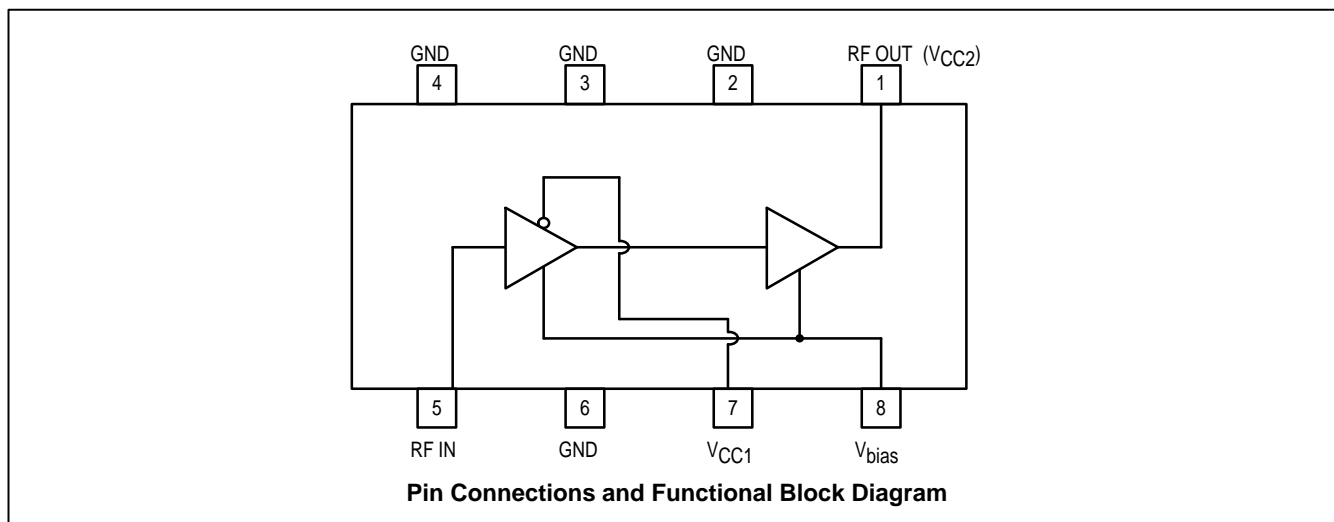
**900 MHz 2 STAGE PA
SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**CASE 751-05
(SO-8)**

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, $Z_0 = 50 \Omega$ unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1}, V_{CC2}	5.0	Vdc
Bias Voltage	V_{bias}	6.0	Vdc
Total Supply Current	I_{CC1}, I_{CC2}	100	mA
RF Output Power ($V_{CC2} < 4.0 \text{ V}$)	P_{out}	+21	dBm
RF Output Power ($4.0 \text{ V} < V_{CC2} \leq 5.0 \text{ V}$)	P_{out}	$53 - 8 V_{CC2}$	dBm
RF Input Power	P_{in}	+10	dBm
Operating Ambient Temperature	T_A	-35 to +85	$^\circ\text{C}$
Storage and Junction Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	63	$^\circ\text{C/W}$



RECOMMENDED OPERATING RANGES

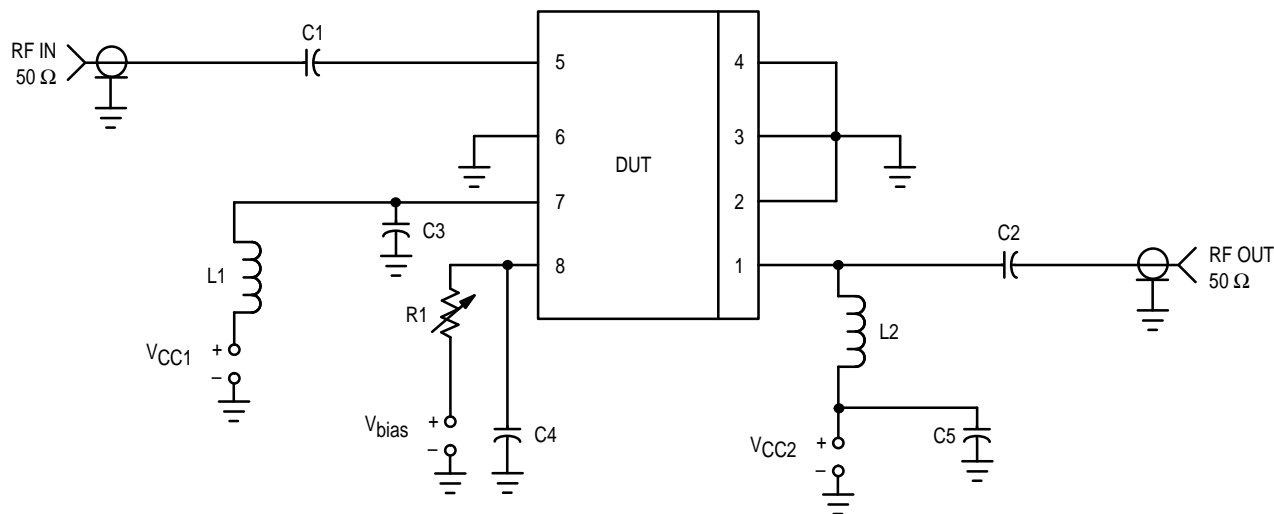
Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	1.8 to 4.0	Vdc
Bias Voltage Range	V_{bias}	0 to 5.0	Vdc
RF Frequency Range	f	500 to 1000	MHz

ELECTRICAL CHARACTERISTICS ($V_{CC1}, V_{CC2}, V_{bias} = 3.0\text{ V}, T_A = 25^\circ\text{C}, f = 900\text{ MHz}, Z_0 = 50\ \Omega$ unless otherwise noted)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current — Total	—	46	55	mA
I_{CC1}	—	14	—	mA
I_{CC2}	—	29	—	mA
I Bias	—	3.0	—	mA
Small Signal Gain	19	23	26	dB
Input Return Loss, RF IN Port	—	15	—	dB
Output Return Loss, RF OUT Port	—	15	—	dB
Reverse Isolation	—	35	—	dB
Output Power at 1.0 dB Gain Compression	+12	+15.5	—	dBm
3rd Order Intercept Point (Out)	—	+ 25	—	dBm
5th Order Intercept Point (Out)	—	+ 21	—	dBm

NOTE:

- All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C2 — 100 pF Chip Capacitor
 C3, C5 — 1.0 nF Chip Capacitor
 C4 — 10 nF Chip Capacitor
 L1 — 150 nH Chip Inductor
 L2 — 10 nH Chip Inductor

R1 — Resistor Optional
 RF Connectors — SMA Type
 Board Material — Epoxy/Glass $\epsilon_r = 4.5$,
 Dielectric Thickness = 0.014" (0.36 mm)

Figure 1. Typical Biasing Configuration

Table 1. Scattering Parameters for 900 MHz Two-Stage PA

(V_{CC1} , V_{CC2} , $V_{BIAS} = 3\text{ V}$, $I = 49\text{ mA}$, $T_A = 25^\circ\text{C}$, $50\ \Omega$ System)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.739	-16.67	3.785	51.56	0.003	-163.12	0.461	-89.23
100	0.702	-24.53	5.772	46.52	0.001	15.96	0.354	-117.30
150	0.671	-33.09	7.901	40.16	0.001	84.34	0.263	-144.77
200	0.649	-41.55	10.065	32.12	0.001	-165.89	0.208	-167.08
250	0.630	-49.79	12.287	23.06	0.002	-159.68	0.169	170.65
300	0.610	-58.60	14.576	12.25	0.002	171.75	0.136	145.40
350	0.592	-67.09	16.834	1.32	0.003	-160.23	0.113	113.52
400	0.567	-75.32	19.009	-10.72	0.005	-167.93	0.105	73.18
450	0.537	-83.69	20.901	-23.88	0.005	167.71	0.122	33.86
500	0.495	-91.79	22.237	-37.89	0.007	159.88	0.157	2.30
525	0.470	-95.35	22.626	-45.02	0.007	168.37	0.178	-10.93
550	0.448	-98.65	22.821	-52.22	0.010	162.65	0.196	-22.73
575	0.421	-101.69	22.834	-59.20	0.009	159.52	0.216	-32.62
600	0.397	-104.40	22.647	-66.13	0.010	155.15	0.233	-42.62
625	0.371	-106.50	22.299	-73.01	0.011	151.24	0.246	-50.98
650	0.349	-108.28	21.813	-79.43	0.011	148.14	0.258	-59.21
675	0.329	-109.85	21.204	-85.70	0.012	145.35	0.269	-66.61
700	0.310	-111.02	20.538	-91.62	0.012	140.66	0.273	-73.29
725	0.293	-111.65	19.824	-97.20	0.014	136.88	0.280	-79.97
750	0.278	-112.24	19.094	-102.54	0.014	136.98	0.281	-85.86
775	0.265	-112.60	18.334	-107.76	0.014	134.67	0.285	-91.50
800	0.252	-112.81	17.594	-112.54	0.016	133.71	0.284	-96.72
825	0.242	-113.50	16.880	-117.13	0.015	129.16	0.282	-102.24
850	0.233	-114.93	16.127	-122.44	0.017	131.80	0.281	-107.68
875	0.224	-115.32	15.438	-126.92	0.017	126.66	0.279	-112.88
900	0.216	-116.04	14.796	-130.89	0.017	127.06	0.275	-117.56
925	0.210	-116.66	14.165	-134.57	0.018	121.77	0.273	-120.85
950	0.203	-117.91	13.555	-138.19	0.019	122.40	0.269	-125.53
975	0.195	-118.87	13.009	-141.73	0.019	120.80	0.265	-129.73
1000	0.191	-120.47	12.515	-145.08	0.019	122.53	0.265	-132.68
1025	0.186	-122.39	12.004	-148.23	0.020	119.56	0.259	-137.22
1050	0.179	-124.03	11.517	-151.36	0.022	115.24	0.254	-140.85
1075	0.175	-126.22	11.063	-154.40	0.022	117.88	0.251	-144.69
1100	0.168	-128.77	10.634	-157.40	0.024	112.04	0.248	-148.25
1125	0.163	-131.41	10.228	-160.15	0.023	112.42	0.246	-151.75
1150	0.161	-133.93	9.841	-163.04	0.023	115.77	0.245	-155.28
1175	0.155	-136.68	9.479	-165.88	0.025	110.34	0.241	-158.69
1200	0.152	-140.85	9.125	-168.50	0.025	109.94	0.241	-161.95

TYPICAL CHARACTERISTICS

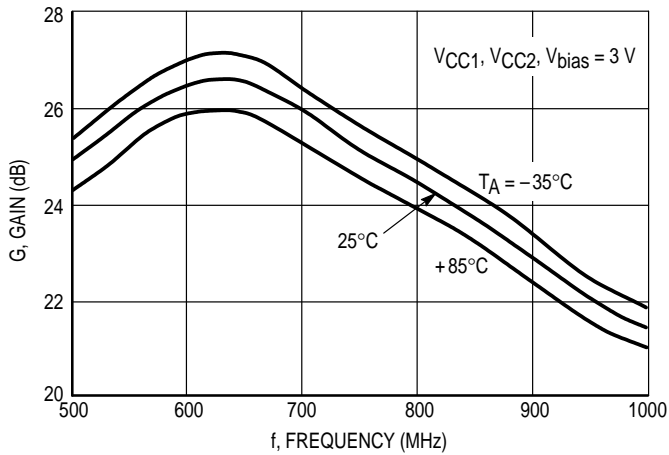


Figure 2. Gain versus Frequency

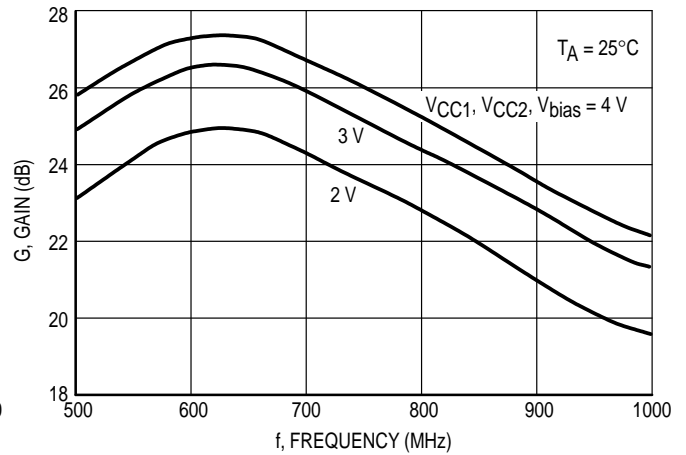


Figure 3. Gain versus Frequency

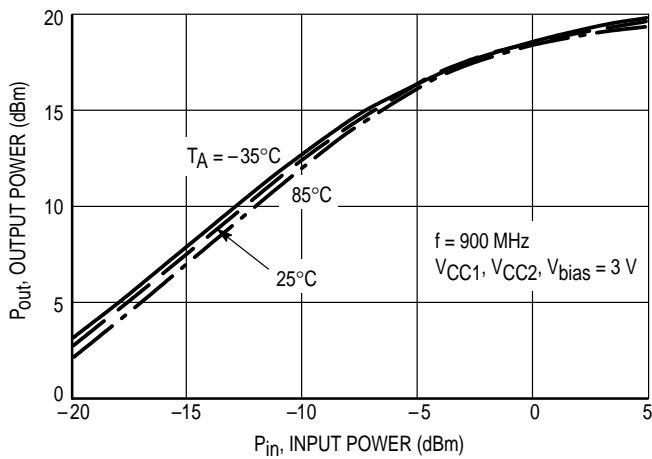


Figure 4. Output Power versus Input Power

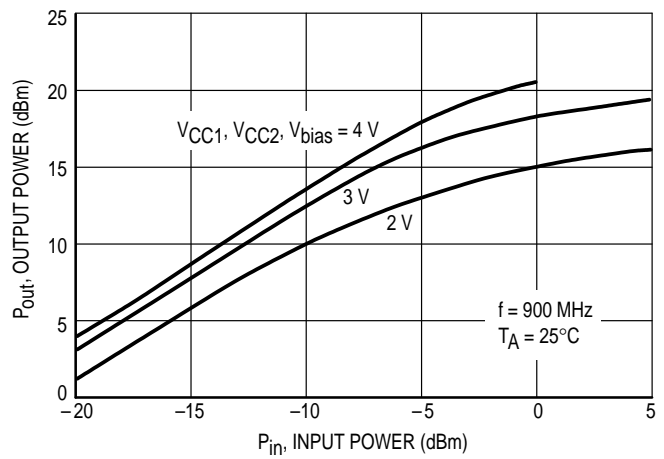


Figure 5. Output Power versus Input Power

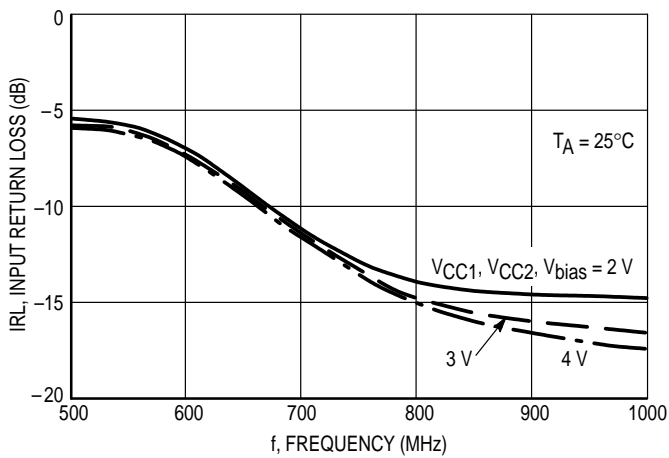


Figure 6. Input Return Loss versus Frequency

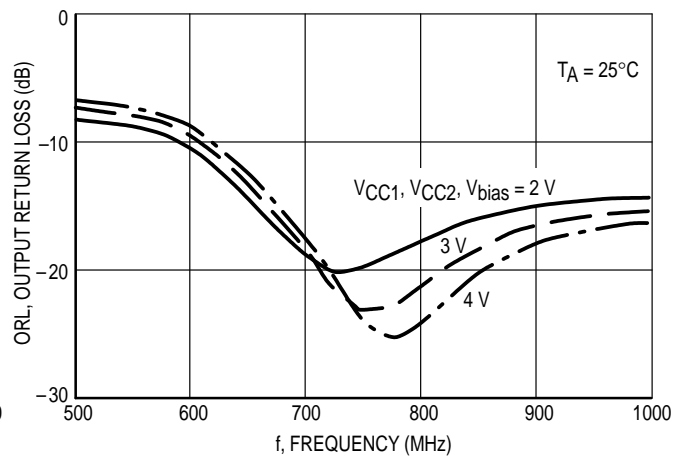


Figure 7. Output Return Loss versus Frequency

TYPICAL CHARACTERISTICS

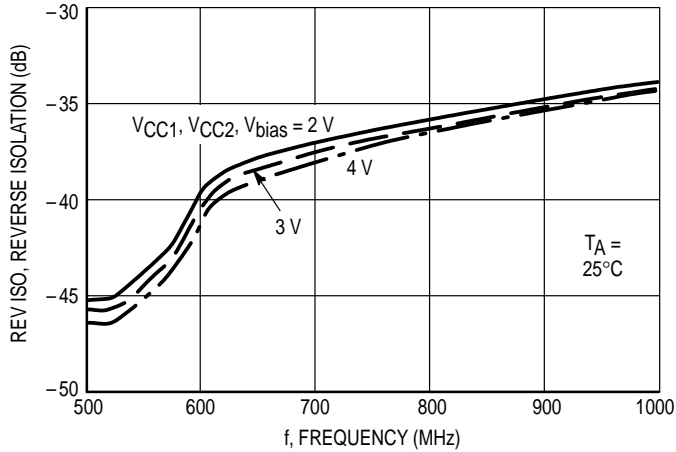


Figure 8. Reverse Isolation versus Frequency

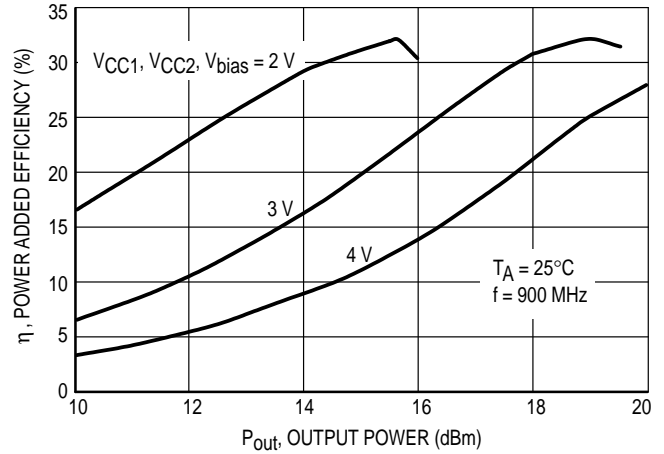


Figure 9. Power Added Efficiency versus Output Power

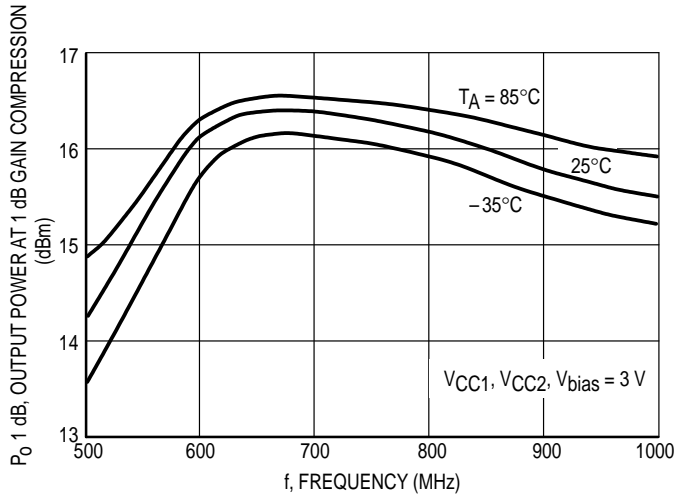


Figure 10. Output Power at 1 dB Gain Compression versus Frequency

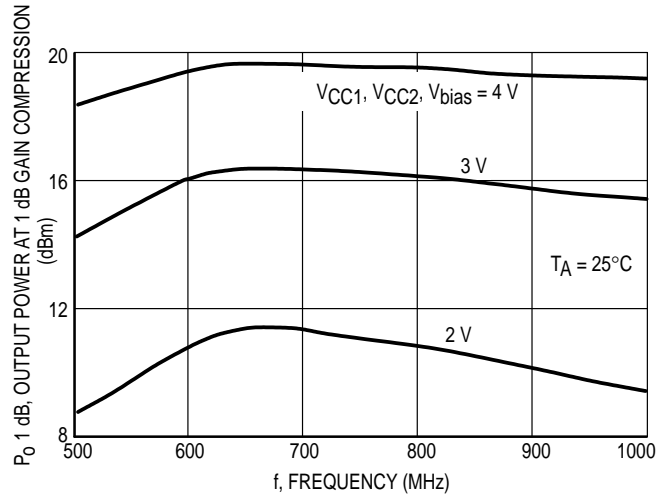


Figure 11. Output Power at 1 dB Gain Compression versus Frequency

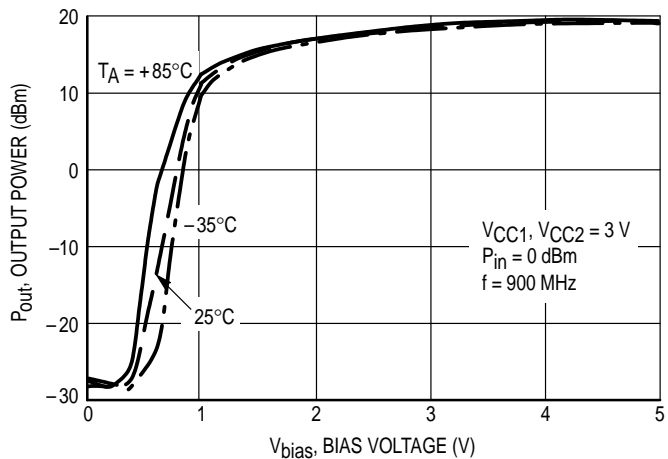


Figure 12. Output Power versus Bias Voltage

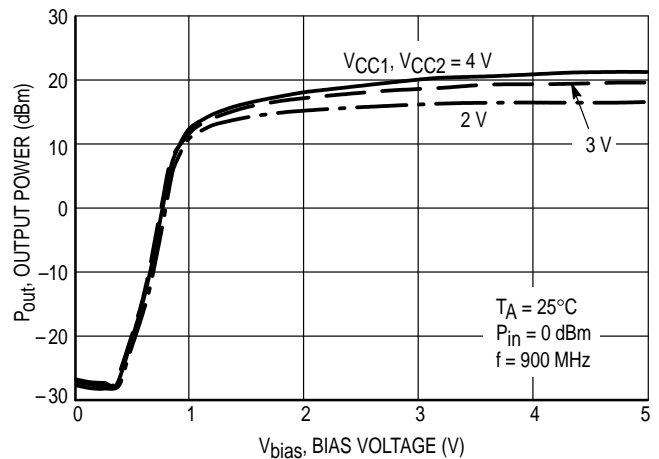


Figure 13. Output Power versus Bias Voltage

TYPICAL CHARACTERISTICS

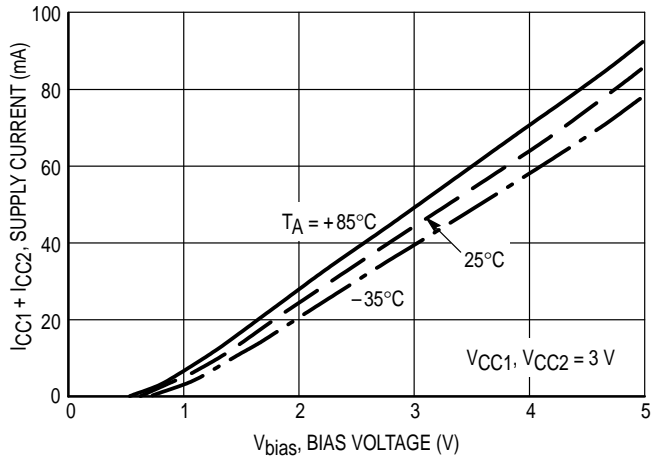


Figure 14. Supply Current versus Bias Voltage

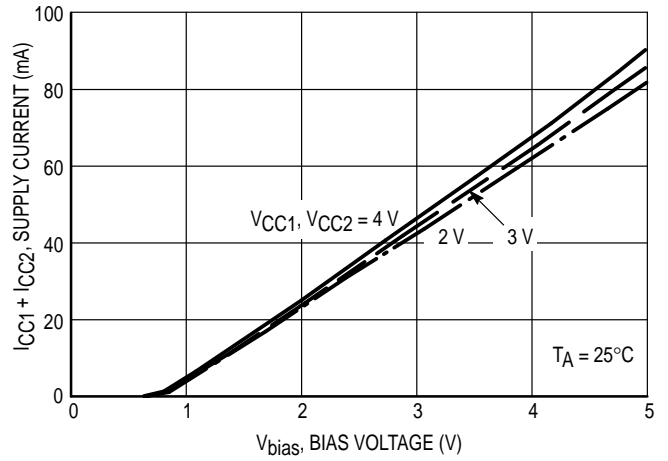


Figure 15. Supply Current versus Bias Voltage

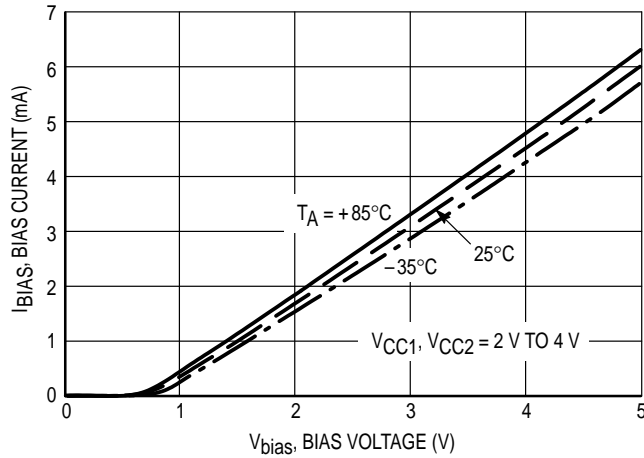


Figure 16. Bias Current versus Bias Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2006 was designed for low cost and flexibility. Low cost was achieved by minimizing external components and using an SOIC package. Flexibility was achieved by allowing the bias current to be externally adjustable resulting in a broad range of output power capability. The bias pin can be ramped to reduce AM splatter in TDD/TDMA systems and can be used to trim the RF output power.

THEORY OF OPERATION

The input port is internally matched to 50 ohms. Return loss is typically 15–16 dB in the 800–1000 MHz range. The output port is nearly 50 ohms but is an open collector and therefore requires an external bias inductor. Using an RF choke will result in a 11–12 dB output return loss. However, a 10 nH inductor will improve it to 15–20 dB. A 10 nH inductor is small enough in value to be printed on the board. DC blocks are required on the input and output. Values of 100 pF are recommended.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. A series RF choke is recommended to keep the RF signal off the supply line. A 10 nF decoupling capacitor is recommended on the V_{bias} line but does not need to be very close to the IC.

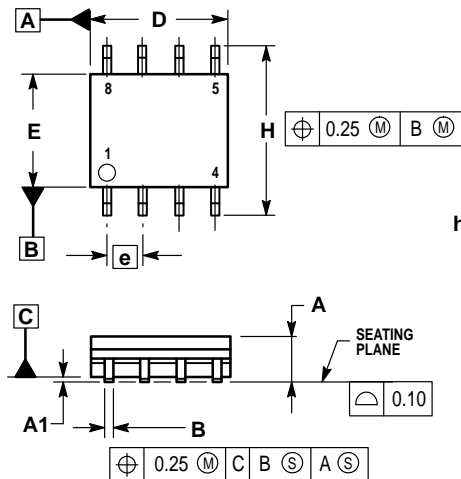
The V_{bias} pin can be used several ways. Tying it directly to V_{CC} will maximize the bias current which will maximize linearity. Adding a series resistor will reduce the bias current which will improve efficiency. Figure 9 shows the efficiency versus output power with V_{bias} tied to V_{CC} . The series resistor will cause these curves to shift to the left. The RF output power can be trimmed by using a variable resistor. The V_{bias} pin can also be used to power down the IC or, in the case of TDD/TDMA systems, to ramp the IC. By applying a linear ramp voltage, such as the one provided by the MRFIC2004, it has been demonstrated to meet the CT2 Common Air Interface splatter specifications.

The MRFIC2006 is internally temperature compensated. For input powers of –5.0 to 0 dBm the output power temperature variation is typically less than 0.2 dB from –35 to +85°C.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS ARE IN MILLIMETERS.
 3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

CASE 751-05 ISSUE S

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