DATA SHEET

O K I A S I C P R O D U C T S

MSM10S0000
0.8 μm Sea of Gates Family
3-V and 5-V Applications

December 1997

Oki Semiconductor

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Oki Semiconductor

MSM10S0000

0.8 µm Sea of Gates Family for 3-V and 5-V Applications

DESCRIPTION

The Oki MSM10S0000 Sea of Gates (SOG) family is a high-performance, high-density semicustom product using Oki's scalable, 0.8 µm drawn (0.6 µm effective), two-layer metal, polysilicide, dual-well process which has been adapted for logic from Oki's proven high volume 4- and 16-Meg DRAM manufacturing process.

The MSM10S0000 features a wide operating range, from 2.7 to 5.5 V, timing driven layout, and clock skew less than 1.0 ns. Also featured is speed / density logic permitting optimized critical paths with high-speed logic functions and reduced total chip power and cell area for noncritical paths with high-density logic. Additionally the MSM10S0000 has both memory and high-performance, high-density mega macrocells like universal asynchronous receiver / transmitters (UARTs) and 82Cxx. Other features include typical gate delays under 300 ps and flip-flop toggle rates over 500 MHz. Usable two input gate equivalent circuit density exceeds 100k gates.

FEATURES

- 0.8 µm drawn two-metal CMOS
- 7 sizes from 11k to 225k total gates
- Up to 840 configurable I / O cells
- Clock tree macrocells with ≤1 ns clock skew (FO = 2,000 at 70 MHz)
- Usable density from 4k to >80k gates (maximum random logic)
- Slew rate controlled outputs
- I / Os may be V_{SS} , V_{DD} , CMOS, TTL, 3-state, 2 to 48 mA
- ESD 4 kV, latchup >200 mA
- ATVG using scan macros
- Compatible with Oki's MSM91S000 0.8 µm Customer Structured Array (CSA) products
- JTAG-Boundary Scan,small computer system interface (SCSI) and RTC cells in development
- Supports most popular EWS: Cadence, DAZIX, IKOS, Mentor Graphics, Synopsys, Valid and VIEWLogic
- Timing driven layout for speed enhanced net and path control
- Efficient standard product library of 82Cxx, UART and multiport memories
- 3-V version for low power

MSM10S0000 FAMILY

Part Number	Raw Gates	Typical Usable Gates Logic Only	No. of I/O Cells	No. of Configurable I/O Pads (Wire Bond)
MSM10S0050	5,148	2,214	144	72
MSM10S0110	10,864	3,693	200	100
MSM10S0210	21,330	7,252	272	136
MSM10S0300	30,268	10,291	320	160
MSM10S0570	57,018	19,386	432	216
MSM10S0980	98,020	33,326	560	280

ARRAY ARCHITECTURE

The primary components of a 0.8 µm SOG circuit include:

- I/O base cells
- Configurable I/O pads for V_{DD}, $V_{SS,}$ or I/O
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells contain n-channel and p-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 16 dedicated corner pads for power and ground use during wafer probing. There are four pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and the output drive transistors (V_{DDO} and V_{SSO}) as shown in *Figure 1*.

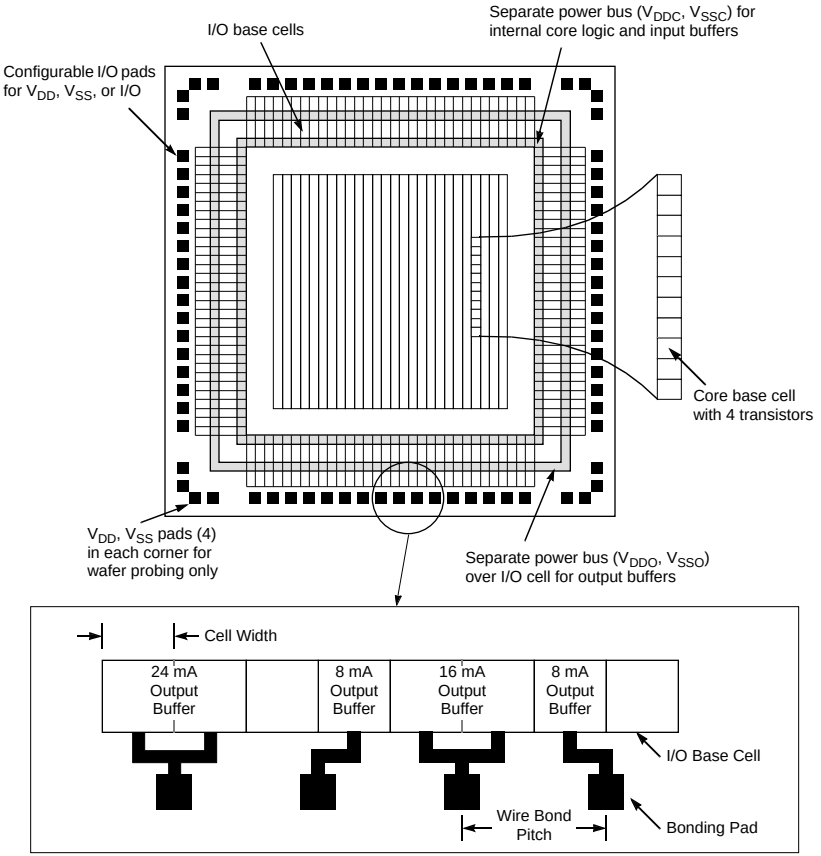


Figure 1. MSM10S0000 Array Architecture

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Condition	Value	Unit
Power supply voltage	V_{DD}	T_j = 25°C V_{SS} = 0 V	-0.5 to +6.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output current per I/O base cell	I_O		-16 to +16	mA
Current per power PAD	I_{PAD}		-90 to +90	mA
Storage temperature			-65 to +150	°C
ESD voltage (MIL-STD-883C 3015.7)			4000	V
Input/output latch-up current			±200	mA

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rated Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
		4.5	5.0	5.5	V
Operating temperature	T_a	-40	+25	+85	°C
Input rise/fall time (normal type) [1] [2]	trA, tfA	–	2	500	ns
	trB, tfB	–	2	500	ns
Input rise/fall time (Schmitt Trigger type) [3] [4]	trC, tfC	–	–	60	µs
	trD, tfD	–	–	200	µs

1. trA, tfA – TTL interface normal input buffer
2. trB, tfB – CMOS interface normal input buffer
3. trC, tfC – TTL interface Schmitt Trigger input buffer
4. trD, tfD – CMOS interface Schmitt Trigger input buffer

Operating Range (V_{SS} = 0 V)

Parameter	Symbol	Rated Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Ambient temperature	T_a	-40 to +85	°C
Oscillation frequency [1]	f_{OSC}	30 k to 50 M	Hz

1. Oscillator macrocells supported for V_{DD} = 4.5 to 5.5 V.

DC Characteristics (V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_j = -40° to +85°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min.	Typ. [1]	Max.	
"H" level input voltage	V_{IH}	TTL input	1.8	–	V_{DD}+0.5	V
		CMOS input	0.7xV_{DD}	–	V_{DD}+0.5	V
"L" level input voltage	V_{IL}	TTL input	-0.5	–	0.5	V
		CMOS input	-0.5	–	0.3xV_{DD}	V
TTL level Schmitt Trigger input threshold voltage	V_{t+}	–	–	1.3	1.8	V
	V_{t-}	–	0.5	1	–	V
	ΔVT	V_{t+} - V_{t-}	0.1	0.3	–	V
CMOS level Schmitt Trigger input threshold voltage	V_{t+}	–	–	2	0.76xV_{DD}	V
	V_{t-}	–	0.24xV_{DD}	1	–	V
	ΔVT	V_{t+} - V_{t-}	0.1xV_{DD}	1	–	V
"H" level output voltage	V_{OH}	I_{OH} = 1, 2, 4, 6, 8, 12 mA	2.2	–	–	V
"L" level output voltage	V_{OL}	I_{OL} = 1, 2, 4, 6, 8 mA	–	–	0.3	V
		I_{OL} = 12 or 24 mA	–	–	0.4	V
"H" level input current	I_{IH}	V_{IH} = V_{DD}	–	0.01	1	µA
		V_{IH} = V_{DD} (50 kΩ pull down)	5	35	120	µA
"L" level input current	I_{IL}	V_{IL} = V_{SS}	-1	-0.01	–	µA
		V_{IL} = V_{SS} (50 kΩ pull up)	-120	-35	-5	µA
		V_{IL} = V_{SS} (3 kΩ pull up)	-2	-.55	-.120	mA
3-state output leakage current	IOZ_H	V_{OH} = V_{DD}	–	0.01	1	µA
	IOZ_L	V_{OL} = V_{SS}	-1	-0.01	–	µA
		V_{OL} = V_{SS} (50 kΩ pull up)	-120	-35	-5	µA
		V_{OL} = V_{SS} (3 kΩ pull up)	-2	-.55	-.12	mA
Stand-by current	I_{DDS}	Output open V_{IH} = V_{DD}, V_{IL} = V_{SS}	–	0.1	10	µA

1. Typical condition is V_{DD} = 3.0 V and T_j = 25°C. Typical process.

AC Characteristics (V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25°C)

Parameter		Driving Type	Condition	Rated Value [1] [2]	Unit
Internal gate delay times	Inverter 2-input NAND 2-input NOR	1x 1x 1x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 1, L = 0 mm	0.31 0.47 0.52	ns
	Inverter	1x 2x 4x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 2, L = 2 mm L = Metal length	0.87 0.67 0.46	ns
	2-input NAND	1x 2x 4x		1.04 0.70 0.54	ns
	2-input NOR	1x 2x 4x		1.29 0.92 0.93	ns
Flip-flop (FD1A)	Delay time: Set-up time: Hold time:	CLK↑ to Q D to CLK↑ CLK↑ to D		2.45 2.60 0.7	ns
Toggle frequency of flip-flop			FO = 1, L = 0 mm	327	MHz
Input buffer delay times	TTL input		Input tr/tf = V_{DD} /1.0 ns FO = 2, L = 2 mm	1.27	ns
	CMOS input		Input tr/tf = V_{DD} /1.0 ns FO = 2, L = 2 mm	0.93	ns
Output buffer delay times	Push-pull	4 mA 8 mA 16 mA 24 mA	CL = 20 pF CL = 50 pF CL = 100 pF CL = 150 pF	3.15 3.21 3.37 3.82	ns
Output buffer transition time (10 - 90%)	Push-pull	Rising Falling	CL = 150 pF Buffer type: 24 mA	6.01 5.75	ns
	Push-pull with slew rate control	Rising Falling		9.70 9.13	ns

1. For the purpose of this table, rated value is calculated as an average of the LH and HL delay times of each macro type.
2. Typical process.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_j = -40° to +85°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ [1]	Max	
"H" level input voltage	V_{IH}	TTL input	2.2	–	V_{DD}+0.5	V
		CMOS input	0.7xV_{DD}	–	V_{DD}+0.5	V
"L" level input voltage	V_{IL}	TTL input	-0.5	–	0.8	V
		CMOS input	-0.5	–	0.3xV_{DD}	V
TTL level Schmitt Trigger input threshold voltage	V_{t+}	–	–	1.7	2.2	V
	V_{t-}	–	0.8	1.3	–	V
	ΔVT	V_{t+} - V_{t-}	0.2	0.4	–	V
CMOS level Schmitt Trigger input threshold voltage	V_{t+}	–	–	3.1	0.76xV_{DD}	V
	V_{t-}	–	0.24xV_{DD}	1.8	–	V
	ΔVT	V_{t+} - V_{t-}	0.6	1.3	–	V
"H" level output voltage	V_{OH}	I_{OH} = 2, 4, 8, 12, 16, 24 mA	3.7	–	–	V
"L" level output voltage	V_{OL}	I_{OL} = 2, 4, 8, 12, 16 mA	–	–	0.4	V
		I_{OL} = 24 or 48 mA	–	–	0.5	V
"H" level input current	I_{IH}	V_{IH} = V_{DD}	–	0.01	10	µA
		V_{IH} = V_{DD} (50 kΩ pull down)	20	100	250	µA
"L" level input current	I_{IL}	V_{IL} = V_{SS}	-10	-0.01	–	µA
		V_{IL} = V_{SS} (50 kΩ pull up)	-250	-100	-20	µA
		V_{IL} = V_{SS} (3 kΩ pull up)	-5	-1.6	-0.5	mA
3-state output leakage current	IOZ_H	V_{OH} = V_{DD}	–	0.01	10	µA
	IOZ_L	V_{OL} = V_{SS}	-10	-0.01	–	µA
		V_{OL} = V_{SS} (50 kΩ pull up)	-250	-100	-20	µA
		V_{OL} = V_{SS} (3 kΩ pull up)	-5	-1.6	-0.5	mA
Stand-by current [2]	I_{DDS}	Output open V_{IH} = V_{DD}, V_{IL} = V_{SS}	–	0.1	100	µA

1. Typical condition is V_{DD} = 5.0 V and T_j = 25°C. Typical process.
2. RAM/ROM should be in powerdown mode.

AC Characteristics (V_{DD} = 5 V, V_{SS} = 0 V, T_j = 25°C)

Parameter		Driving Type	Condition	Rated Value [1] [2]	Unit
Internal gate delay times	Inverter 2-input NAND 2-input NOR	1x 1x 1x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 1, L = 0 mm	0.20 0.31 0.34	ns
	Inverter	1x 2x 4x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 2, L = 2 mm L = Metal length	0.57 0.44 0.30	ns
	2-input NAND	1x 2x 4x		0.68 0.46 0.35	ns
	2-input NOR	1x 2x 4x		0.84 0.60 0.61	ns
Flip-flop (FD1A)	Delay time: Set-up time: Hold time:	CLK↑ to Q D to CLK↑ CLK↑ to D		1.60 1.70 0.0	ns
Toggle frequency of flip-flop			FO = 0, L = 0 mm	500	MHz
Input buffer delay times	TTL input		Input tr/tf = V_{DD} /1.0 ns FO = 2, L = 2 mm	0.83	ns
	CMOS input		input tr/tf = V_{DD} /1.0 ns FO = 2, L = 2 mm	0.61	ns
Output buffer delay times	Push-pull	4 mA 8 mA 16 mA 24 mA	CL = 20 pF CL = 50 pF CL = 100 pF CL = 150 pF	2.06 2.10 2.20 2.50	ns
Output buffer transition time (10 - 90%)	Push-pull	Rising Falling	CL = 150 pF Buffer type: 24 mA	3.93 3.76	ns
	Push-pull with slew rate control	Rising Falling		6.34 5.97	ns

1. For the purpose of this table, Rated Value is calculated as an average of the LH and HL delay times of each macro type.
2. Typical process.

Timing Variation

Delay variations due to process and operating conditions (temperature and voltage) form the total circuit delay factor described by the relationship:

$$\delta = \delta T \times \delta V \times \delta P$$

Values for δT and δV are shown in *Figure 2* and *Figure 3*

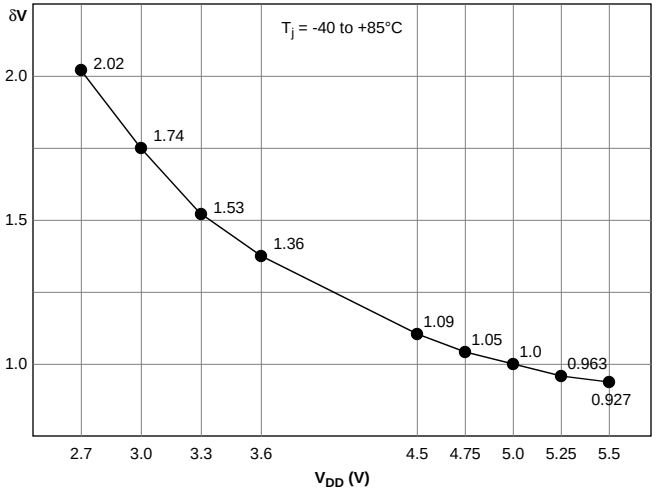


Figure 2. δV vs V_{DD} Characteristics

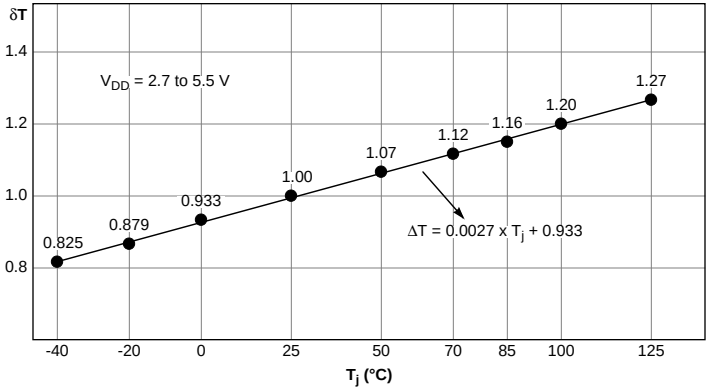
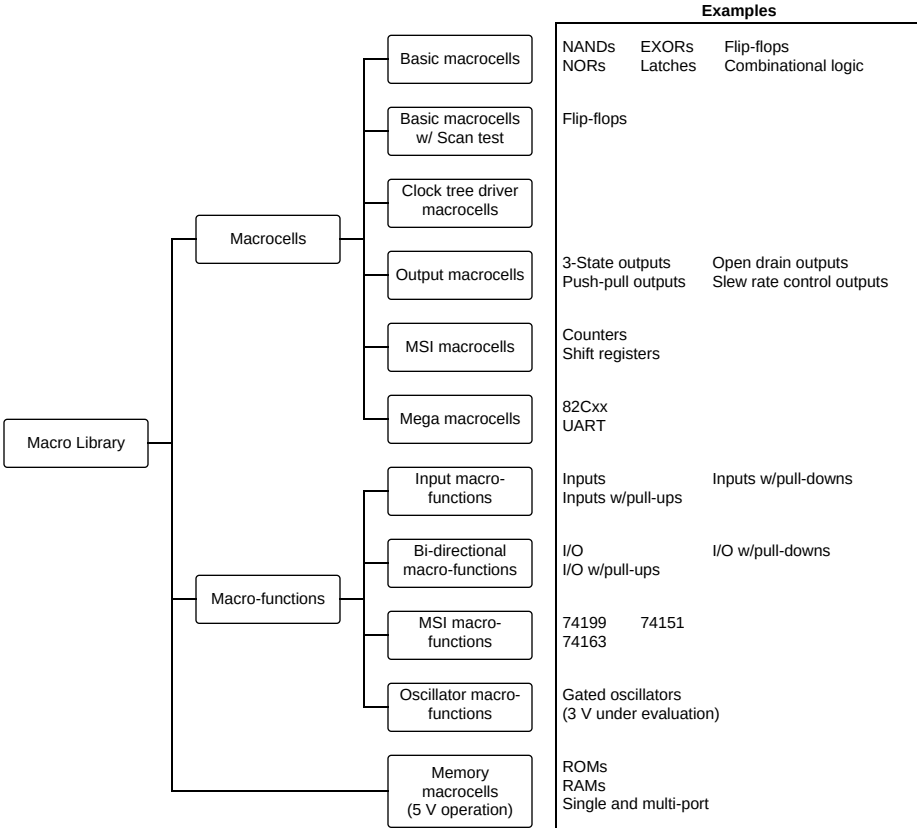


Figure 3. δT vs T_j Characteristics

OKI MACRO LIBRARY (3 V / 5 V)



Clock Tree Driver Macrocells

Oki offers clock tree driver macrocells which guarantee skew time less than 1 ns. Oki's advanced layout software uses a dynamic driver placement and sub-trunk allocation procedure to optimize clock tree implementation. Oki's clock skew management scheme is described in detail in OkiOki's*Clock Skew Management Application Note*

Features

- Clock skew <1.0 ns
- Automatic fanout balancing
- Dynamic sub-trunk allocation
- Single clock driver logic symbol
- Single level clock driver
- Automatic branch length minimization
- Dynamic driver placement

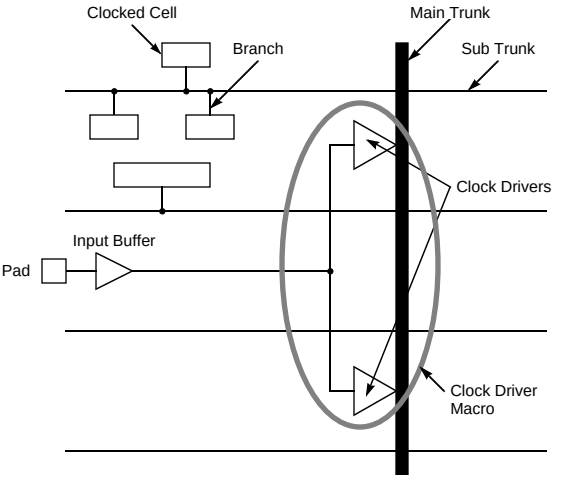


Figure 4. Oki's Clock Tree Structure

Slew Rate Control Output Driver Macrocells

Features

- Reduce simultaneous switching noise
- Reduce output ringing noise

Method

- Split the output transistors into two sets
- Drive the first set; then after it switches and passes the threshold, turn on the next set of transistors.

Available Cells

- All outputs with 8 mA or more are slew rate capable

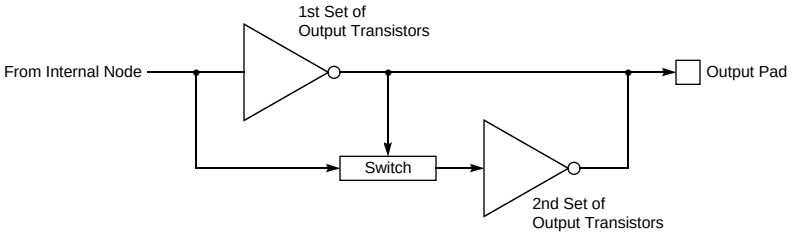


Figure 5. Slew Rate Control Output Buffer

AUTOMATIC TEST VECTOR GENERATION (ATVG)

- Increase fault coverage ≥95%
- Cadence Testscan software
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Multiple scan chains allowed

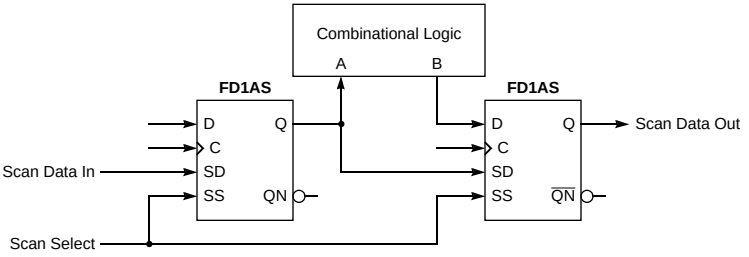
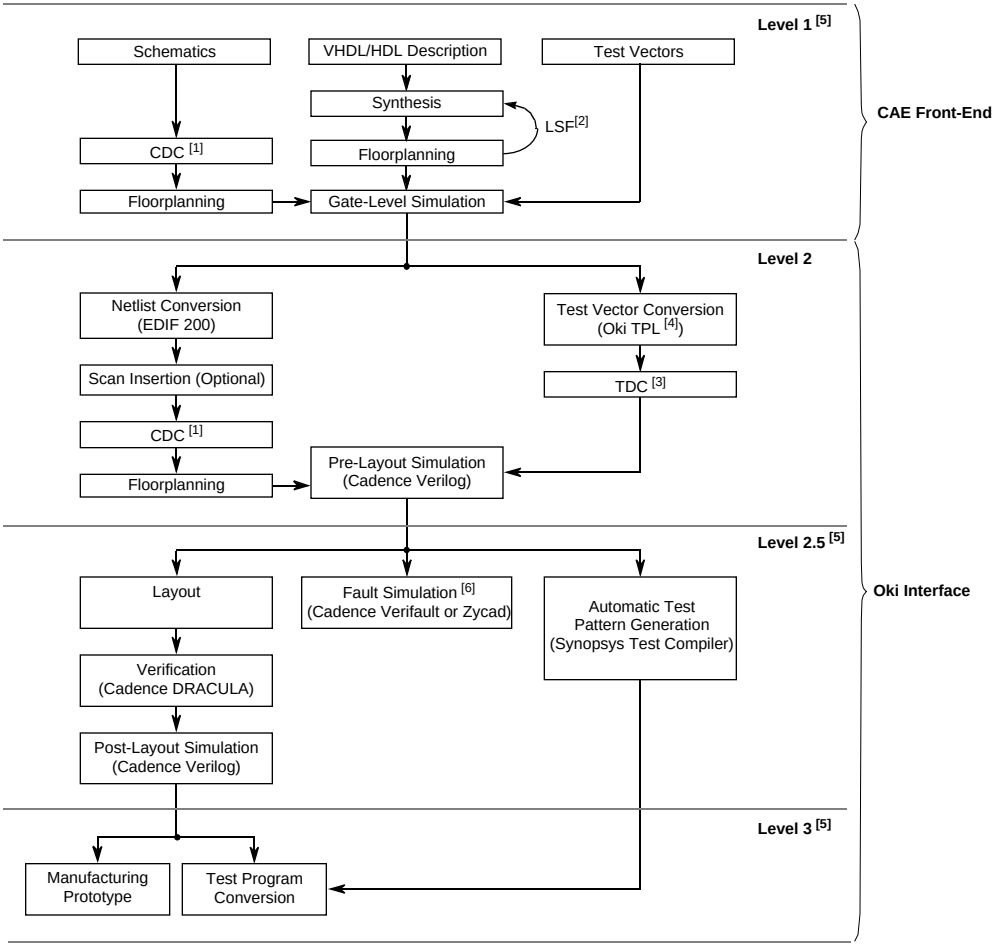


Figure 6. Full Scan Path Configuration

Design Process

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check program (CDC) verifies logic design rules
[2] Oki's Link to Synthesis Floorplanning toolset (LSF) transfers post-floorplanning timing for resynthesis
[3] Oki's Test Data Check program (TDC) verifies test vector rules
[4] Oki's Test Pattern Language (TPL)
[5] Alternate Customer-Oki design interfaces available in addition to standard level 2
[6] Standard design process includes fault simulation

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit

Design Kits

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	HP9000, 7xx IBM RS6000 Sun® [2]	HP-UX AIX SunOS, Solaris	Composer™ Verilog™ Veritime™ Verifault™ Synergy™ Concept™ [3] Leapfrog™	Design capture Simulation Timing analysis Fault grading Design synthesis Design capture VHDL simulation
IKOS	HP9000, 7xx, Sun [2]	HP-UX, SunOS, Solaris	NSIM Gemini/Voyager	Simulation
Mentor Graphics™	HP9000, 7xx Sun [2]	HP-UX SunOS, Solaris	IDEA™ QuickVHDL QuickSim II™ QuickPath™ QuickFault™ QuickGrade™ AutoLogic™ DFT Advisor	Design capture VHDL simulation Logic simulation Timing analysis Fault grading Fault grading Design synthesis Test synthesis
Synopsys (Interface to Mentor Graphics, VIEWLogic)	IBM RS6000 HP9000, 7xx Sun [2]	AIX HP-UX SunOS, Solaris	Design Compiler™ HDL/VHDL Compiler™ Test Compiler™ VSS™	Compilation Design synthesis Test synthesis VHDL simulation
Model Technology, Inc. (MTI)	HP9000, 7xx Sun [2] PC	HP-UX SunOS, Solaris. Win95/NT™	V-System	VHDL Simulation
VIEWLogic	PC Sun [2]	Windows™, Windows NT™ SunOS, Solaris	Workview Office™ Powerview™ Vantage Optium Motive ViewSim™ with VSO	Design capture Simulation VHDL simulation Timing analysis Design synthesis Simulation

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.
3. Sun and HP platform only.

PACKAGE OPTIONS

MSM10S0000 Family

	MSM10S…	0050	0110	0210	0300	0570	0980
	No. I/O Pads [1]	72	100	136	160	216	280
Package	**Pins**						
QFP	44	●	●				
	60	●	●				
	80		●	●	●		
	100			●	●	●	●
	128			●	●	●	●
	136				●	●	●
	144				● [3]	● [4]	● [4]
	160					●	
	176 [2]					●	●
	208 [2]						●
	240 [2]						●
TQFP	44	●	●	●			
	64	●	●	●	●		
	80		●	●	●	●	
	100			●	●	●	
	144				●	●	●
PLCC	44		●	●	●		
	68		●	●	●	●	
	84			●	●	●	
C-PGA	88		●	●	●		
	132			●	●	●	●
	176					❍	●
	208						●

1. You can use I/O pads for input, output, bi-directional, power, or ground.
2. 0.5-mm lead pitch.
3. 0.65-mm lead pitch.
4. 0.65-mm and 0.5-mm lead pitch.

● = Available now.

❍ = Under development.

Notes:

Notes:

Oki Regional Sales Offices

Northwest Area

785 N. Mary Avenue
Sunnyvale, CA 94086
Tel: 408/720-8940
Fax: 408/720-8965

Southwest Area

2302 Martin Street
Suite 250
Irvine, CA 92715
Tel: 714/752-1843
Fax: 714/752-2423

North Central Area

17177 N. Laurel Park Drive
Suite 433
Livonia, MI 48152
Tel: 313/464-7200
Fax: 313/464-1724

South Central Area

2007 N. Collins Blvd.
Suite 303
Richardson, TX 75080
Tel: 214/690-6868
Fax: 214/690-8233

Northeast Area

138 River Road
Shattuck Office Center
Andover, MA 01810
Tel: 508/688-8687
Fax: 508/688-8896

Southeast Area

1590 Adamson Parkway
Suite 220
Morrow, GA 30260
Tel: 404/960-9660
Fax: 404/960-9682

OKI WEB SITE:

http://www.okisemi.com

OKIFAX SERVICE:

Call toll free 1-800-OKI-6994

Oki Stock No: 010394-003

Oki Semiconductor

Corporate Headquarters

785 N. Mary Avenue
Sunnyvale, CA 94086-2909
Tel: 408/720-1900
Fax: 408/720-1918