MSM66P54

One-Time Programmable (OTP) Speech Synthesizer

DESCRIPTION

The MSM66P54 is a one-time-programmable (OTP) version of the MSM6654 speech synthesizer, suitable for evaluation of the MSM6650 family and code development. This part is also suitable for applications requiring small quantities and / or short-term delivery after code completion. The PC-based AR76-202 Speech Development System is used for speech encoding, editing, and programming of the MSM66P54.

When compared to the mask-programmed MSM6654 version, the SOP-packaged version of the MSM66P54 is backwards compatible, while the DIP-packaged version has two extra pins for programming. On the DIP version, programming pins can either be cut off or left open after programming. DIP pin spacing and location allows insertion of the MSM66P54 into an IC socket intended for the MSM6654.

To provide high-quality speech synthesis, all members of the MSM6650 family members implement adaptive differential pulse-code modulation (ADPCM) playback, pulse-code modulation (PCM) playback, 12-bit D / A conversion, and an on-chip -40dB / octave low-pass filter (LPF). In addition, easy-to-use "beep" tones, a two-channel mixing function, a melody function, a fade-out function, and a random playback function are included. Also, an on-chip edit ROM can form sentences by catenating phrases, making external control simpler than before.

Four code versions of the MSM66P54 are available. Stand-alone or microcomputer (MCU) interface modes can be selected by using one of the four available codes. The table below shows the code versions available.

MSM66P54 Code Versions

Part No.	OTP ROM	Mode	Interface/Standby Features
MSM66P54-01	1 Mbit	MCU Interface Mode	Serial Interface
MSM66P54-02	1 Mbit	MCU Interface Mode	Parallel Interface
MSM66P54-03	1 Mbit	Standalone Mode	Standby Function
MSM66P54-04	1 Mbit	Standalone Mode	No Standby Function

FEATURES

- Single-chip synthesizer
- 4-bit ADPCM or 8-bit PCM sound playback
- Melody function
- Edit ROM function
- Built-in two-channel mixing function
- Internal random playback function
- Fade-out function
- Built-in "beep" tones at 0.5, 1.0, 1.6, and 2.0 kHz
- Sampling frequency of 4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16, or 32 kHz[1]
- Up to 127 phrases
- Internal 12-bit D / A converter
- Internal -40 dB / octave low-pass filter (LPF)
- Built-in standby function
- Selectable RC oscillation or ceramic / crystal oscillation
- Package options include 20-pin DIP (DIP20-P-300), 24-pin SOP (SOP24-P-430-2K), or die

1. 32 kHz is not available when RC oscillation is selected

The table below shows the additional functions available in the MSM6650 family when compared to the family's predecessor, the MSM637x family.

Comparison of MSM6376 and MSM6650 Families

	MSM6650 Family	MSM637x Family
Control Method	Standalone mode Microcomputer mode - parallel input Microcomputer mode - serial input	CPU input - software control
Speech synthesis method	4-bit ADPCM or 8-bit PCM/Melody PCM	4-bit ADPCM
"Beep" tone frequency (length)	0.5, 1.0, 1.6, or 2.0 kHz (User-specified length of variable duration)	1.0 or 2.0 kHz, (User-specified length, fixed at either 64, 128, 250, or 500 ms)
Sampling frequency (f_S)	Eight frequencies (4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0, or 32.0 kHz)	Three frequencies at two oscillator frequencies (4.0, 6.4, or 8.0 kHz with f_{OSC} = 64 kHz; 16.0, 25.6, or 32.0 kHz with f_{OSC} = 256 kHz)
Master clock frequency	256 kHz (RC) / 4.096 MHz (crystal)	40 kHz ~ 256 kHz
LPF attenuation factor	–40 dB/octave	–24 dB/octave
LPF cut-off Frequency (f_{CUT}), kHz	f_{CUT}: 1.8, 2.6, 2.6, 3.2, 4.2, 5.1, 6.4, 12.8 f_{SAM}: 4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0, 32.0	f_{CUT}: 1.5, 3.0, 3.0 f_{SAM}: 4.0, 6.4, 8.0
Maximum phrase number	127 (in MCU Interface Mode)	111
Pull-up/pull-down resistors	Built in	—
Standby conversion time	200 ms	3 Sec
Maximum external ROM	64 Mbit	16 Mbit
Added functions in edit ROM	Fade-out Random playback Melody playback PCM playback Serial input control	No Edit ROM

SPEECH DURATION

Type	Data ROM Capacity [1]	Maximum Speech Duration				
		f_{SAM} = 4.0 kHz	f_{SAM} = 6.4 kHz	f_{SAM} = 8.0 kHz	f_{SAM} = 16.0 kHz	f_{SAM} = 32.0 kHz
MSM6650	64 Mbits [2]	> 1 hour	> 40 minutes	> 30 minutes	> 15 minutes	> 8 minutes
MSM6652	288 Kbit	16.9 sec	10.5 sec	8.4 sec	4.2 sec	2.1 sec
MSM6653	544 Kbit	31.2 sec	19.5 sec	15.6 sec	7.8 sec	3.9 sec
MSM6654	1 Mbit	63.8 sec	39.9 sec	31.9 sec	15.9 sec	7.9 sec
MSM66P54 [3]	**1 Mbit**	**63.8 sec**	**39.9 sec**	**31.9 sec**	**15.9 sec**	**7.9 sec**
MSM6655	1.5 Mbit	96.5 sec	60.3 sec	48.2 sec	24.1 sec	12.0 sec
MSM6656	2 Mbit	129.1 sec	80.7 sec	64.5 sec	32.2 sec	16.1 sec

[1] Actual ROM area in MSM6652, MSM6653, MSM6654, MSM6655, and MSM6656 is smaller by 22 Kbits.

[2] Via external ROM only (no on-chip ROM available).

[3] OTP version.

PACKAGE DRAWINGS

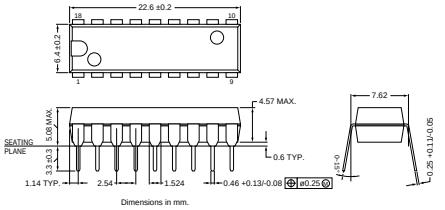

Figure 1. MSM66P54 Mechanical Drawing (DIP20-P-300-W1 Package)

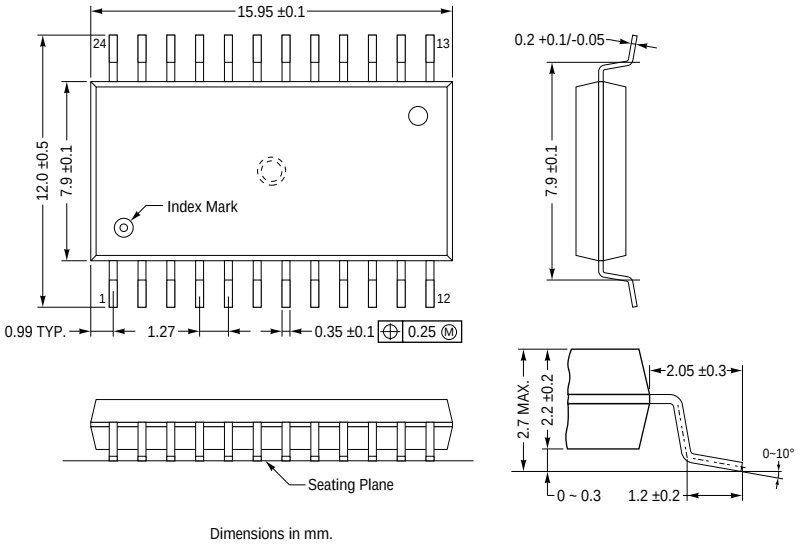

Figure 2. MSM66P54 Mechanical Drawing (SOP24-P-430-2K Package)

BLOCK DIAGRAMS

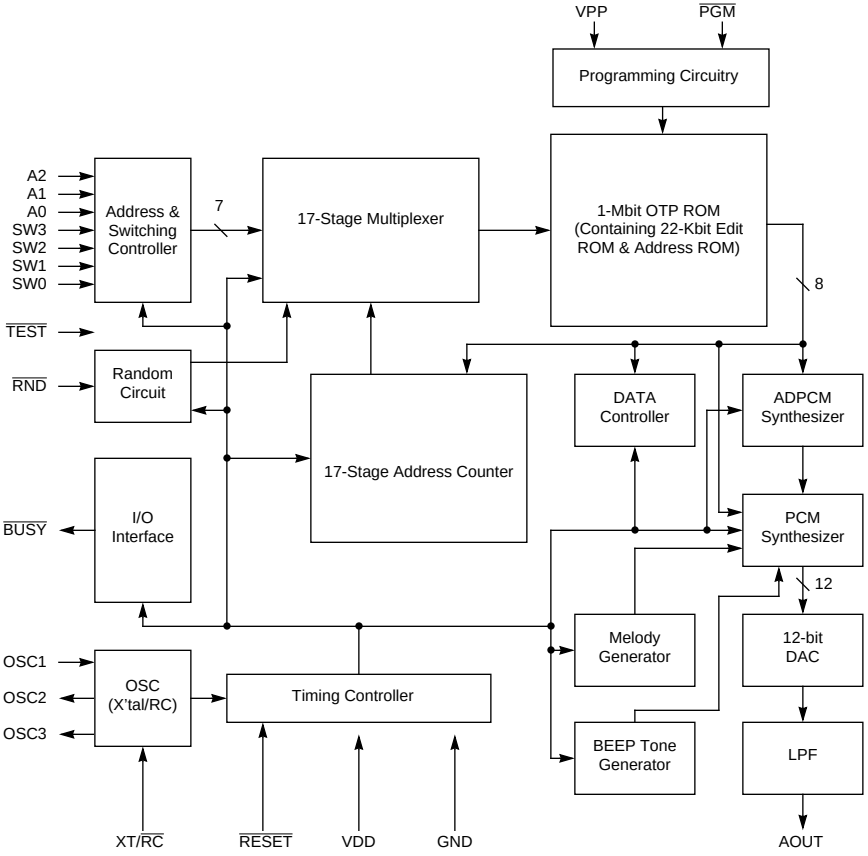

Figure 3. MSM66P54-03/-04 Block Diagram (Standalone Mode)

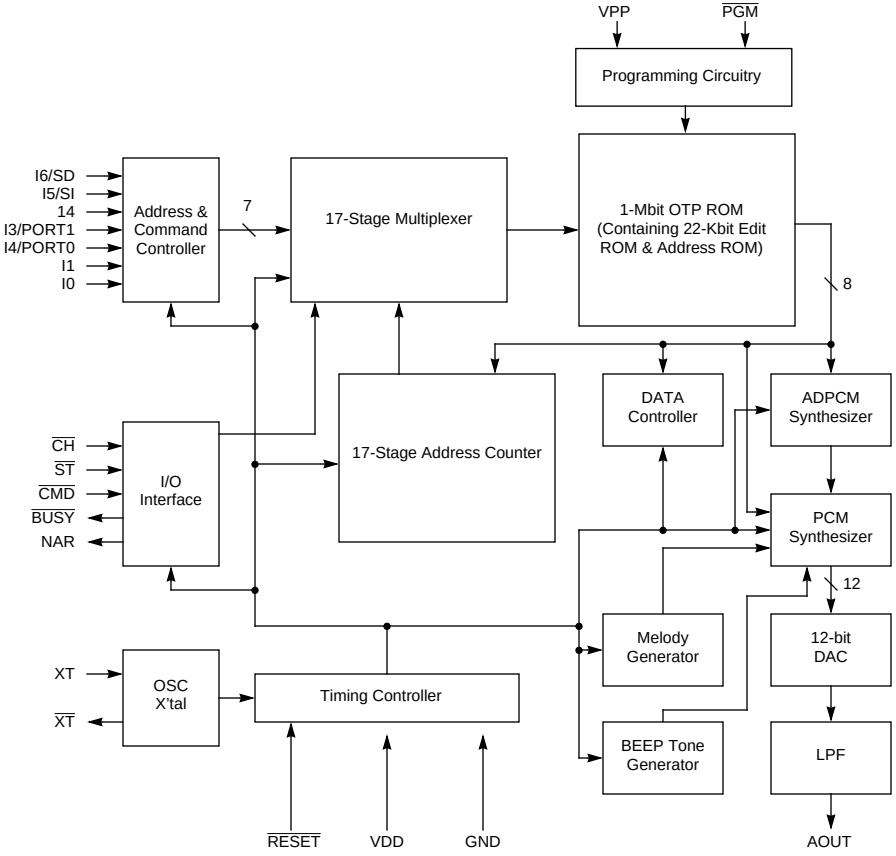

Figure 4. MSM66P54-01/-02 Block Diagram (MCU Interface Mode)

PIN CONFIGURATION

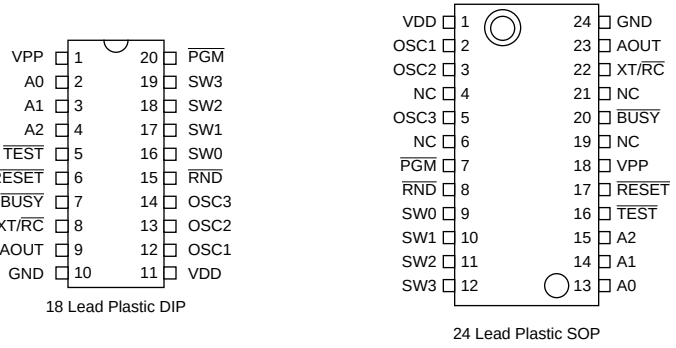

Figure 5. MSM66P54-03/-04 Configuration (Standalone Mode)

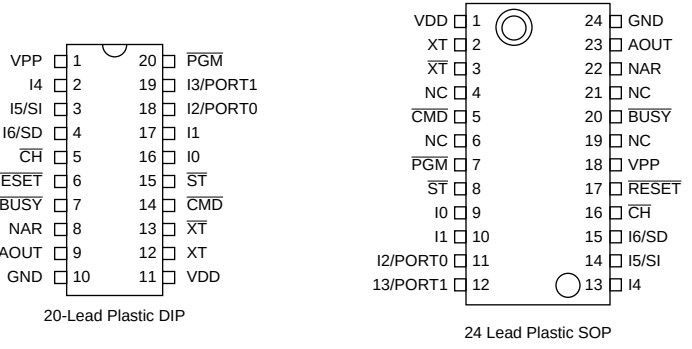

Figure 6. MSM66P54-01/-02 Pin Configuration (MCU Interface Mode)

PIN DESCRIPTIONS

MSM66P54-03/-04 Pin Descriptions (Standalone Mode)

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	**Reset**. Setting this pin to "L" puts the device in standby status. At this time, oscillation stops, A_{OUT} is pulled to GND, and the device is initialized. The MSM6650 Family devices have an internal power-on reset. To operate the power-on reset correctly, power should ramp up within 1 ms. If this is not possible, apply a $\overline{\text{RESET}}$ pulse when power is turned on. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	**Busy**. This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
XT/$\overline{\text{RC}}$	I	**X'tal/RC selectable pin**. Set to "H" level when using ceramic/crystal oscillation. Set to "L" level when using RC oscillation.
A_{OUT}	O	**Sound output**. This is the synthesized output pin of the internal low-pass filter.
GND	–	**Ground**.
V_{DD}	–	**Power supply**.
OSC1	I	**Oscillator 1.** This pin is a ceramic/crystal oscillator connection pin when using ceramic or crystal oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
OSC2	O	**Oscillator 2**. This pin is a ceramic/crystal oscillator connection pin when using a ceramic or crystal oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
OSC3	O	**Oscillator 3.** Leave open if using a ceramic/crystal oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
$\overline{\text{RND}}$	I	**Random Playback.** Random playback starts when the $\overline{\text{RND}}$ pin is set to a "L" level. At the fall of $\overline{\text{RND}}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
$\overline{\text{TEST}}$	I	**Test Mode**. Set to "H" level. This pin has an internal pull-up resistor.
SW0 ~ SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 ~ SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
A0 ~ A2	I	**Phrase Inputs.** Phrase input pins corresponding to playback. The A0 input becomes invalid when the random playback function is used.
VPP	–	Power-supply voltage for programming the on-chip OTP ROM. Set to a "H" level or open during normal operation.
$\overline{\text{PGM}}$	I	Interface pin for AR76-202 Speech Development System. Set to a "L" level or open during normal operation. This pin has an internal pull-down resistor.

MSM66P54-01/-02 Pin Descriptions (Microcomputer Interface Mode)

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	**Reset**. Setting this pin to "L" puts the device in standby status. At this time, oscillation stops, A_{OUT} is pulled to GND, and the device is initialized. The MSM6650 Family devices have an internal power-on reset. To operate the power-on reset correctly, power should ramp up within 1 ms. If this is not possible, apply a $\overline{\text{RESET}}$ pulse when power is turned on. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	**Busy**. This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
NAR	O	**Next Address Request.** The $\overline{\text{CMD}}$ and $\overline{\text{ST}}$ input is valid when NAR is at a "H" level. When the $\overline{\text{CH}}$ pin is at "H" level, NAR becomes a Channel 1 status signal. When the $\overline{\text{CH}}$ pin is at "L", NAR becomes a Channel 2 status signal. This pin indicates whether the register that latches the addresses of I0~I6 in the Address & Command Controller (refer to the block diagram) is empty or not. At "H" level, it is empty and new address data may be applied. At power-on, NAR is "H" level.
AOUT	O	**Analog Sound Output**. Either the D/A converter or the low-pass filter output can be selected by a command input.
GND	–	**Ground.**

MSM66P54-01/-02 Pin Descriptions (Microcomputer Interface Mode) (Continued)

V_{DD}	–	**Power supply.**
XT	I	**Ceramic/Crystal Oscillator Input.** A feedback resistor of 0.5~5M Ω between XT and $\overline{XT}$ is built in this pin. When using an external clock, input to this pin.
$\overline{XT}$	O	**Ceramic/Crystal Oscillator Output**. When using an external clock, leave this pin open.
$\overline{CMD}$	I	**Command Input and Option Selection Control**. Command and option input is enabled if the $\overline{ST}$ pin is set to a "L" level when the $\overline{CMD}$ pin is "L." Set the $\overline{CMD}$ pin to a "H" level when $\overline{CMD}$ is not used and when using the serial input interface. This pin has an internal pull-up resistor.
$\overline{ST}$	I	**Start**. Speech synthesis starts with the fall of $\overline{ST}$. With the rise of $\overline{ST}$, addresses I0~I6 are latched inside the IC. Input $\overline{ST}$ when the NAR status signal for Channels 1 and 2 is at a "H" level. A pull-up resistor is built into this pin.
$\overline{CH}$	I	**Channel control signal**. Channel 1 is selected at "H" level and Channel 2 is selected at "L" level. A pull-up resistor is built into this pin.
I6/SD	I	**Command Input 6/Serial Data Input.** When the parallel input option is selected, this is a command and phrase input pin. When the serial input option is selected, this pin becomes a serial data (command and address) input pin.
I5/SI	I	**Command Input 5/Serial Clock Input**. When the parallel input option is selected, this is a command and phrase input pin. When the serial input option is selected, this pin becomes a serial clock input pin.
I4	I	**Command Input 4.** When the parallel input option is selected, this is a command and phrase input pin. When the serial input option is selected, leave this pin at a "L" level. A pull-up resistor is built into this pin.
I3/PORT1	I/O	**Command Input 3/Port 1 Output.** When the parallel input option is selected, this is a command and phrase input pin. When the serial input option is selected, this pin becomes a port output pin. The output from this port can be varied by command inputs from the microcomputer interface.
I2/PORT0	I/O	**Command Input 2/Port 0 Output.** When the parallel input option is selected, this is a command and phrase input pin. When the serial input option is selected, this pin becomes a port output pin. The output from this port can be varied by command inputs from the microcomputer interface.
I0, I1	I	**Command Input 1/0.** These are command and user specified phrase input pins when parallel input is optionally selected. When the serial input option is selected, leave these pins at a "L" level. A pull-up resistor is built into these inputs.
VPP	–	Power-supply voltage for programming the on-chip OTP ROM. Set to a "H" level or open during normal operation.
$\overline{PGM}$	I	Interface pin for AR76-202 Speech Development System. Set to a "L" level or open during normal operation. This pin has an internal pull-down resistor.

APPLICATION CIRCUIT EXAMPLES

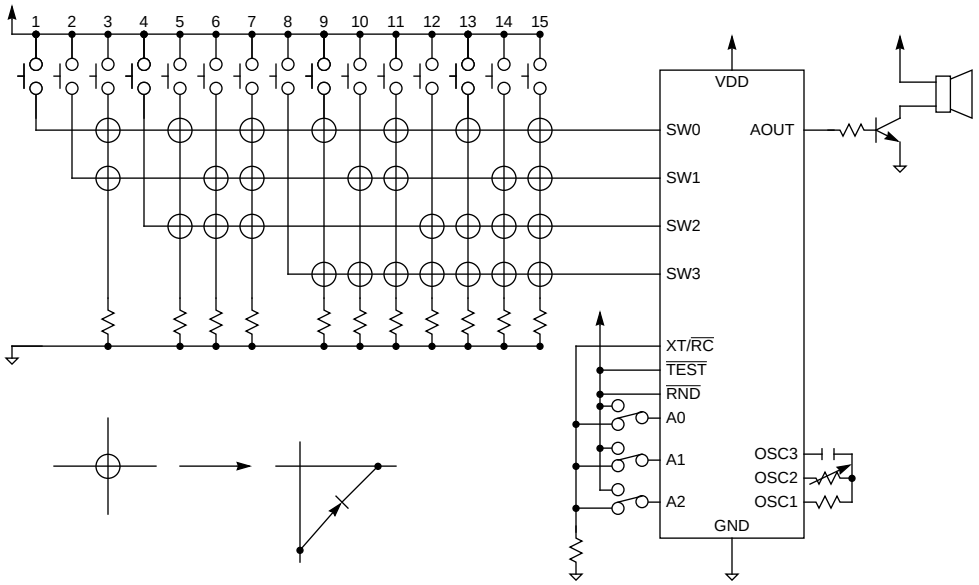

Figure 7. Application Circuit in Standalone Mode with Serial Input Interface

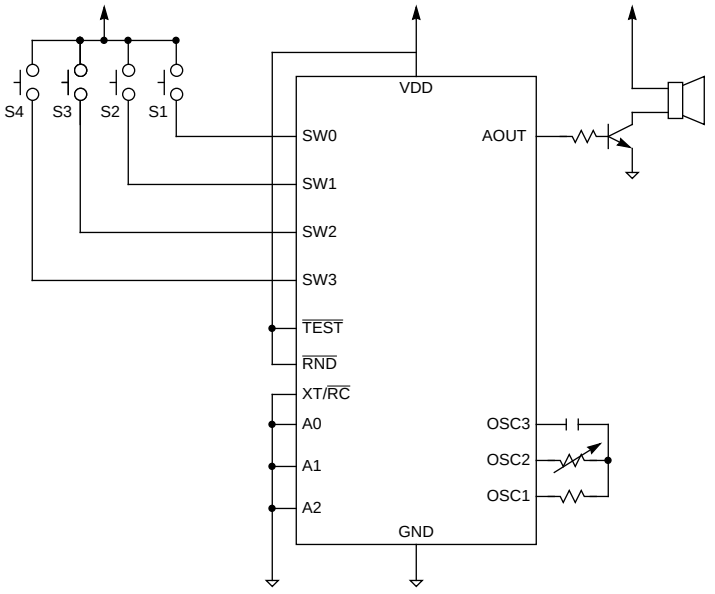

Figure 8. Application Circuit in Standalone Mode with Parallel Input Interface

The following table shows a comparison between switches and speech playback addresses.

Switches and Speech Playback Address Comparison

	A2	A1	A0	SW3	SW2	SW1	SW0	ADR
S1	0	0	0	0	0	0	1	01
S2	0	0	0	0	0	1	0	02
S3	0	0	0	0	1	0	0	04
S4	0	0	0	1	0	0	0	08

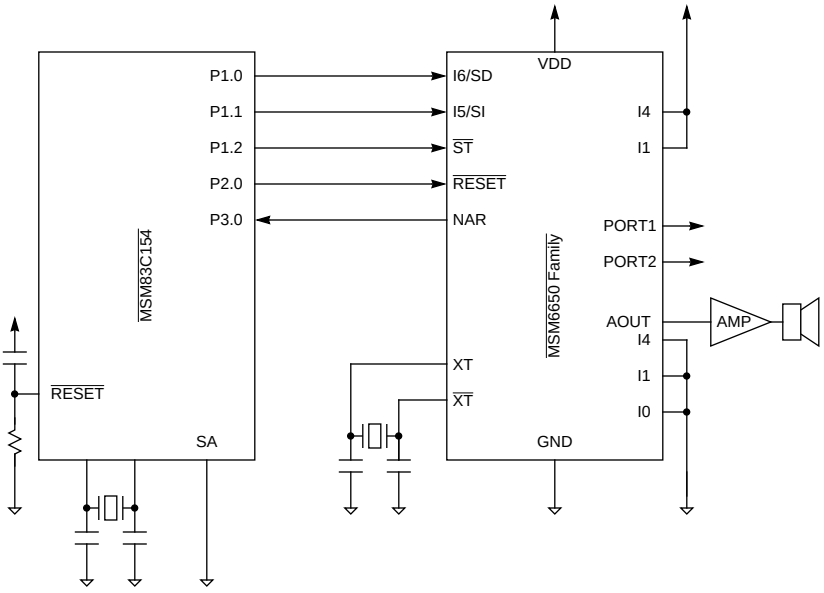

Figure 9. Application Circuit in MCU Interface Mode with a Serial Input Interface

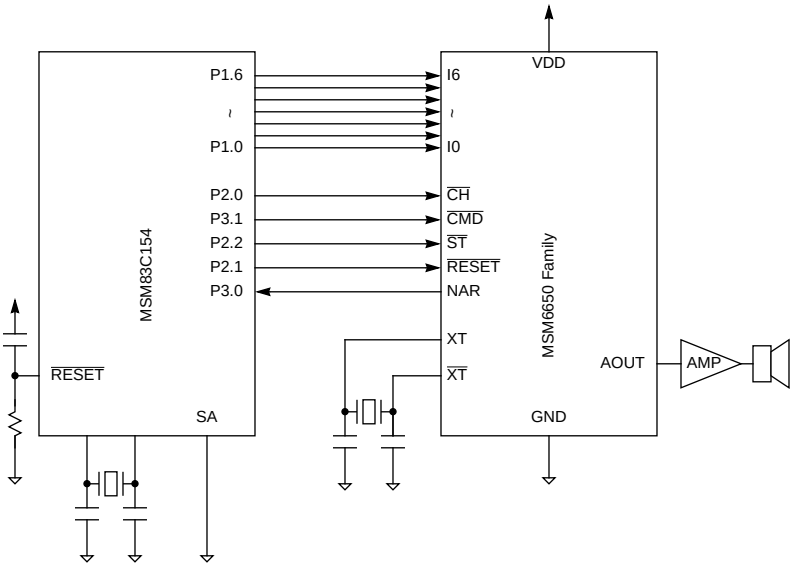

Figure 10. Application Circuit in MCU Interface Mode with a Parallel Input Interface

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	T_a = 25° C	-0.3 ~ 7.0	V
Input voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage temperature	T_{stg}	–	-55 ~ 150	° C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Rated Value	Unit
Power supply voltage	V_{DD}	**LPF output**	+2.7 ~ +5.5	V
		DAC Output [1]	+2.4 ~ +5.5	
Operating temperature	T_{OP}	–	-10 ~ 70	°C
Original oscillation frequency 1	f_{OSC}	When X'tal selected	3.5 ~ 4.5	MHz
Original oscillation frequency 2	f_{OSC2}	When RC selected [2]	200 ~ 300	kHz

[1] In Microcomputer Interface Mode only.

[2] The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the R and C of the external parts.

DC Characteristics (V_{DD} = 5.0 V, GND = 0 V, Ta = -10 ~ 70° C)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}	–	4.2	–	–	V
"L" input voltage	V_{IL}	–	–	–	0.8	V
"H" output voltage	V_{OH}	I_{OH} = -1 mA	4.6	–	–	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	–	–	10	µA
"H" input current 2	I_{IH2}	Internal pull-down resistance	-200	-90	-30	µA
"L" input current 1	I_{IL1}	V_{IL}=GND	-10	–	–	µA
"L" input current 2	I_{IL2}	Internal pull-up resistance	30	90	200	µA
Operating power consumption	I_{DD}	–	–	6	10	mA
Standby power consumption	I_{DS}	–	–	–	10	µA
LPF driving resistor	R_{AOUT}	–	50	–	–	kΩ
LPF output impedance	R_{LFP}	I_F = 100 µA	–	1	3	kΩ

DC Characteristics (V_{DD} = 3.1 V, GND = 0 V, T_a = -10 ~ 70° C)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}	–	2.7	–	–	V
"L" input voltage	V_{IL}	–	–	–	0.5	V
"H" output voltage	V_{OH}	I_{OH} = -1 mA	2.6	–	–	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	–	–	10	µA
"H" input current 2	I_{IH2}	Internal pull-down resistance	-100	-30	-10	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" input current 2	I_{IL2}	Internal pull-up resistance	10	30	100	µA
Operating power consumption	I_{DD}	–	–	4	7	mA
Standby power consumption	I_{DS}	–	–	–	1	µA
LPF driving resistor	R_{AOUT}	–	50	–	–	kΩ
LPF output impedance	R_{LPF}	I_F = 100 µA		1	3	kΩ

AC Characteristics (Standalone Mode, V_{DD} = 5.0 V, GND = 0 V, T_a = 10 ~ 70° C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Master clock duty cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ input pulse width	$tw_{(\overline{RST})}$	–	10	–	–	µs
$\overline{\text{RESET}}$ input time after power-on	$td_{(\overline{RST})}$	–	0	–	–	µs
$\overline{\text{RND}}$ input pulse width	$tw_{(\overline{RAN})}$	Function details 5.2	100	–	–	µs
SW0 ~ SW3 input pulse width	$tw_{(\overline{SW})}$	–	16	–	–	ms
$\overline{\text{BUSY}}$ output time	t_{SBS}	–	–	–	10	µs
$\overline{\text{BUSY}}$ output time	t_{BN}	At f_{SAM} = 8 kHz	350	375	400	µs
Chattering prevention time	t_{CHA}	–	14	15	16	ms

AC Characteristics (Standalone Mode, V_{DD} = 5.0 V, GND = 0 V, T_a = 10 ~ 70° C) (Continued)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
D/A converter change time	t_{DAR}	–	60	64	68	ms
LPF stabilization time	t_L	–	6	8	10	ms
Standby transition period	t_{STB}	–	0.15	0.20	0.25	sec
Random access capture time	t_{RA}	Function details 5.2	16	32	48	µs

AC Characteristics (Microcomputer Interface Mode, V_{DD} = 5.0 V, GND = 0 V, T_a = 10 ~ 70° C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Master clock frequency (1)	$f_{(OSC1)}$	At XT selection	–	4.096	–	MHz
Master clock frequency (2)	$f_{(OSC2)}$	At RC selection [1]	–	256	–	kHz
Master clock duty cycle	f_{duty}	–	40	50	60	%
O($\overline{RESET}$) input pulse width	$tw_{(O(\overline{RST}))}$	–	10	–	–	µs
O($\overline{RND}$) input pulse width	$tw_{(O(\overline{RAN}))}$	–	100	–	–	µs
SW0~SW3 input pulse width	$tw_{(SW)}$	–	32	–	–	ms
($\overline{BUSY}$) output time	t_{SBS}	–	–	–	10	µs
($\overline{BUSY}$) output time	t_{BN}	At fs = 8 kHz	350	375	400	µs
($\overline{BUSY}$) output time	t_{BF}	–	–	–	64	ms
Chattering prevention time	t_{CHA}	–	29	30	31	ms
DA converter change time	t_{DAR}	–	60	64	68	ms
LPF stabilization time	t_L	–	6	8	10	ms
Standby transition period	t_{STB}	–	0.15	0.2	0.25	sec

[1] Accuracy of oscillation frequencies when selecting RC oscillation strongly depends on the accuracy of the externally installed capacitor and resistor.

Timing Waveforms

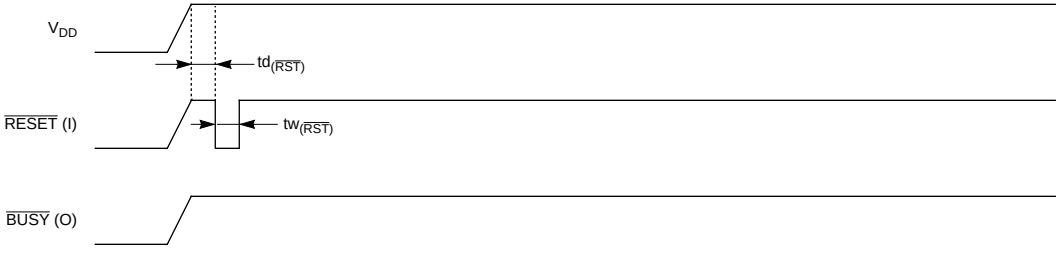

Figure 11. Power-On Timing

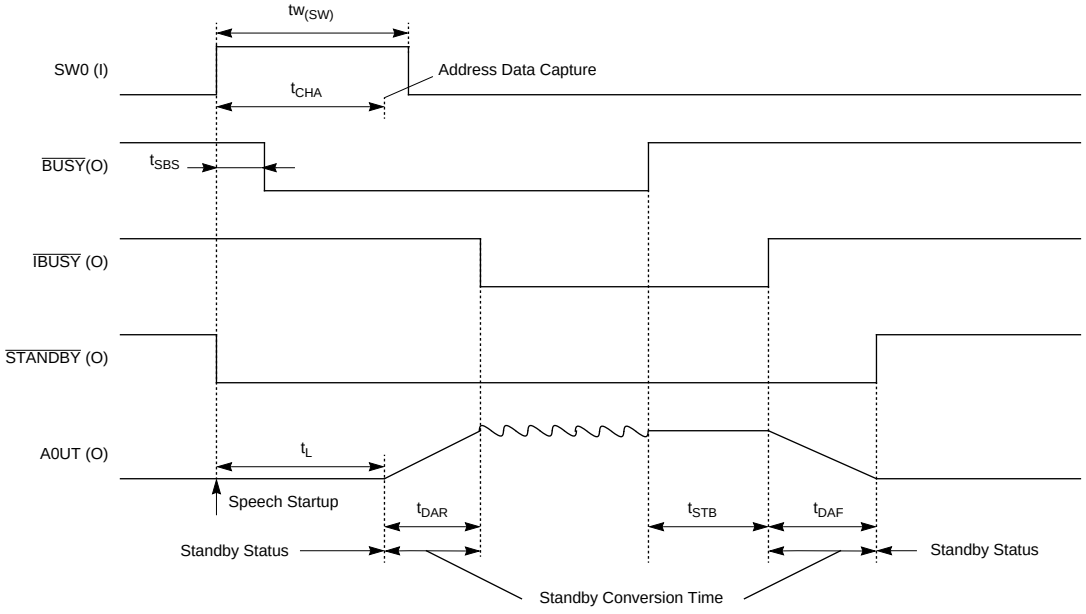

Figure 12. Activation of Standby State Timing

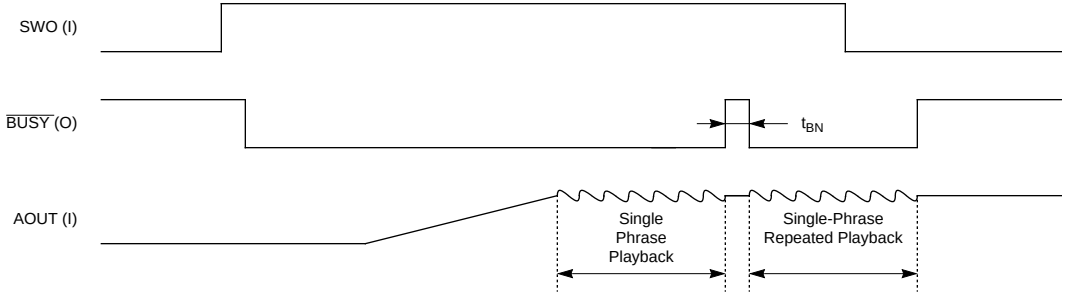

Figure 13. Repeated Playback Timing – Standalone Mode

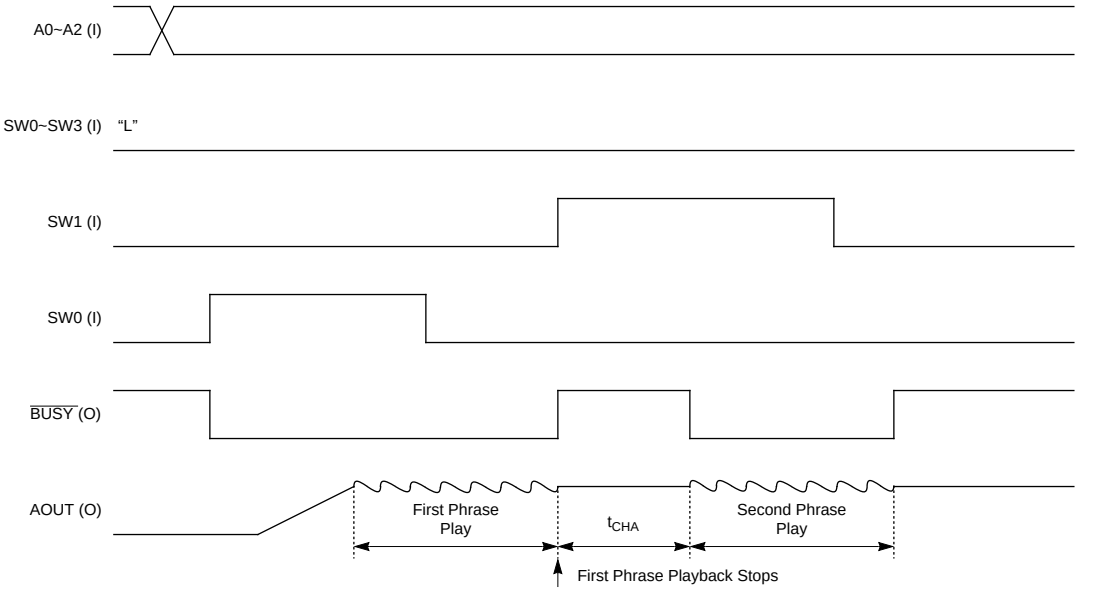

Figure 14. Playback Timing during Transition of SW0 ~ SW3 – Standalone Mode

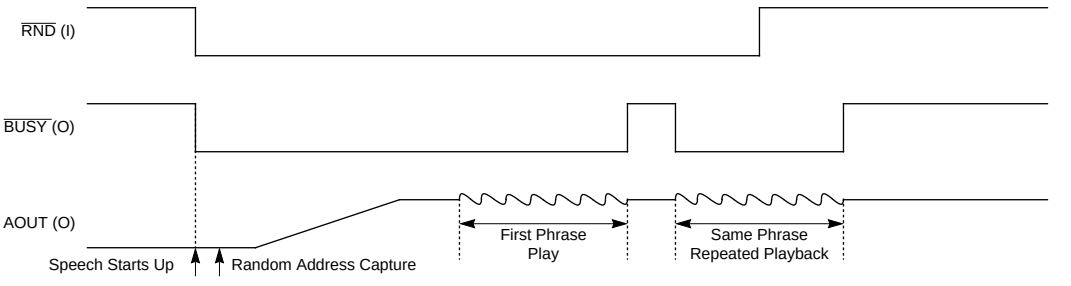

Figure 15. Repeated Random Playback Timing – Standalone Mode

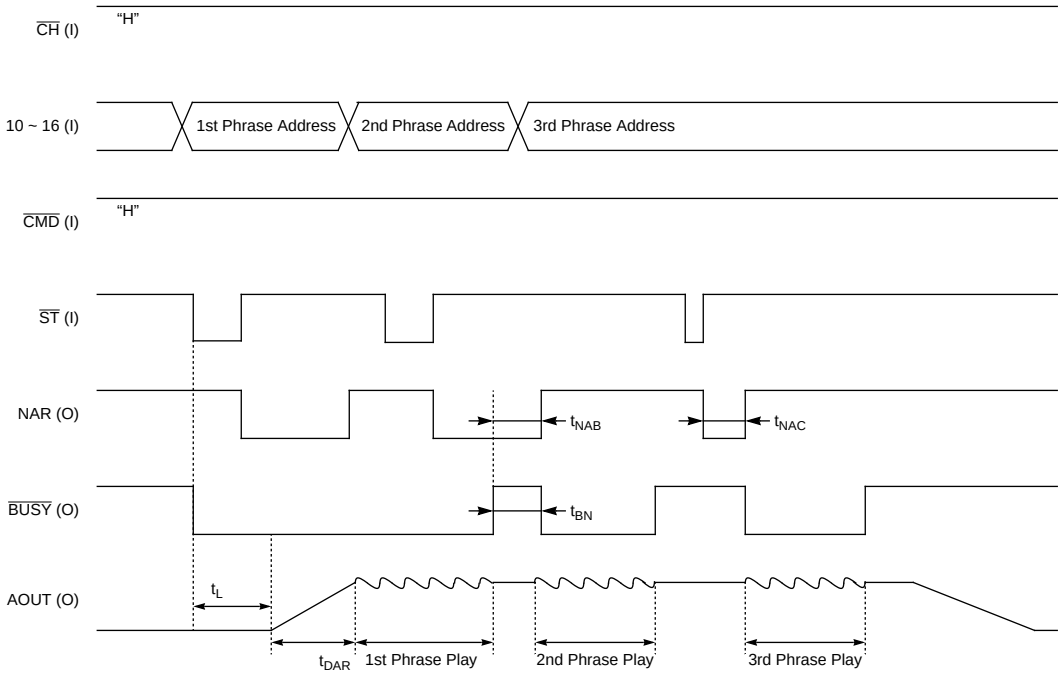

Figure 16. Channel 1 Playback Timing with No External Commands – Microcomputer Interface Mode with Parallel Input

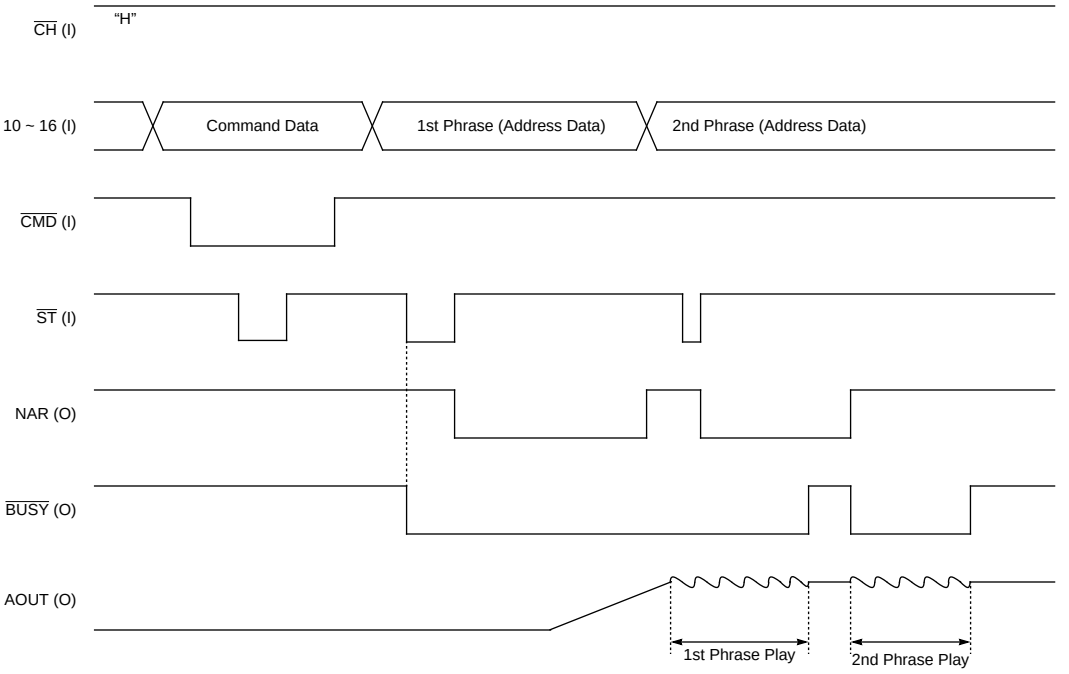

Figure 17. Channel 1 Playback Timing when External Commands are Used – Microcomputer Interface Mode with Parallel Input

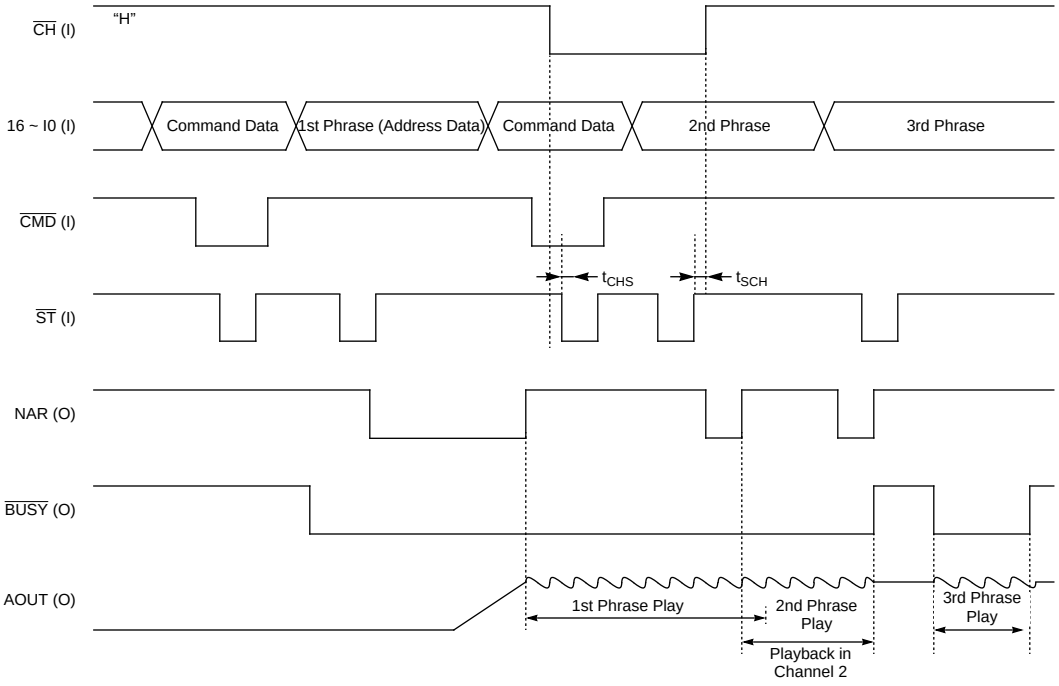

Figure 18. Channels 1 and 2 Playback Timing when External Commands are Used – Microcomputer Interface Mode with Parallel Input

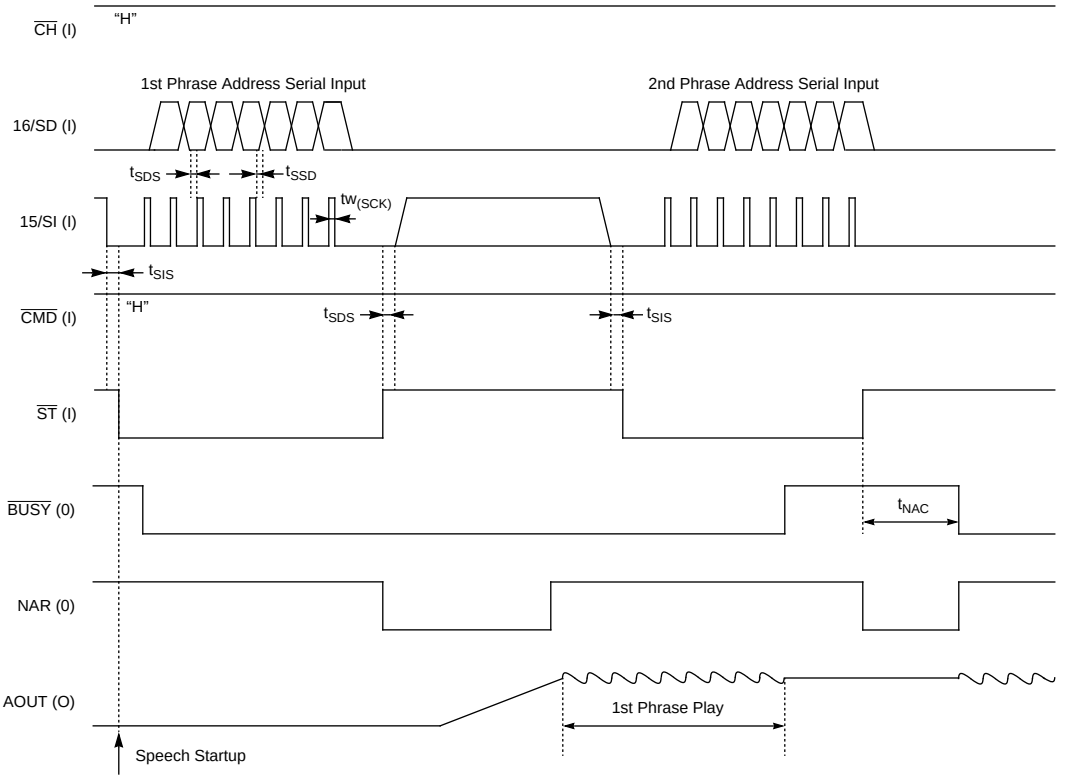

Figure 19. Playback Timing without Using External Command – Microcomputer Interface Mode with Serial Input

During serial input, data is transferred to the IC with the rising of the $\overline{ST}$ input after the input of the serial data.

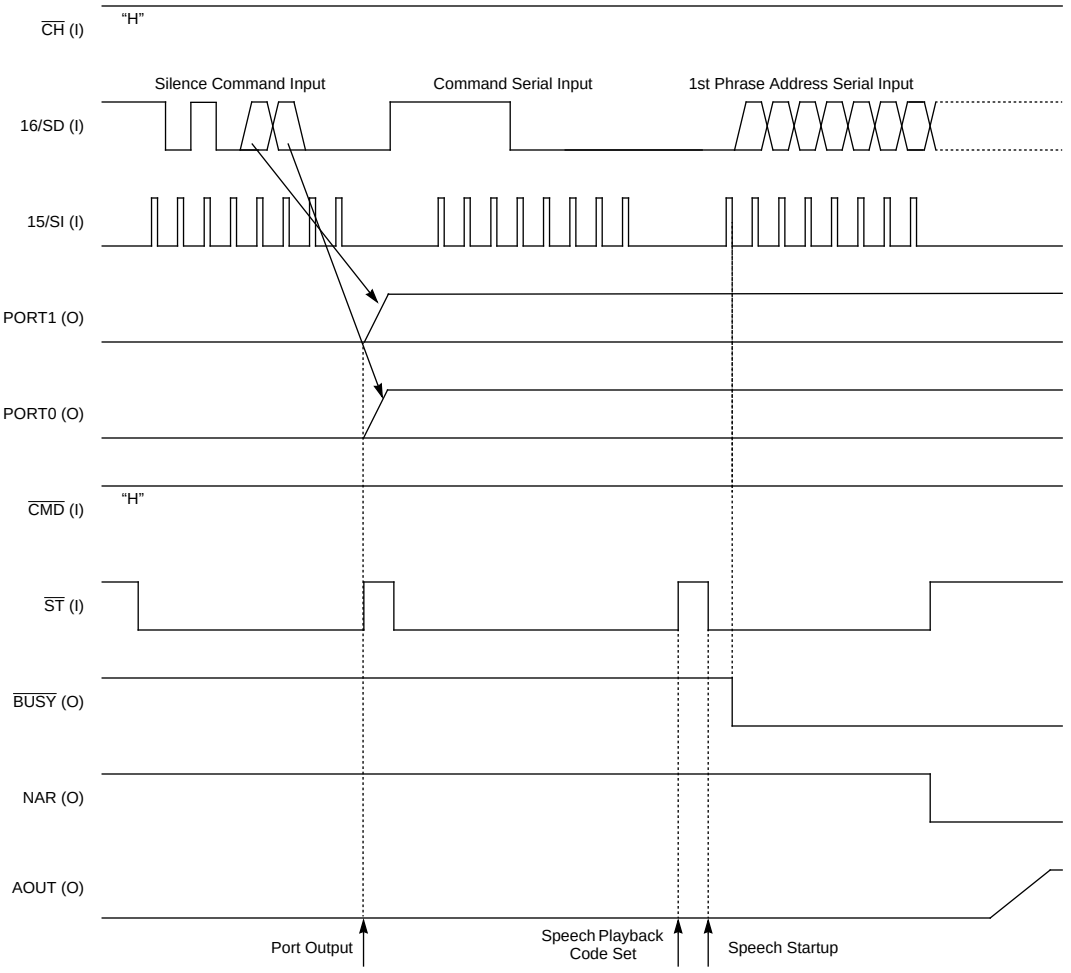

Figure 20. Playback Timing using External Command – Microcomputer Interface Mode with Serial Input