OKI Semiconductor

This version: Jan. 1998
Previous version: Aug. 1996

MSM82C84A-2RS/GS/JS

CLOCK GENERATOR AND DRIVER

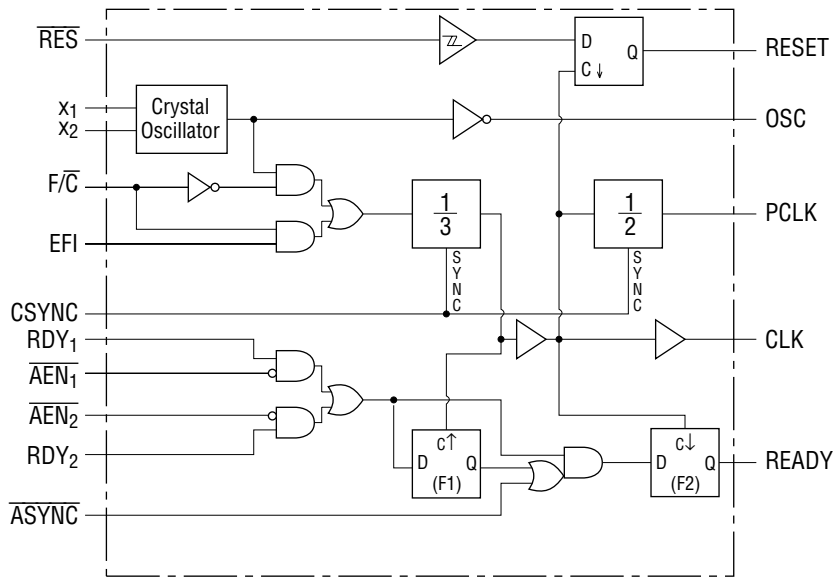
GENERAL DESCRIPTION

The MSM82C84A-2RS/GS is a clock generator designed to generate MSM80C86A-10 and MSM80C88A-10 system clocks of 8MHz.
Due to the use of silicon gate CMOS technology, standby current is only 40 µA (MAX.), and the power consumption is very low with 16 mA (MAX.) when a 8 MHz clock is generated.

FEATURES

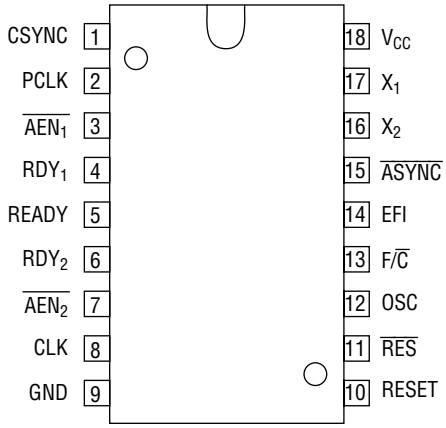
- Operating frequency of 6 to 24 MHz (CLK output 2 to 8 MHz)
- 3 µ silicon gate CMOS technology for low power consumption
- Built-in crystal oscillator circuit
- 3 V to 6 V single power supply
- Built-in synchronized circuit for MSM80C86A-10 and MSM80C88A-10 READY and RESET
- TTL compatible
- Built-in Schmitt trigger circuit (RES input)
- 18-pin Plastic DIP (DIP18-P-300-2.54): (Product name: MSM82C84A-2RS)
- 20-pin Plastic QFJ (QFJ20-P-S350-1.27): (Product name: MSM82C84A-2JS)
- 24-pin Plastic SOP (SOP24-P-430-1.27-K): (Product name: MSM82C84A-2GS-K)

FUNCTIONAL BLOCK DIAGRAM

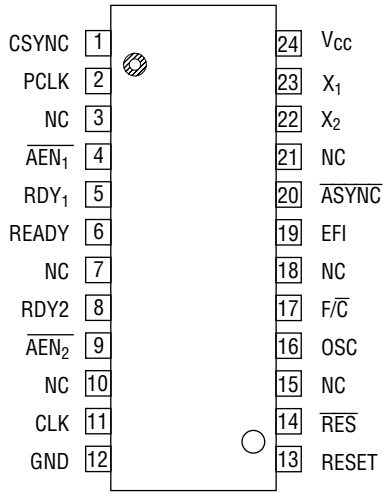


PIN CONFIGURATION (TOP VIEW)

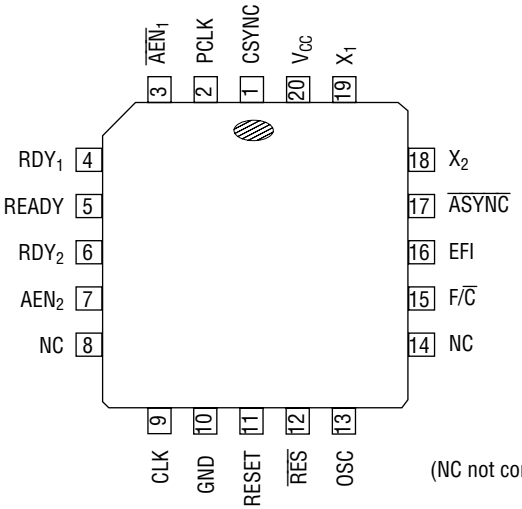
18 pin Plastic DIP



24 pin Plastic SOP



20 pin Plastic QFJ



(NC not connected)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			MSM82C84A-2RS/JS	MSM82C84A-2GS	
Supply Voltage	V_{CC}	Respect to GND	–0.5 to +7		V
Input Voltage	V_{IN}		–0.5 to V_{CC} +0.5		V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5		V
Storage Temperature	T_{STG}	—	–55 to +150		°C
Power Dissipation	P_D	Ta = 25°C	0.8	0.7	W

OPERATING RANGES

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{op}	–40 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{op}	–40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	–0.5	—	+0.8	V
"H" Level Input Voltage (except $\overline{RES}$)	V_{IH}	2.2	—	V_{CC} +0.5	V
"H" Level Input Voltage ($\overline{RES}$)		0.6*V_{CC}			

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"L" Level Output Voltage (CLK)	V_{OL}	I_{OL} = 4 mA	—	0.4	V
"L" Level Output Voltage (Others)	V_{OL}	I_{OL} = 2.5 mA	—	0.4	V
"H" Output Voltage (CLK)	V_{OH}	I_{OH} = –4 mA	V_{CC} –0.4	—	V
"H" Output Voltage (Others)	V_{OH}	I_{OH} = –1 mA	V_{CC} –0.4	—	V
$\overline{RES}$ Input Hysteresis	V_{IHR} -V_{ILR}		0.2*V_{CC}	—	V
Input Leak Current (Except $\overline{ASYNC}$)	I_{LI}	$0 \le V_{IN} \le V_{CC}$	–1	+1	µA
Input Current ($\overline{ASYNC}$)	I_{LIA}	$0 \le V_{IN} \le V_{CC}$	–100	+10	µA
Standby Supply Current	I_{CCS}	Note 1	—	40	µA
Operating Supply Current	I_{CC}	f = 24 MHz, C_L= O $_P$F	—	16	mA
Input Capacitance	C_{IN}	f =1 MHz	—	7	pF

Note: 1. X1 ≥ V_{CC} – 0.2 V, X2 ≤ 0.2 V
F/C ≥ V_{CC} – 0.2 V, ASYNC = V_{CC} or open
VIH ≥ V_{CC} – 0.2 V, VIL ≤ 0.2 V

AC CHARACTERISTICS

(1)

(V_{CC} = 5 V ± 10%, Ta = –40 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Conditions	
EFI "H" Pulse Width	t_{EHEL}	13	—	ns	90% to 90%	
EFI "L" Pulse Width	t_{ELEH}	17	—	ns	10% to 10%	
EFI Cycle Time	t_{ELEL}	36	—	ns	—	
Crystal Oscillator Frequency	—	6	24	MHz	—	
Set up Time of RDY $_1$ or RDY $_2$ to CLK Falling Edge (Active)	t_{R1VCL}	35	—	ns	$\overline{\text{ASYNC}}$ = High	
Set up Time of RDY $_1$ or RDY $_2$ to CLK Rising Edge (Active)	t_{R1VCH}	35	—	ns	$\overline{\text{ASYNC}}$ = Low	
Set up Time of RDY $_1$ or RDY $_2$ to CLK Falling Edge (Inactive)	t_{R1VCL}	35	—	ns	—	
Hold Time of RDY $_1$ or RDY $_2$ to CLK Falling Edge	t_{CLR1X}	0	—	ns	—	Output Load Capacitance CLK output C_L = 100 pF Others 30 pF
Set up Time of $\overline{\text{ASYNC}}$ to CLK Falling Edge	t_{AYVCL}	50	—	ns	—	
Hold Time of $\overline{\text{ASYNC}}$ to CLK Falling Edge	t_{CLAYX}	0	—	ns	—	
Set up Time of $\overline{\text{AEN}}_1$ ($\overline{\text{AEN}}_2$) to RDY $_1$ (RDY $_2$) Rising Edge	t_{A1R1V}	15	—	ns	—	
Hold Time of $\overline{\text{AEN}}_1$ ($\overline{\text{AEN}}_2$) to CLK Falling Edge	t_{CLA1X}	0	—	ns	—	
Set up Time of CSYNC to EFI Rising Edge	t_{YHEH}	20	—	ns	—	
Hold Time of CSYNC to EFI Rising Edge	t_{EHYL}	10	—	ns	—	
CSYNC Pulse Width	t_{YHYL}	$2 \times t_{ELEL}$	—	ns	—	
Set up Time of $\overline{\text{RES}}$ to CLK Falling Edge	t_{I1HCL}	65	—	ns	—	
Hold Time of $\overline{\text{RES}}$ to CLK Falling Edge	t_{CLI1H}	20	—	ns	—	
Input Rising Edge Time	t_{ILIH}	—	15	ns	—	
Input Falling Edge Time	t_{IHIL}	—	15	ns	—	

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5 V and V_H = 1.5 V for both inputs and outputs.

AC CHARACTERISTICS

(2)

(V_{CC} = 5 V ± 10%, Ta = -40 to 85°C)

Parameter	Symbol	Conditions		Min.	Max.	Unit
CLK Cycle Time	t_{CLCL}	—		125	—	ns
CLK "H" Pulse Width	t_{CHCL}	—		$\frac{1}{3}$ T_{CLCL} + 2	—	ns
CLK "L" Pulse Width	t_{CLCH}	—		$\frac{2}{3}$ T_{CLCL} –15	—	ns
CLK Rising and Falling Edge Times	t_{CH1CH2} t_{CL2CL1}	1.0 V to 3.5 V		—	10	ns
PCLK "H" Pulse Width	t_{PHPL}	—		T_{CLCL} –20	—	ns
PCLK "L" Pulse Width	t_{PLPH}	—		T_{CLCL} –20	—	
Time from READY Falling Edge to CLK Falling Edge	t_{RYLCL}	—		-8	—	ns
Time from READY Rising Edge to CLK Rising Edge	t_{RYHCH}	—	Output Load Capacitance	$\frac{2}{3}$ T_{CLCL} –15	—	ns
Delay from CLK Falling Edge to RESET Falling Edge	t_{CLIL}	—	CLK Output C_L = 100 pF Others 30 pF	—	40	ns
Delay from CLK Falling Edge to PCLK Rising Edge	t_{CLPH}	—		—	22	ns
Delay from CLK Falling Edge to PCLK Falling Edge	t_{CLPL}	—		—	22	ns
Delay from OSC Falling Edge to CLK Rising Edge	t_{OLCH}	—		–5	22	ns
Delay from OSC Falling Edge to CLK Falling Edge	t_{OLCL}	—		2	35	ns
Output Rising Edge Time (Except CLK)	t_{OLOH}	0.8 V to 2.2 V		—	15	ns
Output Falling Edge Time (Except CLK)	t_{OHOL}	2.2 V to 0.8 V		—	15	ns

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5 V and V_H = 1.5 V for both inputs and outputs.

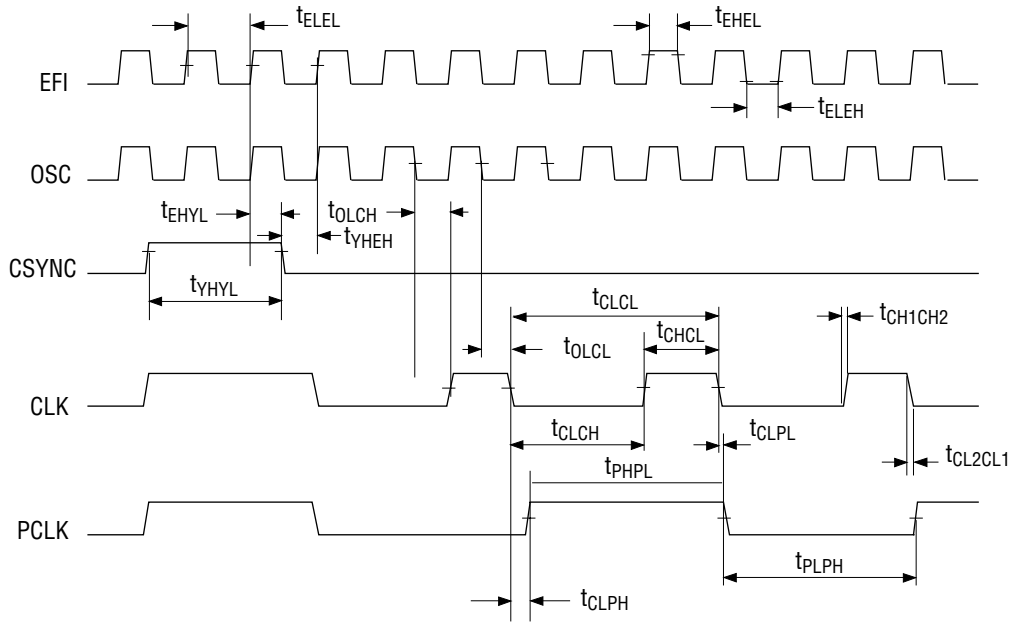
PIN DESCRIPTION

Pin Symbol	Name	Input/Output	Function
CSYNC	Clock Synchronization Single	Input	Synchronizing signal for output of in-phase CLK signals when more than one MSM82C84A-2 is used. The internal counter is reset when this signal is at high level, and a high level CLK output is generated. The internal counter is subsequently activated and a 33% duty CLK output is generated when this signal is switched to low level. When this signal is used, external synchronization of EFI is necessary. When the internal oscillator is used, it is necessary for this pin to be kept to be low level.
PCLK	Peripheral Clock Output	Output	This peripheral circuit clock signal is output in a 50% duty cycle at a frequency half that of the clock signal.
$\overline{AEN_1}$ $\overline{AEN_2}$	Address Enable Signals	Input	The $\overline{AEN_1}$ signal enables $\overline{RDY_1}$, and the $\overline{AEN_2}$ signal RDY_2. The respective RDY inputs are activated when the level applied to these pins is low. Although two separate inputs are used in multi-master systems, only the $\overline{AEN}$ which enables the RDY input to be used is to be switched to low level in the case of not using multi-master systems.
RDY_1 RDY_2	Bus Ready Signals	Input	Completion of data bus reading and writing by the device connected to the system data bus is indicated when one of these signals is switched to high level. The relevant RDY input is enables only when the corresponding $\overline{AEN}$ is at low level.
READY	Ready Output	Output	This signal is obtained by synchronizing the bus ready signal with CLK. This signal is output after guaranteeing the hold time for the CPU in phase with the RDY input.
CLK	Clock Output	Output	This signal is the clock used by the CPU and peripheral devices connected to the CPU system data bus. The output waveform is generated in a 33% duty cycle at a frequency 1/3 the oscillating frequency of the crystal oscillator connected to the X_1 and X_2 pins, or at a frequency 1/3 the EFI input frequency.
$\overline{RES}$	Reset in	Input	This low-level active input is used to generate a CPU reset signal. Since a Schmitt trigger is included in the input circuit for this signal, "power on resetting" can be achieved by connection of a simple RC circuit.
RESET	Reset Output	Output	This signal is obtained by CLK synchronization of the input signal applied to $\overline{RES}$ and is output in opposite phase to the $\overline{RES}$ input. This signal is applied to the CPU as the system reset signal.
F/C	Clock Select Signal	Input	This signal selects the fundamental signal for generation of the CLK signal. The CLK is generated from the crystal oscillator output when this signal is at low level, and from the EFI input signal when at high level.
EFI	External Clock Signal	Input	The signal applied to this input pin generaters the CLK signal when F/$\overline{C}$ is at high level. The frequency of the input signal needs to be three times greater than the desired CLK frequency.
X_1, X_2	Crystal Oscillator Connecting Pins	Input	Crystal oscillator connections. The crystal oscillator frequency needs to be three times greater than the desired CLK frequency.
OSC	Crystal Resonator Output	Output	Crystal oscillator output. This output frequency is the same as the oscillating frequency of the oscillator connected to the X_1 and X_2 pins. As long as a Xtal oscillator is connected to the X_1 and X_2 pins, this output signal can be obtained independently even if F/$\overline{C}$ is set to high level to enable the EFI input to be used CLK generation purpose.

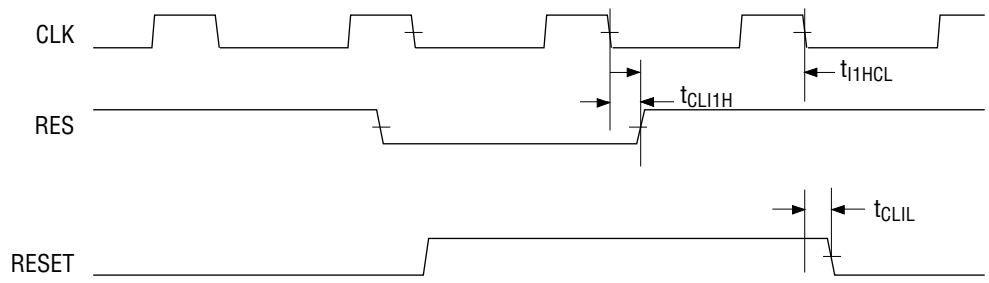
Pin Symbol	Name	Input/Output	Function
$\overline{\text{ASYNC}}$	Ready synchronization select signal	Input	Signal for selection of the synchronization mode of the READY signal generator circuit. When this signal is at low level, the READY signal is generated by double synchronization. And when at high level, the READY signal is generated by single synchronization. This pin is equipped with internal pull-up resistor.
V_{CC}	—	—	+5 V power supply
GND	—	—	GND

TIMING DIAGRAM

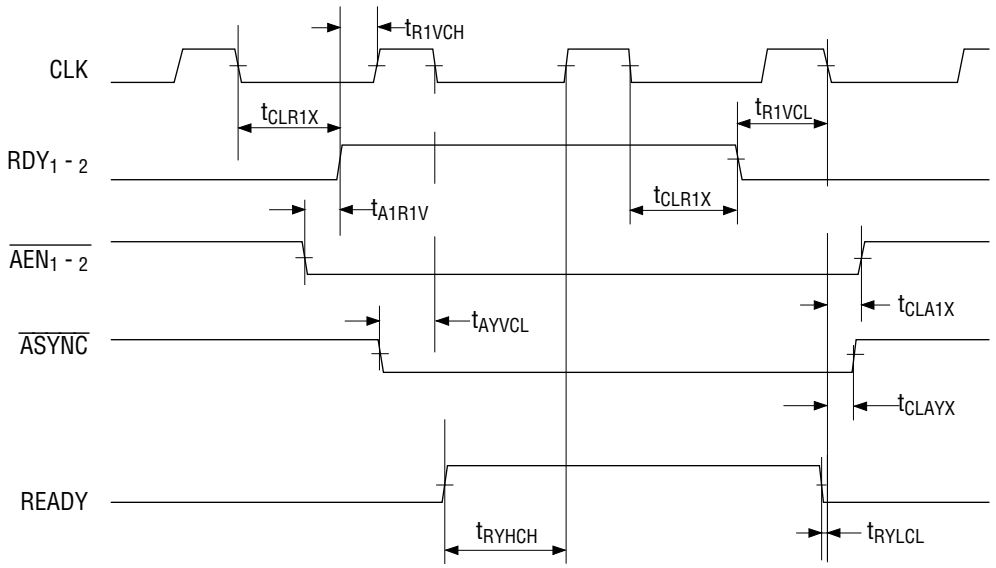
CLK • PCLK • OSC Waveforms



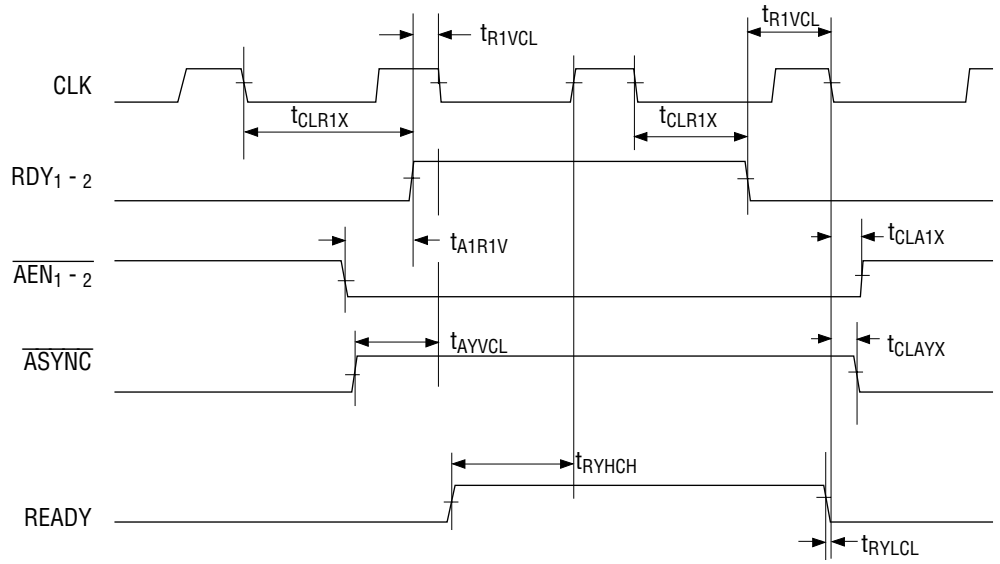
RESET Waveform



READY Waveform ($\overline{\text{ASYNC}}$ = L)



READY Waveform ($\overline{\text{ASYNC}}$ = H)

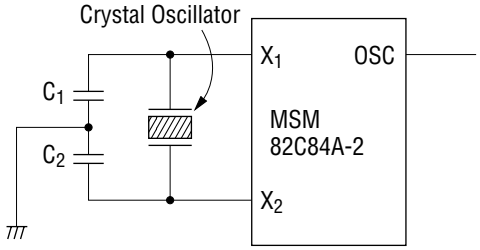


OPERATIONAL DESCRIPTION

(1) Oscillator Circuit

The MSM82C84A-2 internal oscillator circuit can be driven by connecting a crystal oscillator to the X_1 and X_2 pins.
The frequency of the crystal oscillator in this case needs to be three times greater than the desired CLK frequency.
Since the oscillator circuit output (the same output as for the crystal resonator frequency) appears at the OSC pin, independent use of this output is also possible.

Oscillator Circuit Example



When input frequency is 6 to 15 MHz
$C_1 = C_2 = 33$ pF
When input frequency is 15 to 24 MHz
$C_1 = C_2 = 10$ pF

Note: Because Oscillator circuit and values depend on crystal oscillator characteristics, OKI recommends to make contact with crystal oscillator vendor to determine the best circuit and values for customers' application.

(2) Clock Generator Circuit

This circuit generates two clock outputs-CLK obtained by dividing the input external clock or crystal oscillator circuit output by three, and PCLK obtained by halving CLK. CLK and PCLK are generated from the external clock applied to the EFI pin when F/$\overline{C}$ is at high level, and are generated from the crystal oscillator circuit when at low level.

(3) Reset Circuit

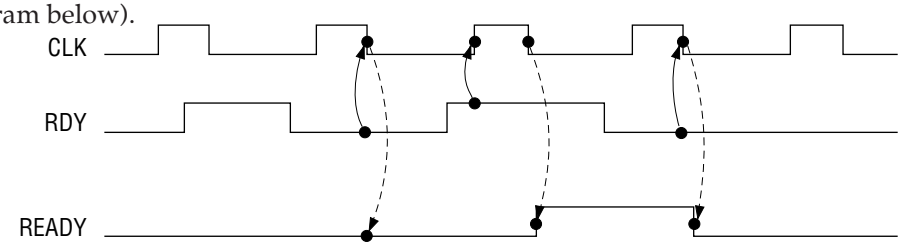
Since a Schmitt trigger circuit is used in the $\overline{RES}$ input, the MSM82C84A-2 can be reset by "power on" by connection to a simple RC circuit. If the MSM80C86A-10 or MSM80C88A-10 is used as the CPU in this case, it is necessary to keep the $\overline{RES}$ input at low level for at least 50 ms after Vcc reaches the 4.5V level.

(4) Ready Circuit

The READY signal generator circuit can be set to synchronization mode by $\overline{\text{ASYNC}}$.

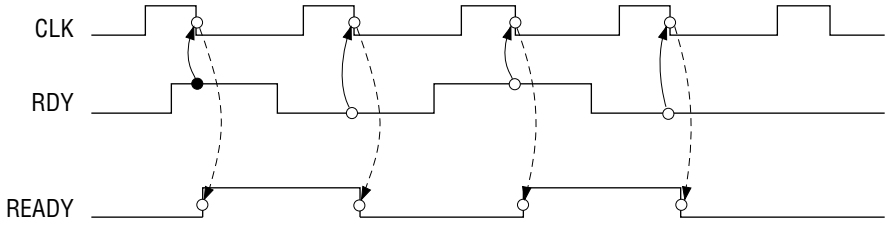
(i) When $\overline{\text{ASYNC}}$ is at low level
The RDY input is output as the READY signal by double synchronization.
The high-level RDY input is synchronized once by the rising edge of the CLK of the first stage flip-flop (F1 in the circuit diagram), and then synchronized again by the falling edge of the CLK of the next stage flip-flop (F2 in the circuit diagram), resulting in output of a high-level READY output signal (see diagram below).

The low-level RDY input is synchronized directly by the falling-edge of the CLK of the next stage flip-flop, resulting in output of a low-level READY output signal (see diagram below).



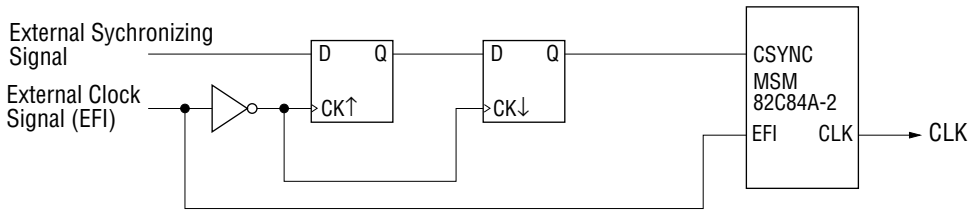
(ii) When $\overline{\text{ASYNC}}$ is at high level
The RDY input is output as the READY signal by single synchronization.

Both low-level and high-level RDY inputs are synchronized by the falling edge of the CLK of the next stage flip-flop, resulting output of respective low-level and high-level READY output signals (see diagram below).

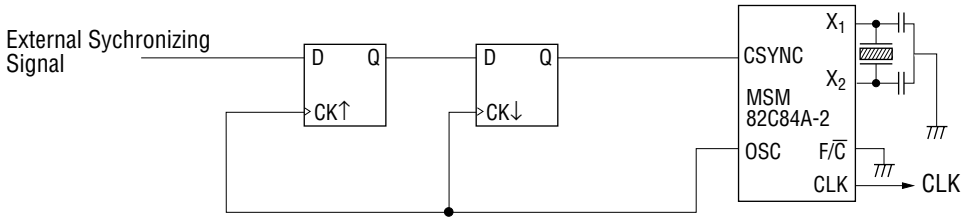


EXAMPLE OF USE (CSYNC)

The MSM82C84A-2 1/3 frequency divider counter is unsettled when the power is switched on. Therefore, the CSYNC pin has been included to synchronize CLK with another signal. When CSYNC is at high level, both CLK and PCLK are high-level outputs. If CSYNC is then switched to low level, CLK is output from the next input clock rising edge, and is divided by 3.
If CSYNC has not been synchronized with the input clock, use the following circuit to achieve the required synchronization



When an external clock EFI is used as the clock source



When the crystal oscillator is used as the clock source

NOTES ON USE

The MSM82C84A-2 cannot be used if the MSM80C86A-10 or MSM80C88A-10 is used within the range of 8 MHz < operating frequency ≤ 10 MHz.

NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below.
When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8bit MPU
M80C86A-10	M80C86A/M80C86A-2	16bit MPU
M80C88A-10	M80C88A/M80C88A-2	8bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM.I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI

Differences between MSM82C84A and MSM82C84A-5/MSM82C84A-2

1) Manufacturing Process

All these devices use a 3 μ Si-Gate CMOS process technology.
The chip size of these devices is same.
The chip of the MSM82C84A-5 is entirely identical to that of the MSM82C84A-2.

2) Functions

Item	MSM82C84A	MSM82C84A-5/-2
Internal processing of $\overline{\text{ASYNC}}$ pin	Normal CMOS input pin	Input pin with built-in pull up resistor
Notes on use	The pin should have a pullup or pulldown resistor if it is unused.	The value of pulldown resistor (when used) is limited. (See page 3.)

3) Electrical Characteristics

3-1) DC Characteristics

Parameter	Symbol	MSM82C84A	MSM82C84A-5/-2
''L''Level Output Voltage (CLK)	V_{OL}	0.45 V maximum (+5 mA)	0.40 V maximum (+4 mA)
''L''Level Output Voltage (Other than CLK)	V_{OL}	0.45 V maximum (+5 mA)	0.40 V maximum (+2.5 mA)
''H''Level Output Voltage (CLK)	V_{OH}	3.7 V minimum (-1 mA)	V_{CC}-0.1 V minimum (-4 mA)
''H''Level Output Voltage (Other than CLK)	V_{OH}	3.7 V minimum (-1 mA)	V_{CC}-0.1 V minimum (-1 mA)
$\overline{\text{RES}}$ Input Hysteresis Width	V_{IHR}-V_{ILR}	0.25 V minimum	0.2 × V_{CC} min
Input Current ($\overline{\text{ASYNC}}$)	I_{LIA}	-10 μA to +10 μA	-100 μA~+10 μA
Input Leak Current	I_{LI}	-10 μA to +10 μA	-1 μA~+1 μA
Supply Current (Standby)	I_{CCS}	100 μA maximum	40 μA maximum

As shown above, the MSM82C84A-5/MSM82C84A-2 satisfies the characteristics (except for V_{OL} and input current ($\overline{\text{ASYNC}}$) of the MSM82C84A.

3-2) AC Charasteristics

1) MSM82C84A and MSM82C84A-2

Parameter	Symbol	MSM82C84A	MSM82C84A-2
Input Rise Time	t_{ILIH}	20 ns maximum	15 ns maximum
Input Fall Time	t_{ILIH}	20 ns maximum	15 ns maximum
CLK High Time	t_{CHCL}	65 ns minimum	1/3 t_{CLCL} +2 ns minimum
CLK Low Time	t_{CLCH}	119 ns minimum	2/3 t_{CLCL} -15 ns minimum
CLK Rise/Fall Time	t_{CH1CH2} t_{CL1CL2}	15 ns maximum	10 ns maximum
PCLK High Time	t_{PHPL}	180 ns minimum	t_{CLCL} -20 ns minimum
PCLK Low Time	t_{PLPH}	180 ns minimum	t_{CLCL} -20 ns minimum
READY Falling to CLK Rising	t_{RYHCH}	114 ns minimum	2/3 t_{CLCL} -15 ns minimum

As shown above, the MSM82C84A-2 satisfies the characteristics (except for Input Rise/Fall Time) of the MSM82C84A.

1) MSM82C84A-5 and MSM82C84A-2

Parameter	Symbol	MSM82C84A-5	MSM82C84A-2
EFI High Time	t_{EHEL}	20 ns minimum	13 ns minimum
EFI Low Time	t_{ELEH}	20 ns minimum	17 ns minimum
EFI Period	t_{ELEL}	66 ns minimum	36 ns minimum
Crystal Frequency	—	15 MHz maximum	24 MHz maximum
CLK Period	t_{CHCL}	200 ns minimum	125 ns minimum

As shown above, the MSM82C84A-2 satisfies the characteristics of the MSM82C84A-5.

4) Notices on use

Note the following when replacing devices as the ASYNC pin is differently treated between the MSM82C84A and the MSM82C84A-5/MSM82C84A-2:

Case 1: When only a pullup resistor is externally connected to.
The MSM82C84A can be replaced by the MSM82C84A-2.

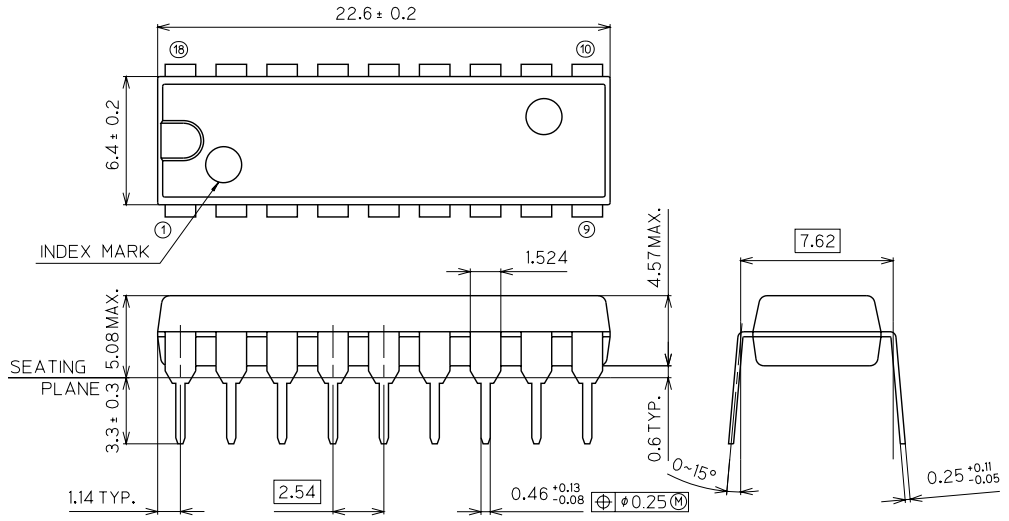
Case 2: When only pulldown resistor is externally connected to.
When the pulldown resistor is 8 kiloohms or less, the MSM82C84A can be replaced by the MSM82C84A-2.
When the pulldown resistor is greater than 8 kiloohms, use a pulldown resistor of 8 kiloohms or less.

Case 3: When an output of the other IC device is connected to the device.
The MSM82C84A can be replaced by the MSM82C84A-2 when the I_{OL} pin of the device to drive the $\overline{\text{ASYNC}}$ pin of the MSM82C84A-2 has an allowance of 100 μA or more.

PACKAGE DIMENSIONS

(Unit : mm)

DIP18-P-300-2.54



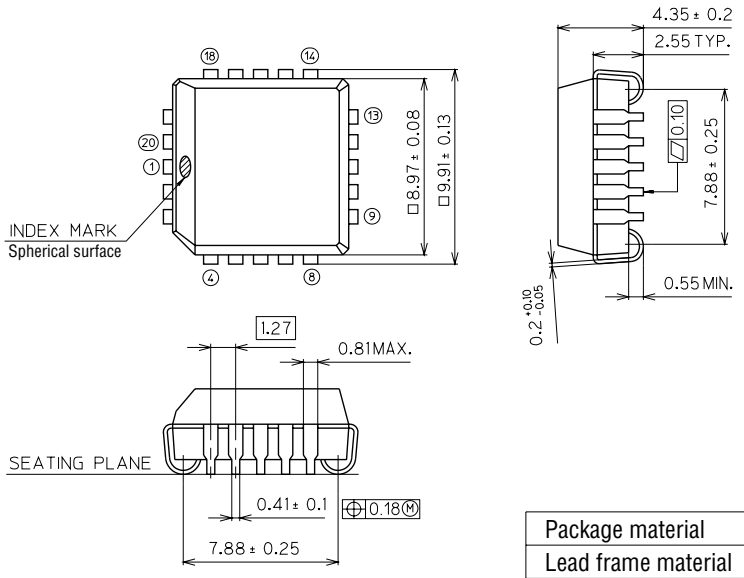
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.30 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ20-P-S350-1.27



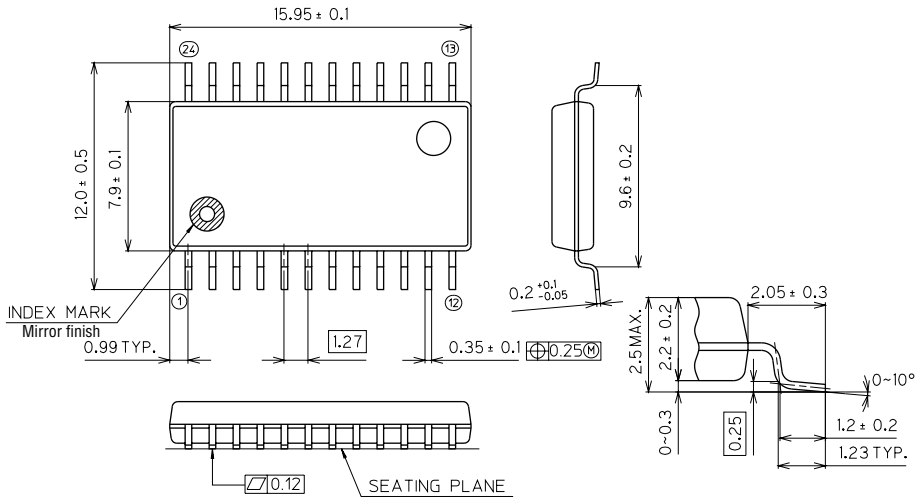
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.59 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).