

OKI Semiconductor

FEDL9810BFULL-03

Issue Date: Jun. 20, 2003

MSM9810B

8-Channel Mixing OKI ADPCM Type Voice Synthesis LSI

GENERAL DESCRIPTION

The MSM9810B is an 8-channel mixing voice synthesis LSI, to which up to 128 Mbits of ROM and/or EPROM storing voice data can directly be connected externally.

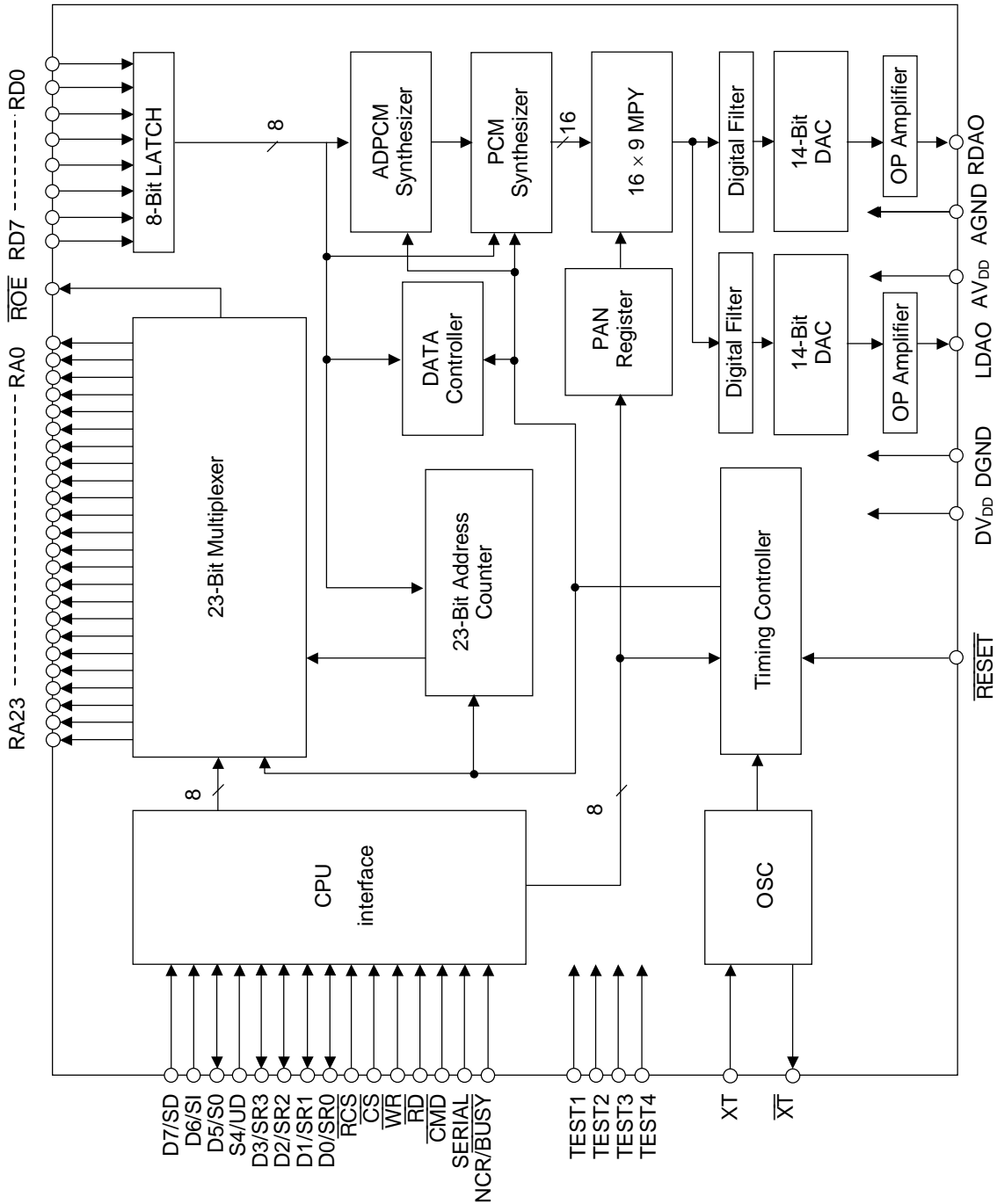
The device is straight 8-bit PCM playback, non-linear 8-bit PCM playback, 4-bit ADPCM playback, and 4-bit ADPCM2 playback selectable and provides 2-channel stereo output and volume control. The MSM9810B contains a 14-bit D/A converter and LPF.

The MSM9810B can easily configure a system by connecting voice data storage memory, power amplifier, and CPU externally.

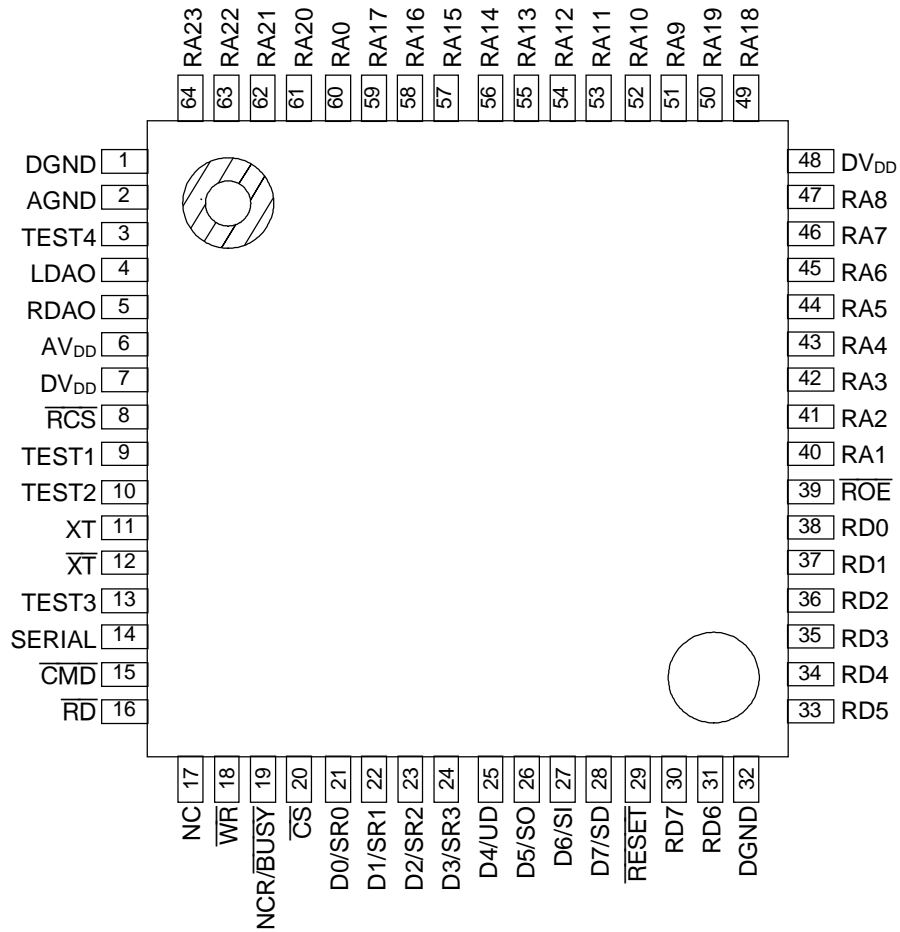
FEATURES

- Non-linear 8-bit PCM/straight 8-bit PCM/4-bit ADPCM/4-bit ADPCM2
 - Serial input or parallel input selectable
 - Phrase Control Table function
 - 8-channel mixing function
 - Master clock frequency : 4.096 MHz
 - Sampling frequency : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 21.2 kHz, 25.6 kHz, 32.0 kHz
 - Maximum number of phrases : 256
 - Output channel : L/R 2 channels
 - Built-in volume control function (for each output channel)
 - Built-in 14-bit D/A converter
 - Built-in low-pass filter : Digital filter
- 64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSM9810BGS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No connection

64-pin Plastic QFP

PIN DESCRIPTIONS

| Pin | Symbol | Type | Description |
|---------------|------------------|------|--|
| 40-47, 49-64 | RA23-RA0 | O | Address pins for external memory. These pins become high impedance when \overline{RCS} pin is "H". |
| 30, 31, 33-38 | RD7-RD0 | I | Data pin for external memory. Pull-down resistors are internally connected to these pins. These pull-down resistors become valid when the \overline{RCS} pin is "H", and become invalid when the \overline{RCS} pin is "L". |
| 39 | \overline{ROE} | O | Output enable pin for external memory. |
| 8 | \overline{RCS} | I | When this pin is "L", RA23 to RA0 and \overline{ROE} pins output address data and output enable signal. When this pin is "H", RA23 to RA0 and \overline{ROE} pins become high impedance. |
| 15 | \overline{CMD} | I | Select pin for Command data or Subcommand data for CPU interface. When this pin is "H", subcommand input is selected. When this pin is "L", command input is selected. A pull-up resistor is internally connected to this pin. |
| 16 | \overline{RD} | I | Read pin for CPU interface. A pull-up resistor is internally connected to this pin. |
| 18 | \overline{WR} | I | Write pin for CPU interface. A pull-up resistor is internally connected to this pin. |
| 20 | \overline{CS} | I | Chip select pin for CPU interface. When \overline{CS} is "H", $\overline{WR}/\overline{RD}$ signal is not entered in this LSI. A pull-up resistor is internally connected to this pin. |
| 14 | SERIAL | I | CPU input interface select pin. When SERIAL is "H", serial input interface is selected. When it is "L", parallel input interface is selected. |
| 28 | D7/SD | I/O | Data bus pin for CPU interface when parallel input interface is selected. When \overline{WR} is "L", this pin serves as data input pin. When \overline{RD} is "L", this pin serves as channel status data output pin. When serial input interface is selected, this pin serves as serial data input pin. |
| 27 | D6/SI | I/O | Data bus pin for CPU interface when parallel input interface is selected. When \overline{WR} is "L", this pin serves as data input pin. When \overline{RD} is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as serial clock input pin. |
| 26 | D5/SO | I/O | Data bus pin for CPU interface when parallel input interface is selected. When \overline{WR} is "L", this pin serves as data input pin. When \overline{RD} is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status serial output pin. |

| Pin | Symbol | Type | Description |
|-------|------------------------|------|--|
| 25 | D4/UD | I/O | Data bus pin for CPU interface when parallel input interface is selected. When \overline{WR} is "L", this pin serves as data input pin. When \overline{RD} is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status select pin. When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively. |
| 24 | D3/SR3 | I/O | Data bus pin for CPU interface when parallel input interface is selected. When \overline{WR} is "L", this pin serves as data input pin. When \overline{RD} is "L", this pin serves as channel status output pin. |
| 23 | D2/SR2 | | When serial input interface is selected, this pin serves as channel status output pin. |
| 22 | D1/SR1 | | When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. |
| 21 | D0/SR0 | | When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively. |
| 4 | LDAO | O | LEFT side analog output pin. |
| 5 | RDAO | O | RIGHT side analog output pin. |
| 11 | XT | I | Crystal or ceramic oscillator connection pin. A feedback resistor of about $1M\Omega$ is connected between XT and \overline{XT} . When external clocks are used, enter external clocks into this pin. |
| 12 | \overline{XT} | O | Crystal or ceramic oscillator connection pin. When external clocks are used, leave this pin open. |
| 29 | \overline{RESET} | I | When this pin is "L" level, the LSI is initialized. At that time, oscillation stops and D/A outputs go to GND level. A pull-up resistor is internally connected to this pin. |
| 19 | NCR/ \overline{BUSY} | I | Channel status select pin. When this pin is "H", NCR signal is output. When it is "L", \overline{BUSY} signal is output. |
| 9 | TEST1 | I | Pins for LSI testing. Apply "L" level to these pins. |
| 10 | TEST2 | | |
| 13 | TEST3 | | |
| 3 | TEST4 | | |
| 6 | AV _{DD} | — | Analog power supply pin. A bypass capacitor of 01 μ F or more should be connected between the AGND pin and the AV _{DD} pin. |
| 7, 48 | DV _{DD} | — | Digital power supply pin. A bypass capacitor of 0.1 μ F or more should be connected between the DGND pin and the DV _{DD} pin. |
| 2 | AGND | — | Analog GND pin. |
| 1, 32 | DGND | — | Digital GND pin. |

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------|-----------|--------------------------|------------------------|------------------|
| Power Supply Voltage | V_{DD} | $T_a = 25^\circ\text{C}$ | -0.3 to +7.0 | V |
| Input Voltage | V_{IN} | | -0.3 to $V_{DD} + 0.3$ | V |
| Storage Temperature | T_{STG} | — | -55 to +150 | $^\circ\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

| Parameter | Symbol | Condition | Range | | | Unit |
|------------------------|-----------|-----------|------------|-------|------|------------------|
| Power Supply Voltage | V_{DD} | — | 4.5 to 5.5 | | | V |
| Operating Temperature | T_{op} | — | -40 to +85 | | | $^\circ\text{C}$ |
| Master Clock Frequency | f_{osc} | — | Min. | Typ. | Max. | MHz |
| | | | 3.5 | 4.096 | 4.5 | |

ELECTRICAL CHARACTERISTICS**DC Characteristics**(DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, T_a = -40 to +85 $^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|-----------|--|----------------------|------|----------------------|---------------|
| High-level Input Voltage | V_{IH} | — | $0.84 \times V_{DD}$ | — | — | V |
| Low-level Input Voltage | V_{IL} | — | — | — | $0.16 \times V_{DD}$ | V |
| High-level Output Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | $V_{DD} - 0.4$ | — | — | V |
| Low-level Output Voltage | V_{OL} | $I_{OL} = 2 \text{ mA}$ | — | — | 0.4 | V |
| High-level Input Current 1 | I_{IH1} | $V_{IH} = V_{DD}$ | — | — | 10 | μA |
| High-level Input Current 2 (Note 1) | I_{IH2} | Applied to pins with internal pull-down resistor | 30 | — | 300 | μA |
| Low-level Input Current 1 | I_{IL1} | $V_{IL} = \text{GND}$ | -10 | — | — | μA |
| Low-level Input Current 2 (Note 2) | I_{IL2} | Applied to pins with internal pull-up resistor | -300 | — | -30 | μA |
| Output Leakage Current | I_{LO} | $0 \leq V_{OUT} \leq V_{DD}$ | -10 | — | +10 | μA |
| Operating Current | I_{DD} | $f_{osc} = 4 \text{ MHz}$, no load | — | 6 | 15 | mA |
| Standby Current | I_{DS} | $T_a = -40 \text{ to } +70^\circ\text{C}$ | — | — | 15 | μA |
| | | $T_a = +70 \text{ to } +85^\circ\text{C}$ | — | — | 50 | μA |

Notes 1: Applicable to RD7 to RD0 pins (when $\overline{RCS} = \text{"H"}$).2: Applicable to \overline{CMD} , RD, WR, and CS pins.

Analog Characteristics(DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = -40 to +85°C)

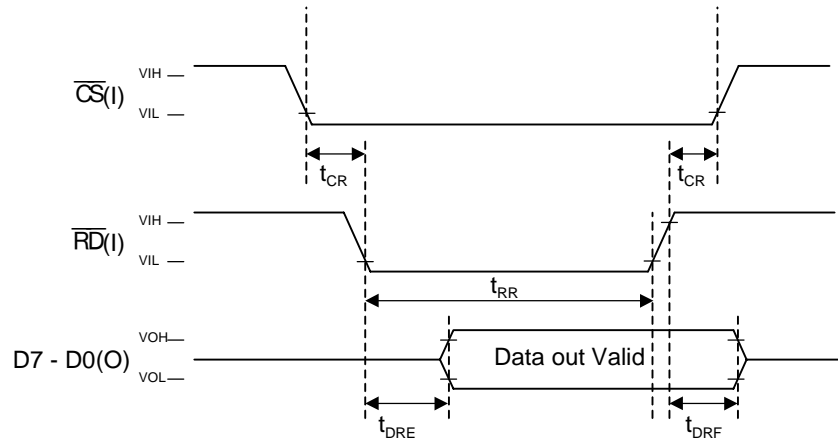
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|-------------------|-----------|------|-------------------------------|------|------|
| LDAO,RDAO Output Load (During OP amplifier output) | R _{OUTA} | — | 50 | — | — | kΩ |
| LDAO,RDAO Output Impedance (When OP amplifier is not used) | R _{OUTD} | — | — | 3 | — | kΩ |
| LDAO,RDAO Output Level | — | No load | — | 0.7 to 0.94 × V _{DD} | — | V |

AC Characteristics(V_{DD} = 4.5 to 5.5 V, GND = 0 V, Ta = -40 to +85°C, C_L = 5 pF)

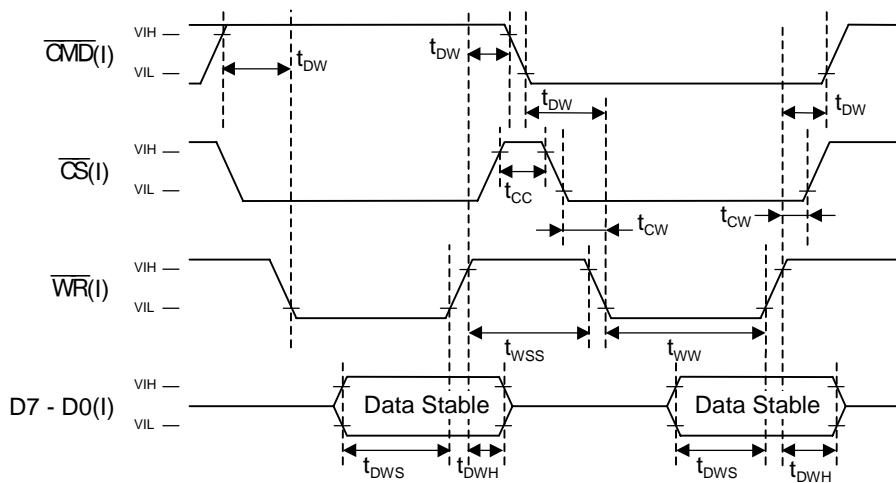
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---------------------|------|------|------|------|
| Master Clock Duty Cycle | f _{duty} | 40 | 50 | 60 | % |
| RESET Input Pulse Width | t _{w(RST)} | 1 | — | — | μs |
| RESET Input Time From Raising of Power Supply | t _{D(RST)} | 0 | — | — | μs |
| Set up and Hold Time of CS for RD | t _{CR} | 30 | — | — | ns |
| RD Pulse Width | t _{RR} | 200 | — | — | ns |
| Output Data Valid Time after Fall of RD | t _{DRE} | — | — | 100 | ns |
| Data Float Time after Rise of RD | t _{DRF} | — | 10 | 50 | ns |
| Setup and Hold Time of CMD for WR | t _{DW} | 50 | — | — | ns |
| Setup and Hold Time of CS for WR | t _{CW} | 30 | — | — | ns |
| WR Pulse Width | t _{WW} | 200 | — | — | ns |
| Data Setup Time before Rise of WR | t _{DWS} | 100 | — | — | ns |
| Data Hold Time after Rise of WR | t _{DWH} | 30 | — | — | ns |
| WR - WR Pulse Interval | t _{WWS} | 160 | — | — | ns |
| CS - CS Pulse Interval | t _{CC} | 100 | — | — | ns |
| Serial Data Setup Time | t _{SDS} | 30 | — | — | ns |
| Serial Data Hold Time | t _{SSD} | 30 | — | — | ns |
| Serial Clock Pulse Width | t _{w(SCK)} | 200 | — | — | ns |
| Output Data Valid Time after Rise of Serial Clock | t _{SDD} | — | — | 200 | ns |
| Setup Time of WR for Serial Data | t _{SWDS} | 200 | — | — | ns |
| Setup Time of Serial Clock Fall for WR Rise | t _{SIWS} | 300 | — | — | ns |
| Setup Time of RD for Serial Clock Rise | t _{SRIS} | 300 | — | — | ns |

TIMING DIAGRAMS (Parallel Input)

Data Read Timing

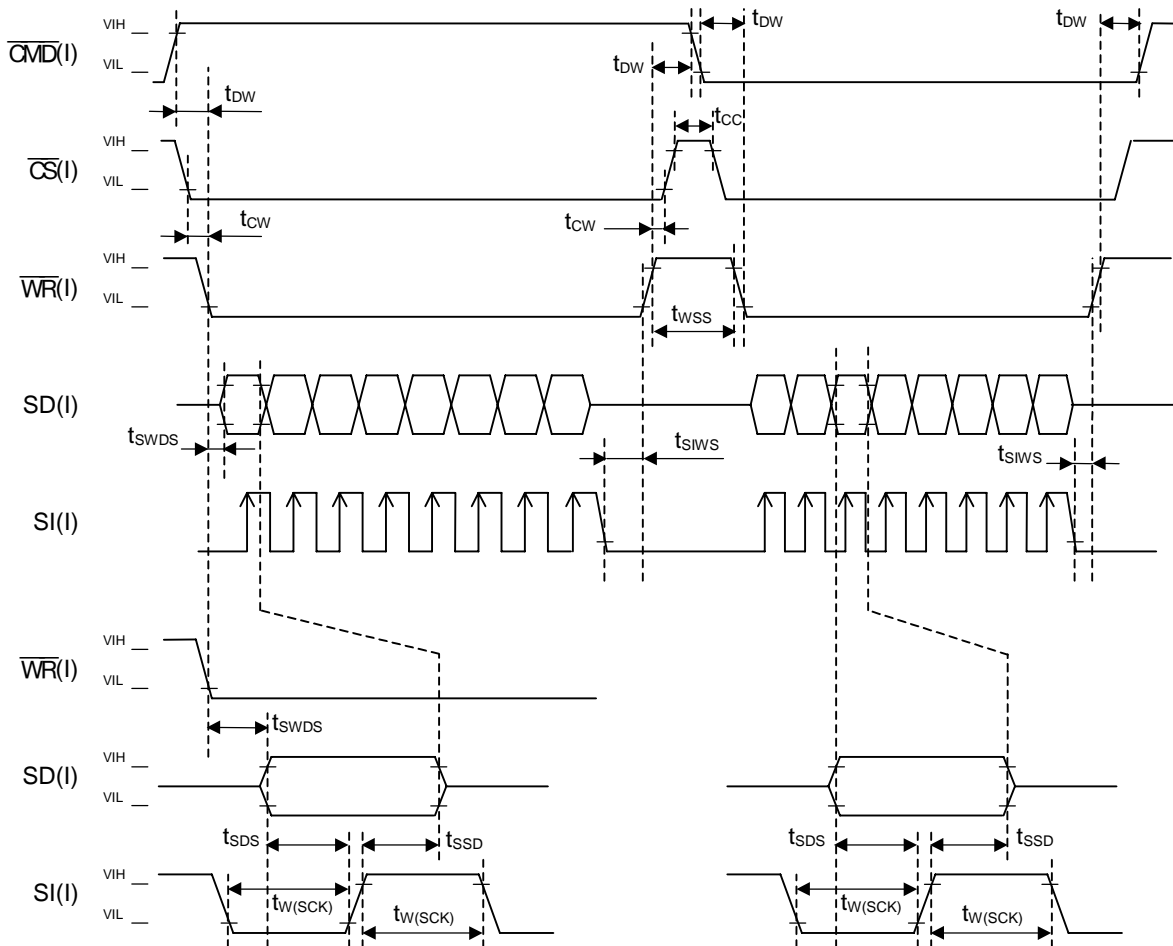


Data Write Timing (Sub-command, Command Input)

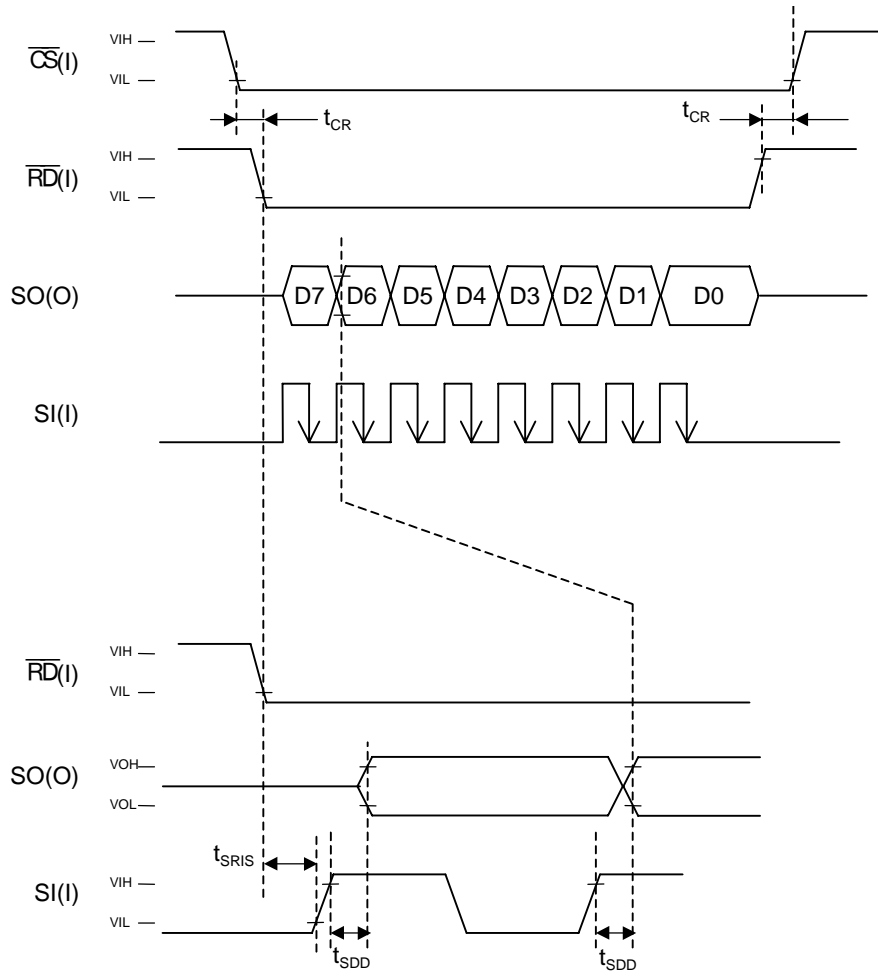


TIMING DIAGRAMS (Serial Input)

Data Write Timing (Sub-command, Command Input)

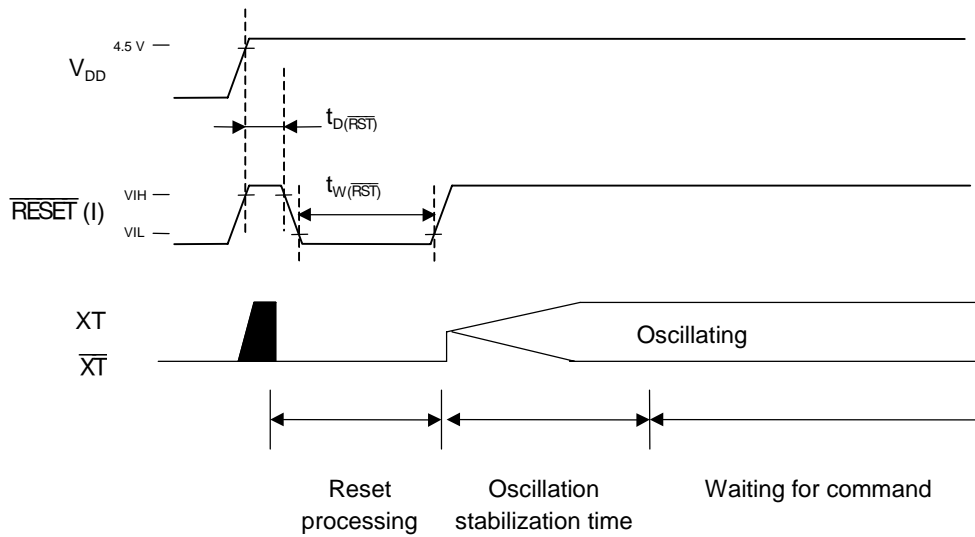


Data Read Timing

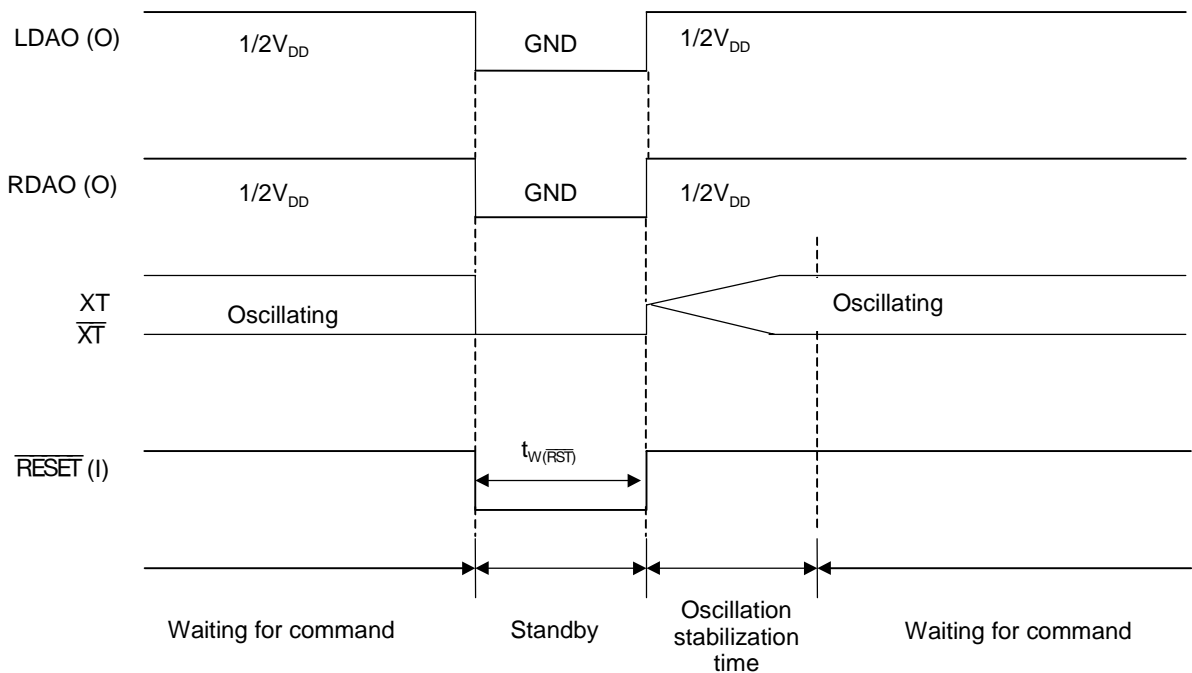


TIMING DIAGRAM (Common to Parallel and Serial I/O)

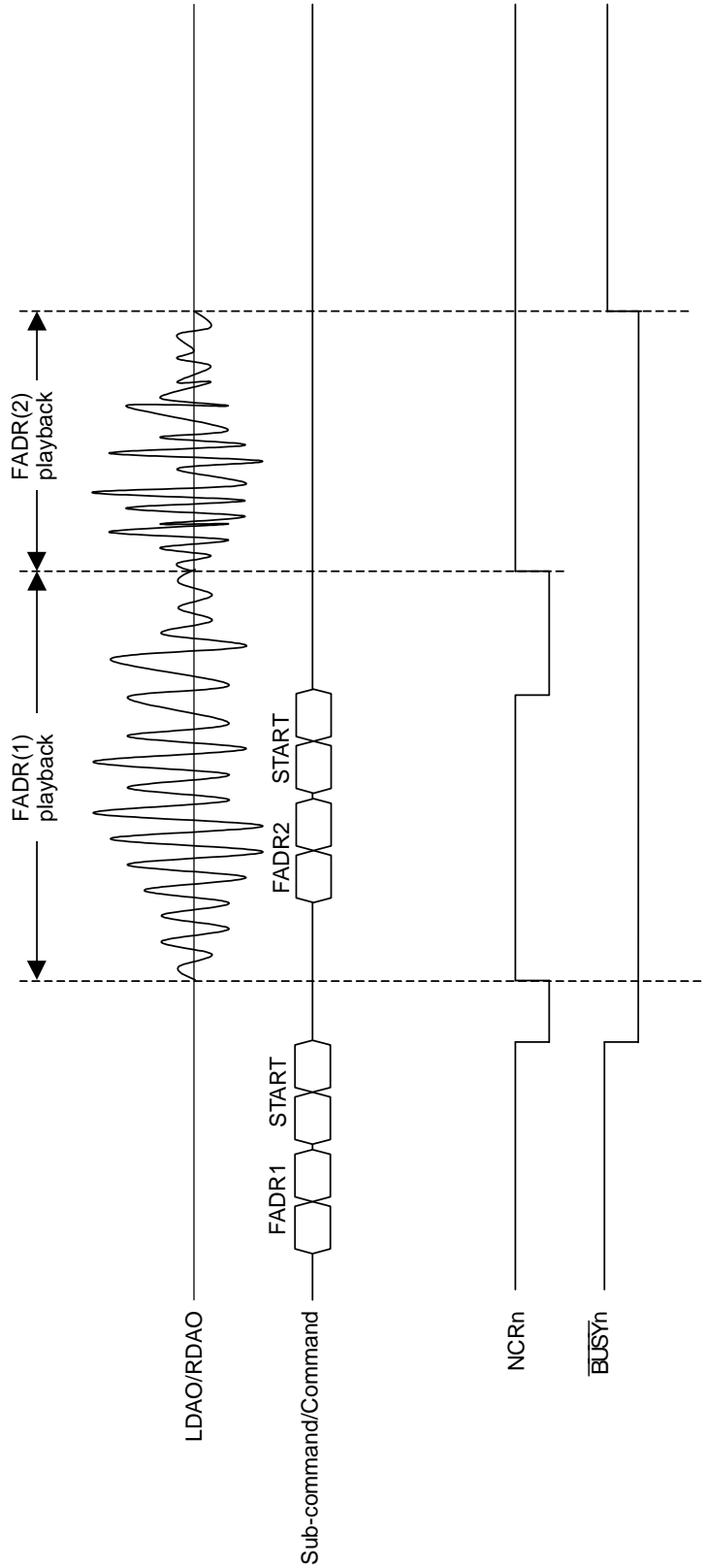
Power-on Timing · Power-down Timing



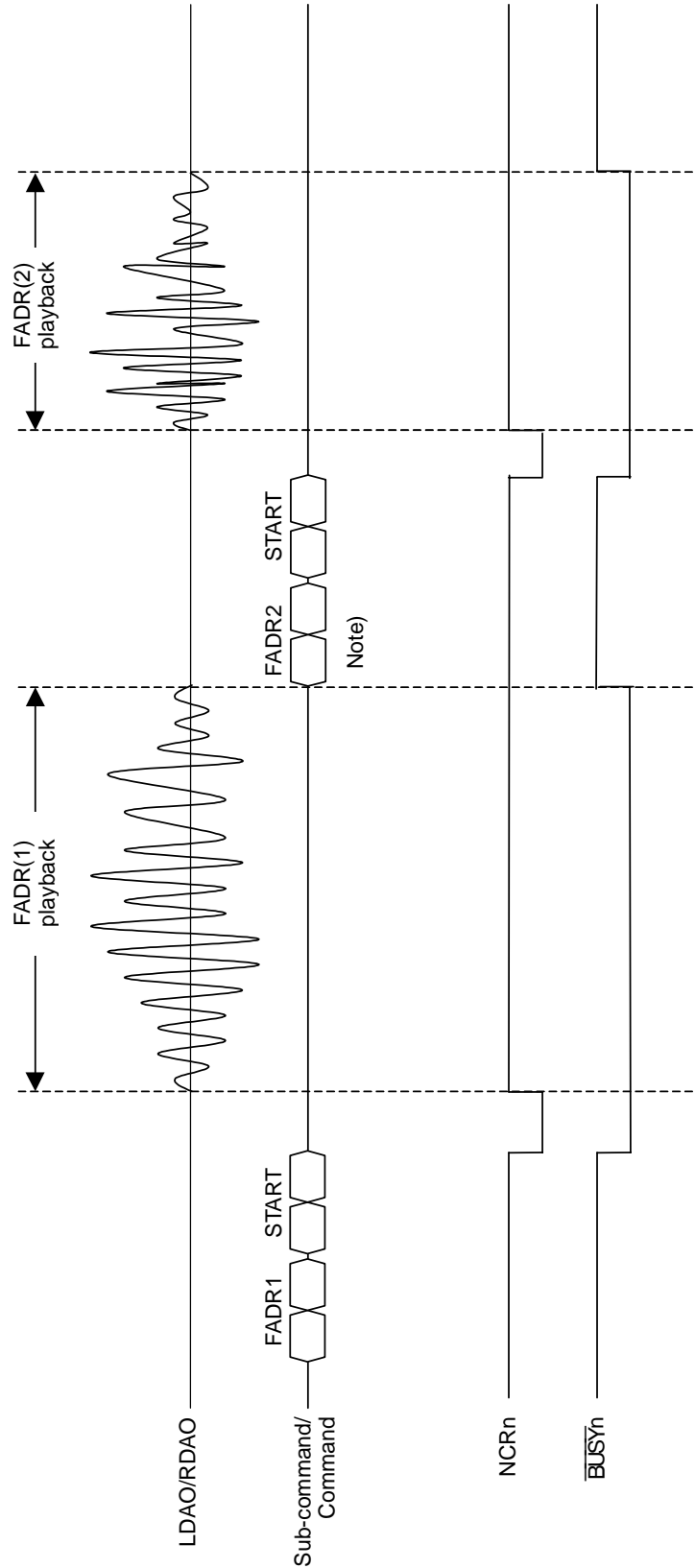
Standby



Continuous Playback Timing When Phrase Control Table is not Used

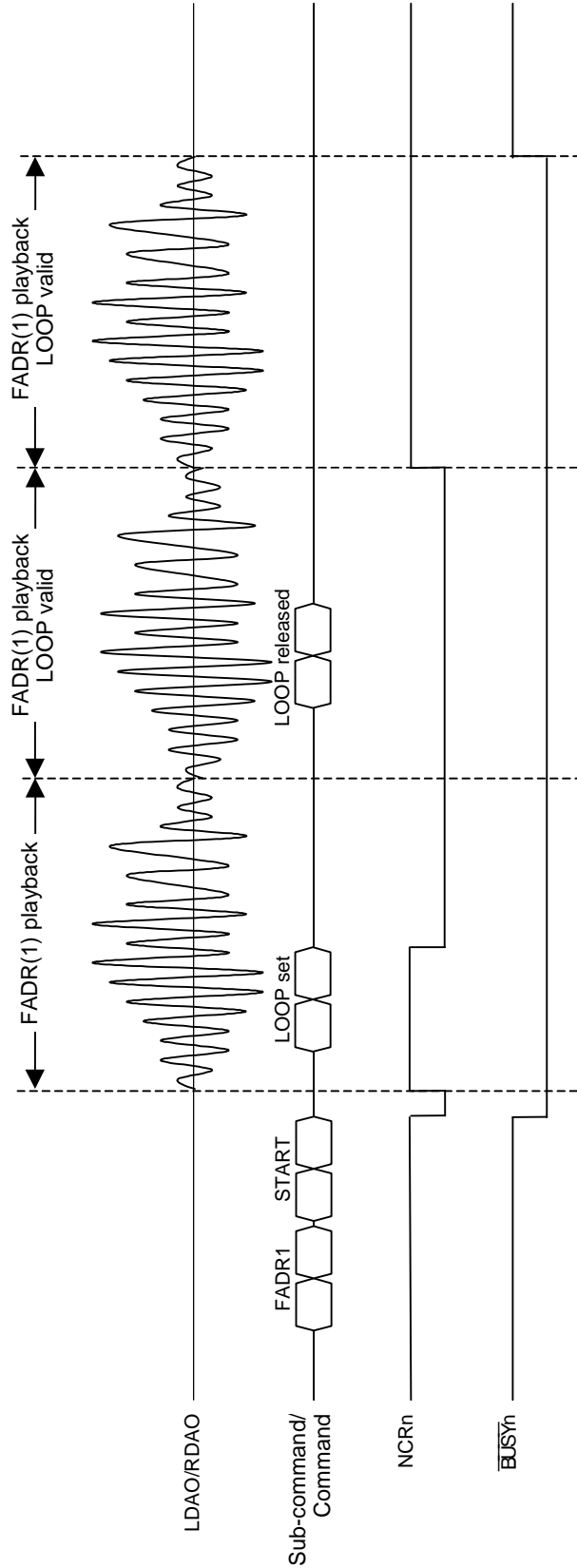


Continuous Playback Timing When Phrase Control Table is Used

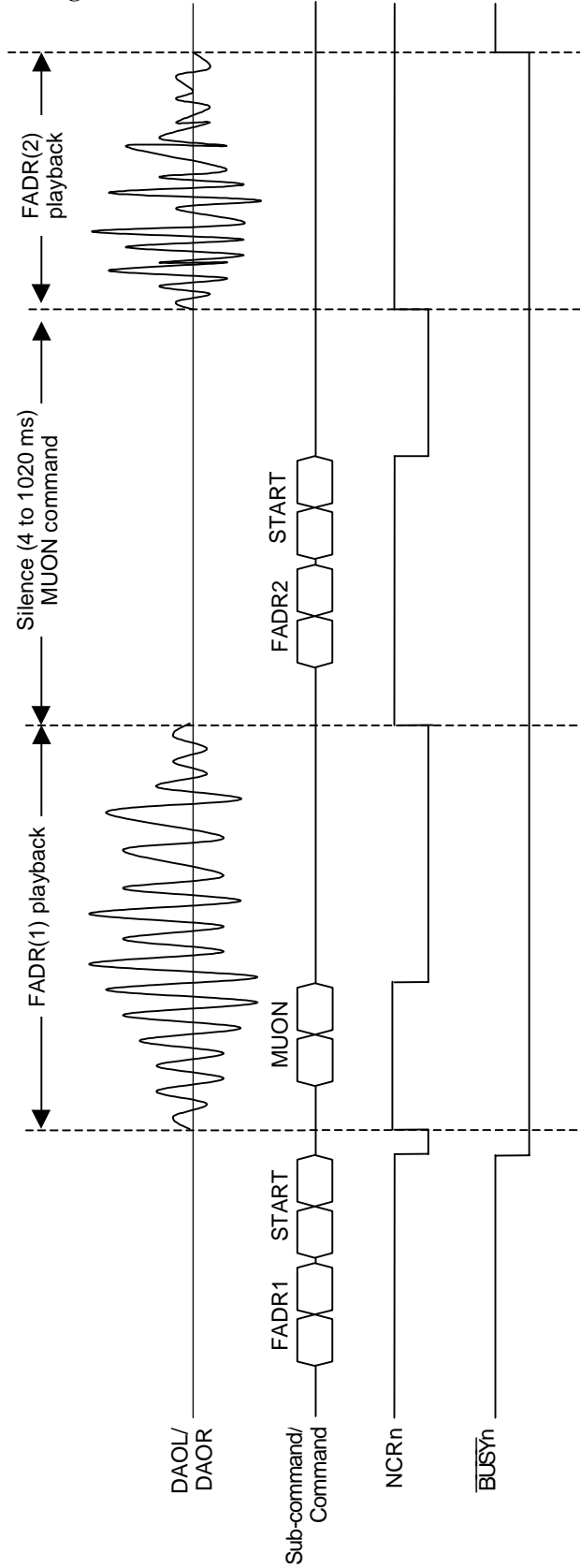


(Note)
 Do not enter the START command and MUON command during playback ($\overline{\text{BUSY}} = \text{"L"}$) when the phrase control table is used. Otherwise, the LSI may malfunction. Enter the START command and MUON command after $\overline{\text{BUSY}} = \text{"H"}$.

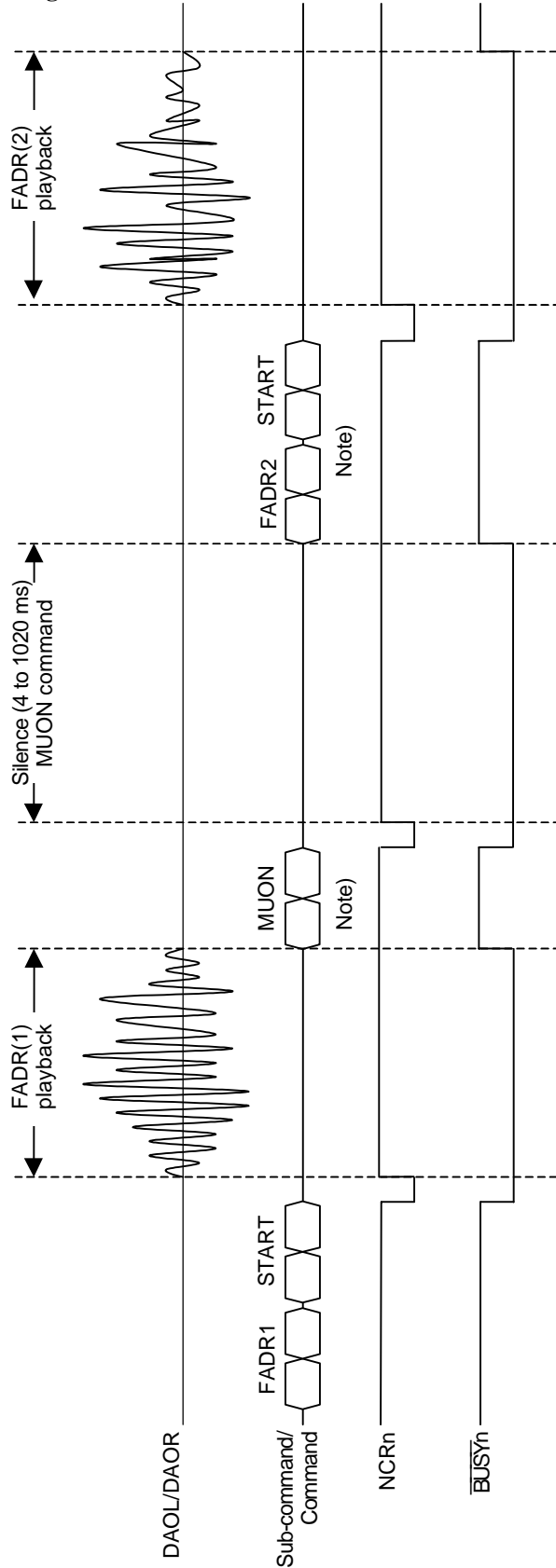
LOOP Playback Timing (Phrase Table is Used/not Used)



MUON Command Input Timing When Phrase Control Table is not Used



MUON Command Input Timing When Phrase Control Table is Used



(Note)
 Do not enter the START command and MUON command during playback ($\overline{\text{BUSY}} = \text{"L"}$) when the phrase control table is used. Otherwise, the LSI may malfunction. Enter the START command and MUON command after $\overline{\text{BUSY}} = \text{"H"}$.

FUNCTIONAL DESCRIPTION

Microcontroller Interface

The microcontroller interface includes two interface circuits, parallel interface and serial interface. The statuses of each pin both in parallel interface mode and in serial interface mode are shown below.

| SERIAL = "L" | | SERIAL = "H" | |
|------------------------|---------------|----------------------|--|
| Parallel I/O interface | | Serial I/O interface | |
| D7 (I/O) | Data I/O pins | SD (I) | Serial data input pin |
| D6 (I/O) | | SI (I) | Serial clock input pin |
| D5 (I/O) | | SO (O) | Serial data output pin |
| D4 (I/O) | | UD (I) | Select pin for channel statuses output via SR3 to SR0 |
| D3 (I/O) | | SR3 (O) | Channel 1 is output when UD is 0 and channel 5 when UD is 1. |
| D2 (I/O) | | SR2 (O) | Channel 2 is output when UD is 0 and channel 6 when UD is 1. |
| D1 (I/O) | | SR1 (O) | Channel 3 is output when UD is 0 and channel 7 when UD is 1. |
| D0 (I/O) | | SR0 (O) | Channel 4 is output when UD is 0 and channel 8 when UD is 1. |

Command List

Commands

Each command consists of a command and a sub-command.

The sub-command is input when the $\overline{\text{CMD}}$ pin is "H". The command is input when the $\overline{\text{CMD}}$ pin is "L".

| NCRn | Command name | $\overline{\text{CMD}}$ pin | D7 to D0 | | | | | | | | Description |
|-------------------|--------------|-----------------------------|--------------|---|---|----|----------|----------|------------|----|--|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Valid only at "H" | START | H | CH8 to CH1 | | | | | | | | Sets the bit of a voice synthesis start channel to "1". |
| | | L | 0 | 0 | 0 | 0 | 0 | X | X | X | Starts playback. |
| None | STOP | H | CH8 to CH1 | | | | | | | | Sets the bit of a voice synthesis end channel to "1". |
| | | L | 0 | 0 | 0 | 0 | 1 | X | X | X | Ends playback. |
| None | LOOP | H | CH8 to CH1 | | | | | | | | Sets the bit of a LOOP channel to "1". |
| | | L | 0 | 0 | 0 | 1 | 0 | X | X | X | Starts LOOP. |
| None | OPT | H | 0 | 0 | 0 | O4 | O3 | O2 | O1 | O0 | Selects an option. |
| | | L | 0 | 0 | 0 | 1 | 1 | X | X | X | |
| Valid only at "H" | MUON | H | M7 to M0 | | | | | | | | Selects a silence time at $M \times 4$ ms. (Condition: $1 \leq M \leq 255$) |
| | | L | 0 | 0 | 1 | 0 | 0 | C2 to C0 | | | Selects a channel that outputs a silence and plays a silence. |
| None | FADR | H | FA7 to FA0 | | | | | | | | Selects a phrase to be played. |
| | | L | 0 | 0 | 1 | 0 | 1 | C2 to C0 | | | Selects a channel that sets up a phrase. |
| None | DADR | H | SA23 to SA16 | | | | | | | | Selects a ROM address at which voice synthesis starts. |
| | | H | SA15 to SA8 | | | | | | | | |
| | | H | SA7 to SA0 | | | | | | | | |
| | | H | ST23 to ST16 | | | | | | | | Selects a ROM address at which voice synthesis ends. |
| | | H | ST15 to ST8 | | | | | | | | |
| | | H | ST7 to ST0 | | | | | | | | |
| | | H | S3 to S0 | | | | P1 to P0 | | 0 | 0 | Selects a sampling frequency using S3 to S0. Selects a voice synthesis method using P1 to P0. |
| | | L | 0 | 0 | 1 | 1 | 0 | 0 | CH1 to CH0 | | Selects the condition to a channel selected by C2 to C0. |
| None | CVOL | H | X | X | X | X | V3 to V0 | | | | Sets a playback volume between V3 and $V0 \times -2$ dB. |
| | | L | 0 | 0 | 1 | 1 | 1 | C2 to C0 | | | Selects a channel to which a playback volume is set. |
| None | PAN | H | L3 to L0 | | | | R3 to R0 | | | | Selects a left side voice volume using L3 to L0 and selects a right side voice volume using R3 to R0. The volume of output is -2 dB \times (L or R). |
| | | L | 0 | 1 | 0 | 0 | 0 | C2 to C0 | | | Selects a channel for setting PAN using C2 to C0. |

X: Don't Care

Sampling Frequency List

| S3 to S0 | Sampling Frequency |
|----------|--------------------|
| 0 | 4.0 kHz |
| 1 | 8.0 kHz |
| 2 | 16.0 kHz |
| 3 | 32.0 kHz |
| 4 | Undefined |
| 5 | 6.4 kHz |
| 6 | 12.8 kHz |
| 7 | 25.6 kHz |
| 8 | Undefined |
| 9 | 5.3 kHz |
| 10 | 10.6 kHz |
| 11 | 21.2 kHz |
| 12 | Undefined |
| 13 | Undefined |
| 14 | Undefined |
| 15 | Undefined |

Voice Synthesis Algorithm List

| P1 to P0 | Voice synthesis algorithm |
|----------|---------------------------|
| 0 | OKI 4-bit ADPCM |
| 1 | OKI 4-bit ADPCM2 |
| 2 | 8-bit Straight PCM |
| 3 | OKI 8-bit Nonlinear PCM |

PAN and CVOL List

| L3 to L0 R3 to R0 V3 to V0 | Volume | L3 to L0 R3 to R0 V3 to V0 | Volume |
|----------------------------------|--------|----------------------------------|--------|
| 0 | 0 dB | 8 | -16 dB |
| 1 | -2 dB | 9 | -18 dB |
| 2 | -4 dB | 10 | -20 dB |
| 3 | -6 dB | 11 | -22 dB |
| 4 | -8 dB | 12 | -24 dB |
| 5 | -10 dB | 13 | -26 dB |
| 6 | -12 dB | 14 | -28 dB |
| 7 | -14 dB | 15 | -30 dB |

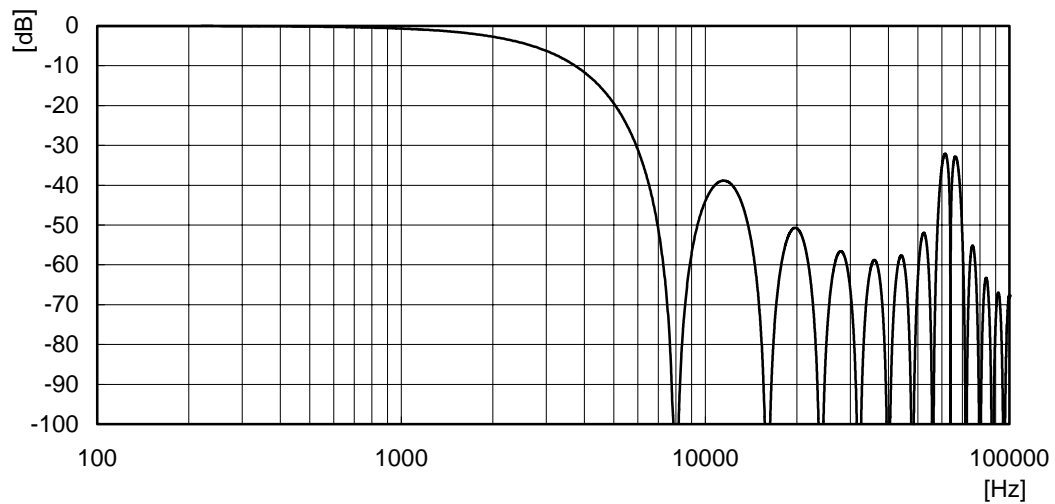
OPT Command List

| Default | O4 | O3 | O2 | O1 | O0 | Description |
|---------|----|----|----|----|----|---|
| * | 0 | 0 | x | x | x | Sets the volumes of all channels to V_{DD} (p-p). |
| | 0 | 1 | x | x | x | Sets the volumes of all channels to $1/2 V_{DD}$ (p-p). |
| | 1 | 0 | x | x | x | Sets the volumes of all channels to $1/4 V_{DD}$ (p-p). |
| | 1 | 1 | x | x | x | Sets the volumes of all channels to $1/8 V_{DD}$ (p-p). |
| * | x | x | 0 | 0 | x | Secondary digital filtering is performed. |
| | x | x | 0 | 1 | x | Primary digital filtering is performed. |
| | x | x | 1 | x | x | An on-chip digital filter is not used. |
| * | x | x | x | x | 0 | Data is output directly from a D/A converter. (Output $Z \cong 3 \text{ k}\Omega$) |
| | x | x | x | x | 1 | Data is output via an OP amplifier. (Output $Z \cong 500 \Omega$) |

(Note) x indicates that data is independent of a function described.

LPF Frequency Characteristics

This LSI contains a LPF in which a digital filter technology is used. The frequency characteristics when a secondary filter is used at $f_s = 8$ kHz is shown below. The cutoff frequency is directly proportional to the sampling frequency f_s .



LPF Output Frequency Characteristics ($f_s = 8$ kHz)

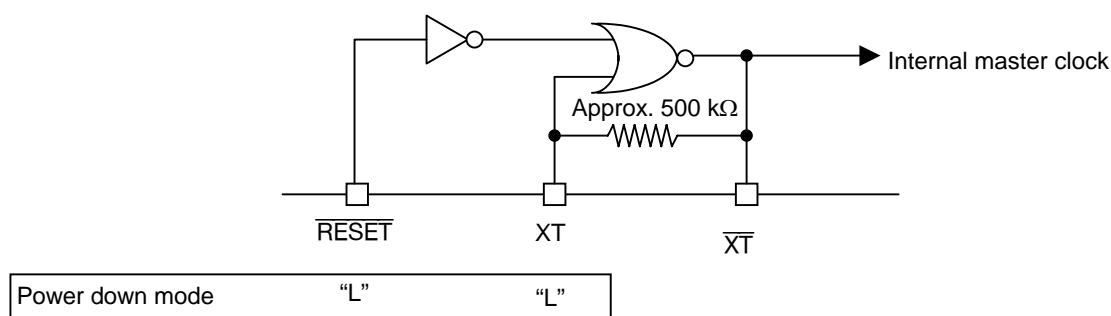
Power Down Function

To enter the power down mode, set the $\overline{\text{RESET}}$ pin to "L".

When an external clock is supplied to the XT pin, fix the $\overline{\text{XT}}$ pin at "L".

If an external clock is supplied via the XT pin during the power down mode, the I_{DS} specification is not satisfied because current flows between the XT pin and the $\overline{\text{XT}}$ pin.

The circuit of XT and $\overline{\text{XT}}$ pins is shown below.



Channel Status

The channel status includes NCR_n and $\overline{\text{BUSY}}_n$. These two channel statuses can be switched by setting the $\text{NCR}/\overline{\text{BUSY}}$ pin.

| Corresponding channel | $\text{NCR}/\overline{\text{BUSY}} = \text{"H"}$ | $\text{NCR}/\overline{\text{BUSY}} = \text{"L"}$ |
|-----------------------|--|--|
| CH1 | NCR_1 | $\overline{\text{BUSY}}_1$ |
| CH2 | NCR_2 | $\overline{\text{BUSY}}_2$ |
| CH3 | NCR_3 | $\overline{\text{BUSY}}_3$ |
| CH4 | NCR_4 | $\overline{\text{BUSY}}_4$ |

The n-channel NCR signal is NCR_n and the n-channel $\overline{\text{BUSY}}$ signal is $\overline{\text{BUSY}}_n$.

When NCR_n is "H", the START command and MUON command can be input for the next message of "n" channel to be played. When the phrase control table is used and $\overline{\text{BUSY}}_n$ is "L", do not enter the START command and MUON command even if NCR_n is "H". Otherwise, the LSI may malfunction.

When $\overline{\text{BUSY}}_n$ is "H", the "n" channel does not output a voice.

When $\overline{\text{BUSY}}_n$ is "L", the "n" channel outputs a voice.

Parallel I/O (SERIAL = "L")

The outputs of channel statuses in parallel I/O mode are shown below.

| Pin name | NCR/ $\overline{\text{BUSY}}$ = "H" | NCR/ $\overline{\text{BUSY}}$ = "L" |
|----------|-------------------------------------|-------------------------------------|
| D3 | NCR4 | $\overline{\text{BUSY4}}$ |
| D2 | NCR3 | $\overline{\text{BUSY3}}$ |
| D1 | NCR2 | $\overline{\text{BUSY2}}$ |
| D0 | NCR1 | $\overline{\text{BUSY1}}$ |

Serial I/O (SERIAL = "H")

The outputs when channel statuses are serially read during serial I/O mode are shown below.

| Signal name | NCR/ $\overline{\text{BUSY}}$ = "H" | NCR/ $\overline{\text{BUSY}}$ = "L" |
|-------------|-------------------------------------|-------------------------------------|
| SO7 | NCR8 | $\overline{\text{BUSY8}}$ |
| SO6 | NCR7 | $\overline{\text{BUSY7}}$ |
| SO5 | NCR6 | $\overline{\text{BUSY6}}$ |
| SO4 | NCR5 | $\overline{\text{BUSY5}}$ |
| SO3 | NCR4 | $\overline{\text{BUSY4}}$ |
| SO2 | NCR3 | $\overline{\text{BUSY3}}$ |
| SO1 | NCR2 | $\overline{\text{BUSY2}}$ |
| SO0 | NCR1 | $\overline{\text{BUSY1}}$ |

The outputs when channel statuses are output via SR3 to SR0 during serial I/O mode are shown below.

| Pin name | UD = "L" | | UD = "H" | |
|----------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| | NCR/ $\overline{\text{BUSY}}$ = "H" | NCR/ $\overline{\text{BUSY}}$ = "L" | NCR/ $\overline{\text{BUSY}}$ = "H" | NCR/ $\overline{\text{BUSY}}$ = "L" |
| SR3 | NCR4 | $\overline{\text{BUSY4}}$ | NCR8 | $\overline{\text{BUSY8}}$ |
| SR2 | NCR3 | $\overline{\text{BUSY3}}$ | NCR7 | $\overline{\text{BUSY7}}$ |
| SR1 | NCR2 | $\overline{\text{BUSY2}}$ | NCR6 | $\overline{\text{BUSY6}}$ |
| SR0 | NCR1 | $\overline{\text{BUSY1}}$ | NCR5 | $\overline{\text{BUSY5}}$ |

Voice Synthesis Algorithms

The MSM9810B contains 4-bit ADPCM algorithm, 4-bit ADPCM2 algorithm, 8-bit straight PCM algorithm, and 8-bit non-linear PCM algorithm. One of these algorithms can be selected depending on the kind of voices to be played. The features of these algorithms are described below.

| Voice synthesis algorithm | Applicable waveform | Feature |
|---------------------------|---|---|
| Oki 4-bit ADPCM | Normal voice waveforms | Oki-original 4-bit ADPCM |
| Oki 4-bit ADPCM2 | Normal voice waveforms | An improved version of Oki-original 4-bit ADPCM. This algorithm has improved its waveform traceability. |
| Oki 8-bit Nonlinear PCM | Sound effects including high frequency components | This algorithm plays back the center of waveform as a 10-bit sound. |
| 8-bit PCM | Sound effects including high frequency components | Normal 8-bit PCM algorithm |

Memory Configuration and Voice Data Creation Method

The ROM data consists of a voice management area, a voice data area, and a phrase control table area.

The voice management area controls the voice data start address, voice data end address, and use of the phrase control table.

256 phrases of voice management data are stored in this area.

The voice data area stores actual waveform data.

The phrase control table area stores data for effectively using voice data. See “Phrase Control Table Function” for details.

The ROM data is created by using a dedicated tool.

| ROM address | |
|----------------|--|
| 0x000000 | Voice management area (16 Kbit fixed) |
| 0x0007FF | |
| 0x000800 | Voice data area |
| max: 0x7ffffff | |
| max: 0x7ffffff | Phrase control table area This area is used to create ROM data. |

Playback Time and Memory Capacity

The playback time is determined by external memory capacity, sampling frequency, and voice synthesis algorithm. The relationship is described below.

$$\text{Playback time} = \frac{1.024 \times (\text{Memory capacity} - 16) \text{ (Kbits)}}{\text{Sampling frequency (kHz)} \times \text{bit length}} \quad \text{(Seconds)}$$

(The bit length is 4 bits for ADPCM and ADPCM2 and 8 bits for PCM.)

When the sampling frequency is 16 kHz and the voice synthesis algorithm is 4-bit ADPCM and an 8-Mbit ROM is used, the playback time is calculated as shown below.

$$\text{Playback time} = \frac{1.024 \times (8192 - 16) \text{ (Kbits)}}{16 \text{ (kHz)} \times 4 \text{ (bit)}} \cong 131 \text{ (Seconds)}$$

In the above equation, the playback time when the phrase control table function is not used is shown.

Mixing Function

It is possible to mix eight channels at a time. Moreover, the LSI is capable of starting or stopping voices of each channel separately.

- Note on waveform clamping during mixing
Increasing the number of channels to be mixed may cause clamping.
To prevent clamping, reduce the volumes of all channels using the OPT command.

(Note)

Mixing using a different sampling frequency cannot be done.

Continuous Playback Function

The continuous playback function is used to continuously play back the next phrase after playing back a phrase. The next phrase to be played can be previously selected while a phrase is being played back. See “Continuous Playback Flowchart” for details.

The continuous playback function is also available in the case of the phase control table.

(Note)

The following changes of voice synthesis algorithms are not permitted for continuous playback function. These changes may generate noises.

- ADPCM → ADPCM2
- ADPCM2 → ADPCM

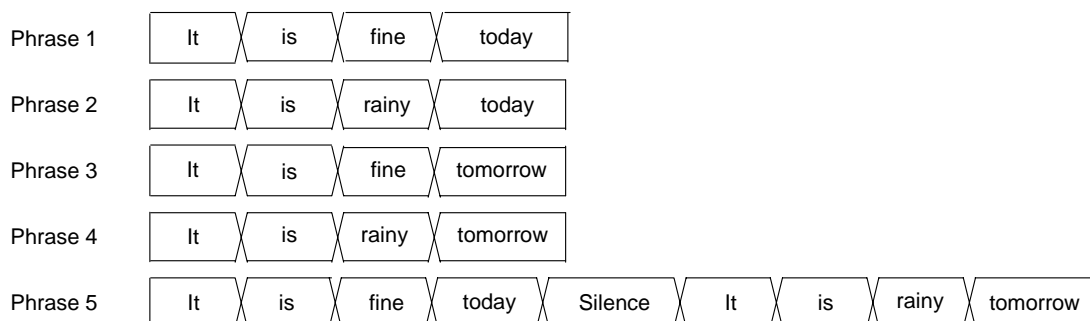
Phrase Control Table Function

The phrase control table function is used to continuously play back multiple phrases. It is possible to perform the following functions using the phrase control table function.

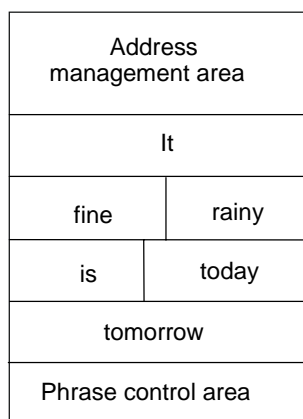
- Continuous playback (The number of continuous playbacks can be specified limitlessly, but depends on memory capacity.)
- Silence insertion function (4 mSec to 124 mSec)

The memory capacity of voice ROM is effectively used by using the phrase control table function. Examples of ROM data when the phrase control table function is used are shown below.

Example 1) Phrases when the phrase control table function is used



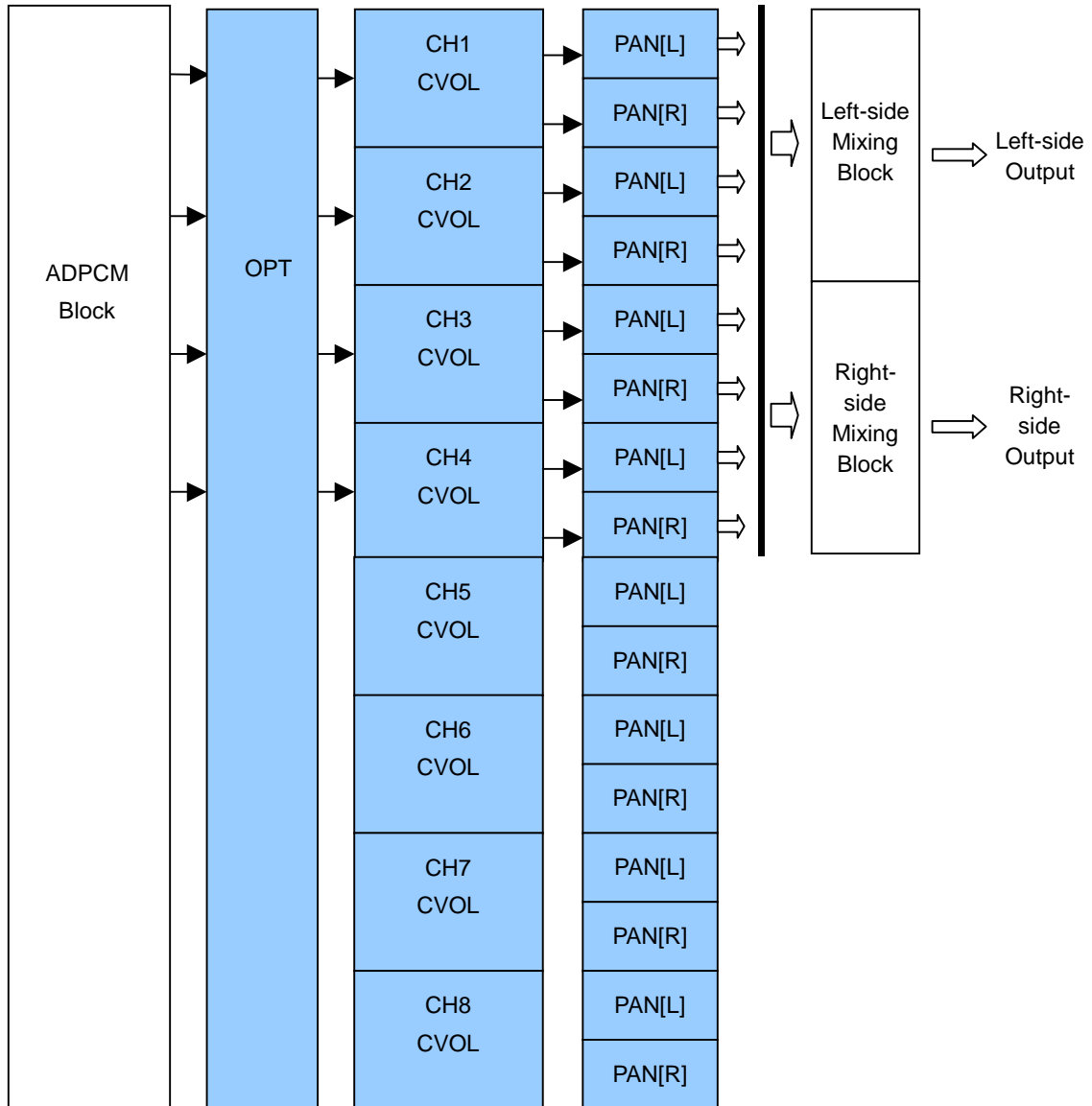
Example 2) ROM data when the example 1 is converted into ROM



Volume Function

A volume can be adjusted at the stages of OPT, CVOL and PAN as shown below.

- A volume is set to all channels at the stage of OPT.
- A volume is set to each channel at the stage of CVOL.
- A volume is set to “L” and “R” of each channel at the stage of PAN.



The output level attenuations when the CVOL, OPT and PAN commands are executed are shown below.

<Left-side output volume calculation>

Left-side output volume = $(V + L) \times -2 + (O4 \times 2 + O3) \times -6$ [dB]

V: Setting a volume (0 to 15) with the CVOL command

L: Setting a left-side volume (0 to 15) with the PAN command

O4, O3: Setting a volume (0 or 1) with the OPT command

<Right-side output volume calculation>

Right-side output volume = $(V + L) \times -2 + (O4 \times 2 + O3) \times -6$ [dB]

V: Setting a volume (0 to 15) with the CVOL command

L: Setting a right-side volume (0 to 15) with the PAN command

O4, O3: Setting a volume (0 or 1) with the OPT command

COMMAND FUNCTIONS

START Command

The START command starts voice synthesis of the channel corresponding to the data stored in the TMP register. Table 1 shows the correspondence between data input (D7-D0) and channels. In the case of serial input, all 8 bits of D7 to D0 should be input serially from MSB.

Table 1 Correspondence between D7-D0 and Channels

| Data bus | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Corresponding channel | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |

When the START command is input, data stored in the TMP register is set at the start register, and voice synthesis processing starts. For example, when all “1” is written from the data bus to the TMP register and the START command is input, all channels start voice synthesis simultaneously.

Input the START command when the status signal (NCR or $\overline{\text{BUSY}}$) of the channel to be started is at “H”. When NCR is “L”, input is disabled. When the phrase control table is used, input the START command while $\overline{\text{BUSY}}$ is “H”. Otherwise, the LSI may malfunction.

Figure 4 shows the flowchart when the START command is input.

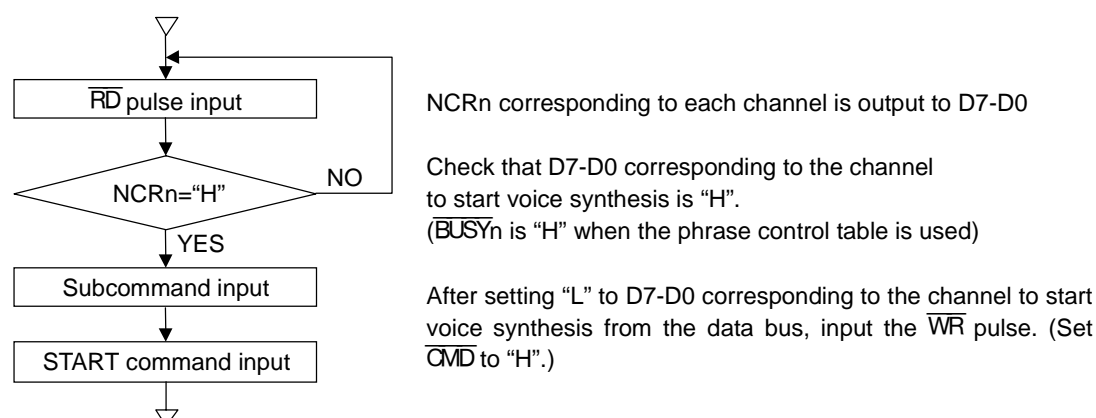


Figure 4 START Command Input Flow

STOP Command

The STOP command stops voice synthesis processing of the channel corresponding to data stored in the TMP register. Table 2 shows the correspondence between data input (D7-D0) and channels.

Table 2 Correspondence between D7-D0 and channels

| Data bus | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Corresponding channel | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |

When the STOP command is input, the LSI stops processing of voice synthesis of the corresponding channel at the rise of the $\overline{\text{WR}}$ pulse. When voice synthesis stops, the PCM value of that channel is cleared to $1/2 V_{\text{DD}}$, and the NCR and $\overline{\text{BUSY}}$ channel status signals become “H”.

When “H” has been set at the START register, the START register is cleared to “L”.

LOOP Command

The LOOP command repeats a playback of voice synthesis of the channel corresponding to data stored in the TMP registers. Table 3 shows the correspondence between data input (D7-D0) and channels.

Table 3 Correspondence between D7-D0 and Channels

| Data bus | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Corresponding channel | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |

When the LOOP command is input, the LSI writes data of the TMP register to the LOOP register at rise of \overline{WR} pulse, and repeats a playback of the channel where "H" is set. Once "H" is set at the LOOP register, playback continues until "L" is set from the outside. If the phrase control table function has been used for a phrase address, the edited voice is repeatedly played back.

To end a repeating playback, set the register of the channel to end the repeat to "L" using the LOOP command again. When the register is set to "L", repeating ends with the phrase next to the current playback phrase. If the START register has been set to continue the playback of another phrase, another phrase is played back continuously after repeating ends.

Figure 5 shows an example.

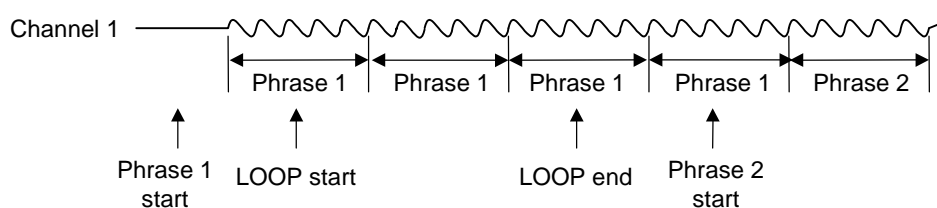


Figure 5 LOOP Command Execution Example

OPT Command

The OPT command changes the setting inside the LSI according to data stored in the TMP register. Table 4 shows the correspondence between data input (D7 to D0) and options. (Input “L” to D7-D5.)

Table 4 OPT Command List

| Default | O4 | O3 | O2 | O1 | O0 | Description |
|---------|----|----|----|----|----|---|
| * | 0 | 0 | x | x | x | Sets the volumes of all channels to V_{DD} (p-p). |
| | 0 | 1 | x | x | x | Sets the volumes of all channels to $1/2 V_{DD}$ (p-p). |
| | 1 | 0 | x | x | x | Sets the volumes of all channels to $1/4 V_{DD}$ (p-p). |
| | 1 | 1 | x | x | x | Sets the volumes of all channels to $1/8 V_{DD}$ (p-p). |
| * | x | x | 0 | 0 | x | Secondary digital filtering is performed. |
| | x | x | 0 | 1 | x | Primary digital filtering is performed. |
| | x | x | 1 | x | x | An on-chip digital filter is not used. |
| * | x | x | x | x | 0 | Data is output directly from a D/A converter. (Output $Z \cong 3 \text{ k}\Omega$) |
| | x | x | x | x | 1 | Data is output via a voltage follower. (Output $Z \cong 500 \Omega$) |

(Note) x indicates that data is independent of a function described.

When the OPT command is input, the LSI changes the option at the rising edge of the \overline{WR} pulse. When power is turned on, or when the \overline{RESET} pulse is input, the registers corresponding to D4-D0 have been set to “L”.

If the option is changed when voice synthesis is in execution, voice quality may change. Oki recommends to set the option after power is turned on or after \overline{RESET} is input.

1) Volume Option

Volume can be set by the CVOL command and PAN command, but a waveform may be clamped when channel synthesis is executed.

If the CVOL command and PAN command are used to prevent a waveform from being clamped, the number of steps used for actual volume decreases, and effective voice synthesis may not be performed.

If it is known that a waveform will be clamped, this option can set the volume of all channels to low, so that the number of steps of the volume can be utilized to the maximum level.

2) Digital Filter Processing

This LSI has a built-in oversampling circuit for digital filter processing. This oversampling system evenly generates four times more points of sampling frequencies.

When power is turned on or if the \overline{RESET} pulse is input, those pulses have been set to pass through the oversampling circuit. If digital filter processing is unnecessary, change this setting by the OPT command.

3) Analog Output

When power is turned on, it has been set that the output of the D/A converter is directly output. To change this setting, use the OPT command.

The output impedance of analog signals being output via the voltage follower is about 500 Ω .

The output impedance of analog signals directly output from the D/A converter is about 3 k Ω .

MUON Command

The MUON command inserts silence into the specified channel at the rise of the \overline{WR} pulse. The length of silence is according to the size of data stored in the TMP register.

The length of silence data is input in advance, before executing the MUON command. Silence length can be set for 255 steps, 4 ms to 1020 ms, in 4 ms intervals. Silence time can be set as follows.

$$t_{\text{mu}} = (2^7 \times (D7) + 2^6 \times (D6) + 2^5 \times (D5) + 2^4 \times (D4) + 2^3 \times (D3) + 2^2 \times (D2) + 2^1 \times (D1) + 2^0 \times (D0)) \times 4.096 \text{ ms}$$

The operation of the MUON command is similar to the START command to start voice synthesis. When the MUON command is input, "H" is set to the START register, and NCR and \overline{BUSY} signals become "L".

If the MUON command is input when voice synthesis is in execution, silence time is inserted after voice synthesis ends.

Input the MUON command when the status signal (NCR or \overline{BUSY}) of the channel to start voice synthesis is at "H". When NCR is "L", input is disabled. When the phrase control table is used, input the MUON command while \overline{BUSY} is "H". Otherwise, the LSI may malfunction.

Figure 6 shows a flow chart example when the MUON command is input.

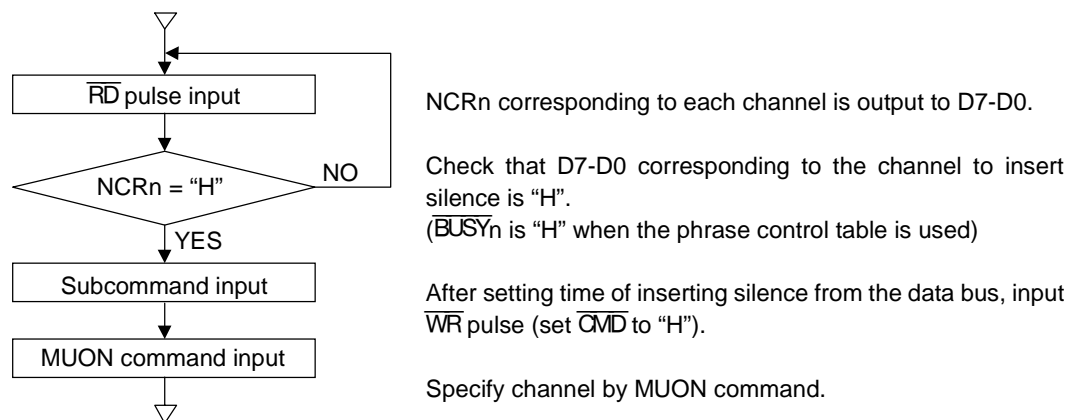


Figure 6 MUON Command Input Flow

FADR Command

The FADR command transfers data stored in the TMP register to the phrase address register of the corresponding channel at the rise of the \overline{WR} pulse.

For the phrase address, the user specification phrases have been set by an analysis tool, and the playback system, sampling frequency and start and stop address of voice data have been registered to the address management area. When the phrase address is set and the START command is input, the LSI reads data of the address management area, and starts voice synthesis.

Since the phrase address is set by D7-D0, a maximum of 256 phrases can be set. The edit function can be used for phrase addresses, so not only one phrase but combinations with other phrases are possible.

DADR Command

The DADR command transfers data stored in the TMP (1-7) register to the start and stop address register of the corresponding channel at the rise of the \overline{WR} pulse.

For the direct address, the playback system, sampling frequency, and start and stop addresses of voice data are directly input from the microcomputer without using the address management area.

Direct address playback system is available with channel 1 to 4, and not available with channel 5 to 8.

Since the phrase that can be set at a phrase address is a maximum of 256, if voice data exceeds 256 phrases, use this command. Data on the playback system, sampling frequency, and start and stop address of voice data is displayed when an analysis tool is used.

Data on the playback system, sampling frequency, and start and stop address of voice data is input to the TMP1 to TMP7 registers divided in 7 steps, unlike the data input of other commands.

Figure 7 shows the input method.

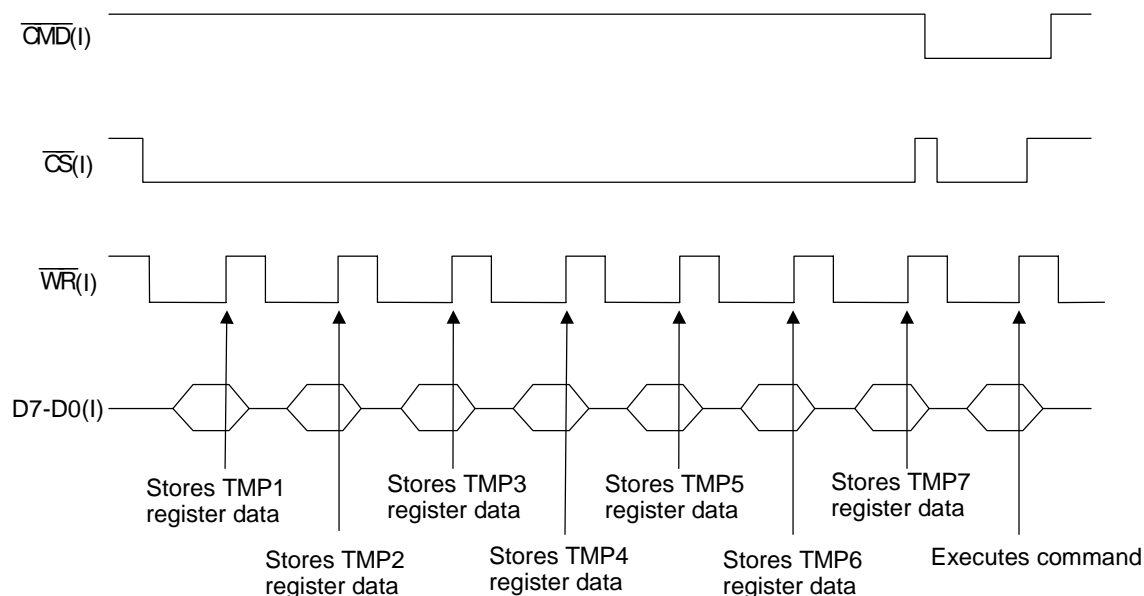


Figure 7 DADR Input Timing

As Figure 7 shows, \overline{CS} and \overline{WR} pulses are input 7 times when \overline{CMD} is in “H” status, to input data to the TMP1 to TMP7 registers. The LSI increments the registers at the rise of the \overline{WR} pulse when \overline{CMD} is “H”. \overline{CMD} must not be “L” while inputting data. When \overline{CMD} becomes “L” while inputting data, a normal setting cannot be made.

Table 5 shows the configuration of data to be input to TMP1 to TMP7 registers.

Table 5 TMP Register Data Configuration

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| TMP1 register | A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 |
| TMP2 register | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |
| TMP3 register | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| TMP4 register | T23 | T22 | T21 | T20 | T19 | T18 | T17 | T16 |
| TMP5 register | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 |
| TMP6 register | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| TMP7 register | S3 | S2 | S1 | S0 | P1 | P0 | 0 | 0 |

Input the start address of voice data to TMP1 to TMP3 registers. Input the stop address of voice data to TMP4 to TMP6 registers. Input the playback system and sampling frequency to the TMP7 register.

Table 6 shows the input data configuration of the playback system and sampling frequency.

Table 6 Data Configuration of Playback System and Sampling Frequency

| | | | | |
|----|----|----|--|-----------------------------|
| S3 | S2 | S1 | S0 | |
| 0 | 0 | 0 | 0 | Sampling frequency 4.0 kHz |
| 0 | 0 | 0 | 1 | Sampling frequency 8.0 kHz |
| 0 | 0 | 1 | 0 | Sampling frequency 16.0 kHz |
| 0 | 0 | 1 | 1 | Sampling frequency 32.0 kHz |
| 0 | 1 | 0 | 1 | Sampling frequency 6.4 kHz |
| 0 | 1 | 1 | 0 | Sampling frequency 12.8 kHz |
| 0 | 1 | 1 | 1 | Sampling frequency 25.6 kHz |
| 1 | 0 | 0 | 1 | Sampling frequency 5.3 kHz |
| 1 | 0 | 1 | 0 | Sampling frequency 10.6 kHz |
| 1 | 0 | 1 | 1 | Sampling frequency 21.3 kHz |
| P1 | P0 | | | |
| 0 | 0 | | Playback algorithm: 4-bit ADPCM | |
| 0 | 1 | | Playback algorithm: 4-bit ADPCM2 | |
| 1 | 0 | | Playback algorithm: 8-bit straight PCM | |
| 1 | 1 | | Playback algorithm: 8-bit non-linear PCM | |

CVOL Command

The CVOL command adjusts the volume of the specified channel to the volume which corresponds to the size of data stored in the TMP register at the rise of the \overline{WR} pulse.

Volume can be set in 16 steps up to -30 dB in -2dB step units. Set data as shown in Table 7.

Table 7 Volume Setting Data Configuration

| D3 | D2 | D1 | D0 | Volume(dB) |
|----|----|----|----|------------|
| 0 | 0 | 0 | 0 | 0 dB |
| 0 | 0 | 0 | 1 | -2 dB |
| 0 | 0 | 1 | 0 | -4 dB |
| 0 | 0 | 1 | 1 | -6 dB |
| 0 | 1 | 0 | 0 | -8 dB |
| 0 | 1 | 0 | 1 | -10 dB |
| 0 | 1 | 1 | 0 | -12 dB |
| 0 | 1 | 1 | 1 | -14 dB |
| 1 | 0 | 0 | 0 | -16 dB |
| 1 | 0 | 0 | 1 | -18 dB |
| 1 | 0 | 1 | 0 | -20 dB |
| 1 | 0 | 1 | 1 | -22 dB |
| 1 | 1 | 0 | 0 | -24 dB |
| 1 | 1 | 0 | 1 | -26 dB |
| 1 | 1 | 1 | 0 | -28 dB |
| 1 | 1 | 1 | 1 | -30 dB |

(D7-D4: Don't care)

When power is turned on and the \overline{RESET} pulse is input, all channels are set to 0 dB.

PAN Command

The PAN command adjusts the volume of the specified channel for the left and right respectively, to the volume which corresponds to the size of data stored in the TMP register at the rise of the \overline{WR} pulse.

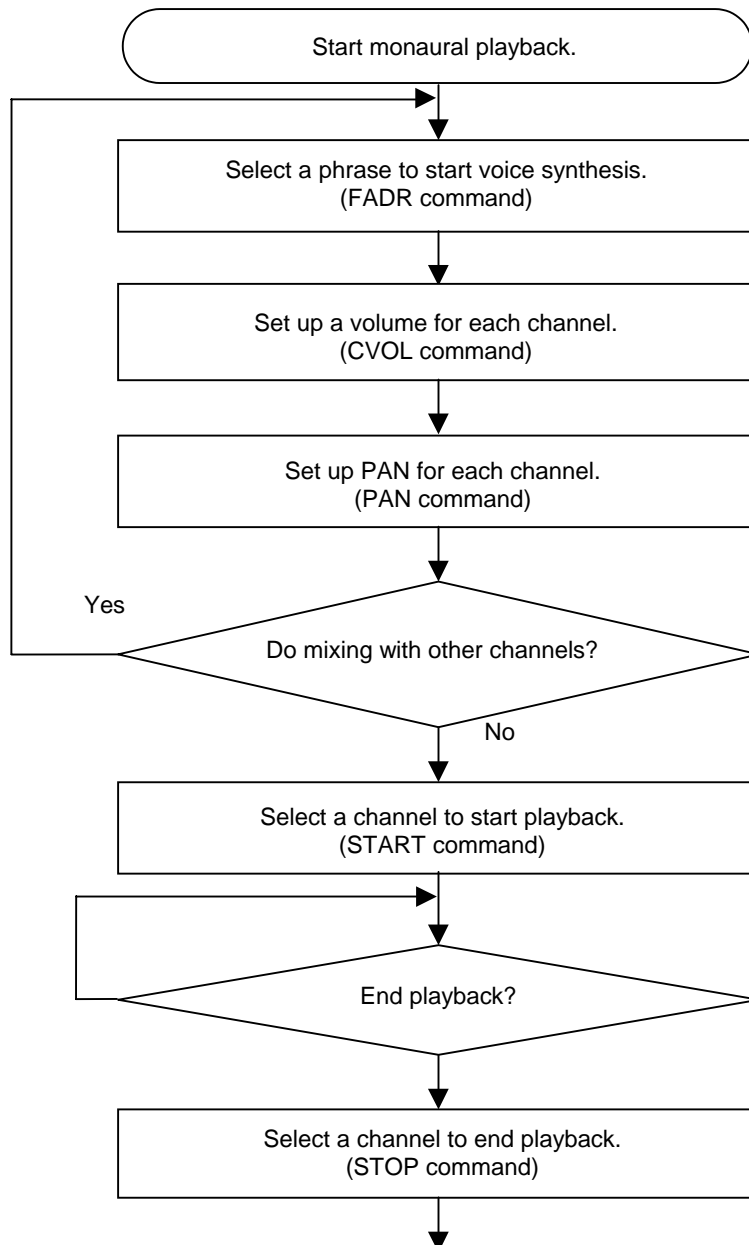
This command enables stereo output.

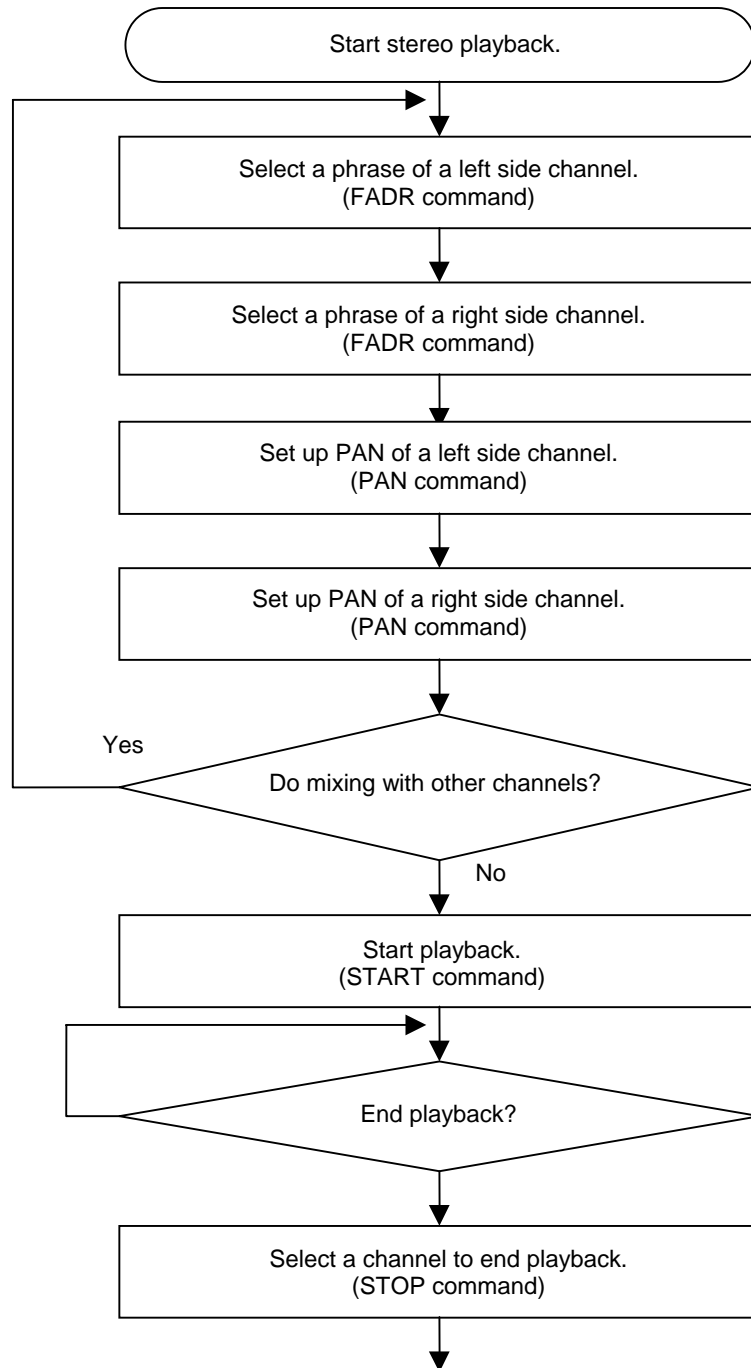
When volume is controlled by the OPT command and CVOL command, volume to be output is the volume stored in ROM multiplied by volume set by the OPT command, CVOL command, and PAN command respectively. This volume is output from LDAO and RDAO.

Volume can be set in 16 steps up to -30 dB in -2 dB step units. Set data as shown in Table 8.

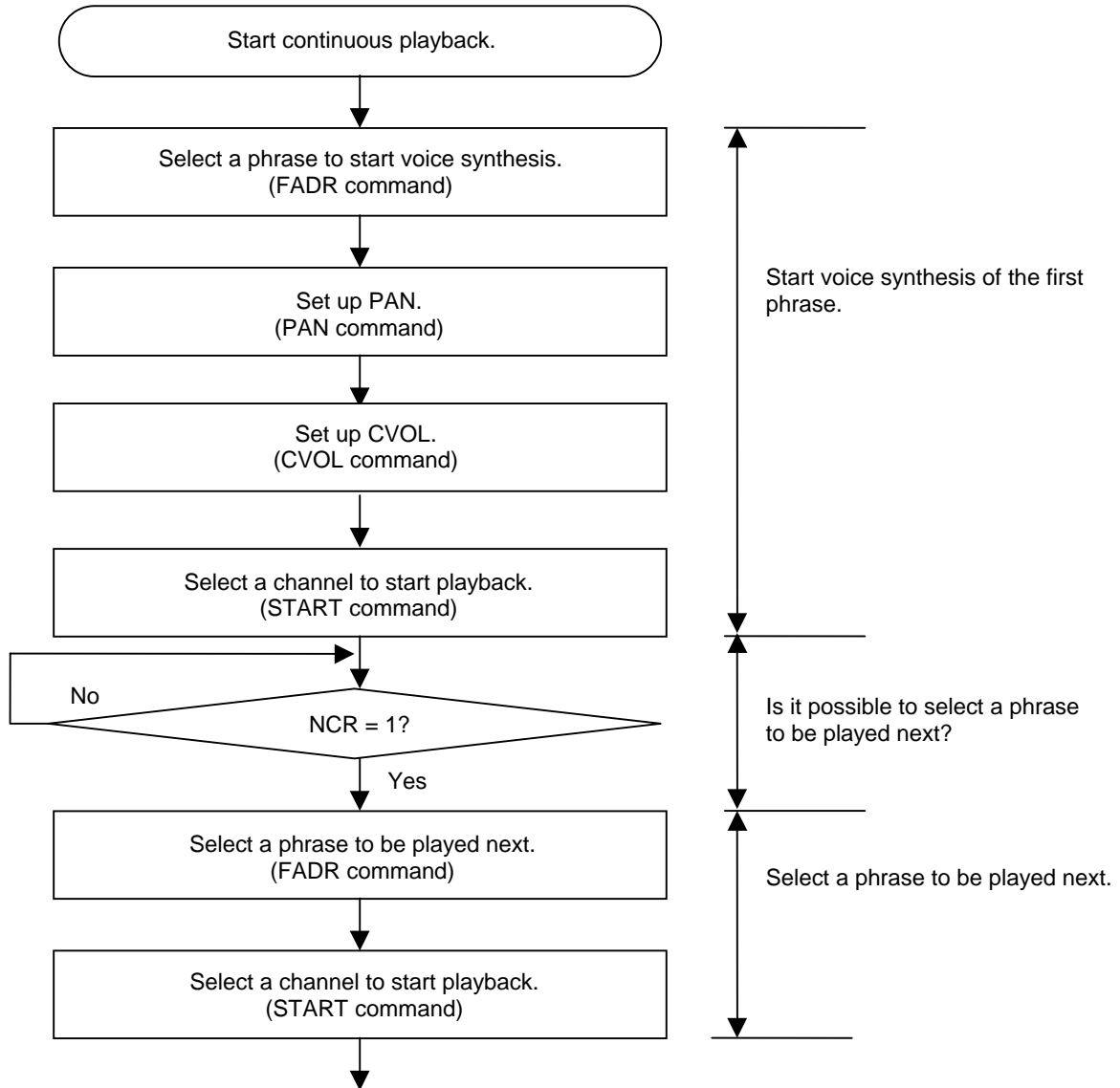
Table 8 PAN Data Configuration

| D7 | D6 | D5 | D4 | Volume at left side |
|----|----|----|----|----------------------|
| D3 | D2 | D1 | D0 | Volume at right side |
| 0 | 0 | 0 | 0 | 0 dB |
| 0 | 0 | 0 | 1 | -2 dB |
| 0 | 0 | 1 | 0 | -4 dB |
| 0 | 0 | 1 | 1 | -6 dB |
| 0 | 1 | 0 | 0 | -8 dB |
| 0 | 1 | 0 | 1 | -10 dB |
| 0 | 1 | 1 | 0 | -12 dB |
| 0 | 1 | 1 | 1 | -14 dB |
| 1 | 0 | 0 | 0 | -16 dB |
| 1 | 0 | 0 | 1 | -18 dB |
| 1 | 0 | 1 | 0 | -20 dB |
| 1 | 0 | 1 | 1 | -22 dB |
| 1 | 1 | 0 | 0 | -24 dB |
| 1 | 1 | 0 | 1 | -26 dB |
| 1 | 1 | 1 | 0 | -28 dB |
| 1 | 1 | 1 | 1 | -30 dB |

FLOWCHART**Monaural Playback**

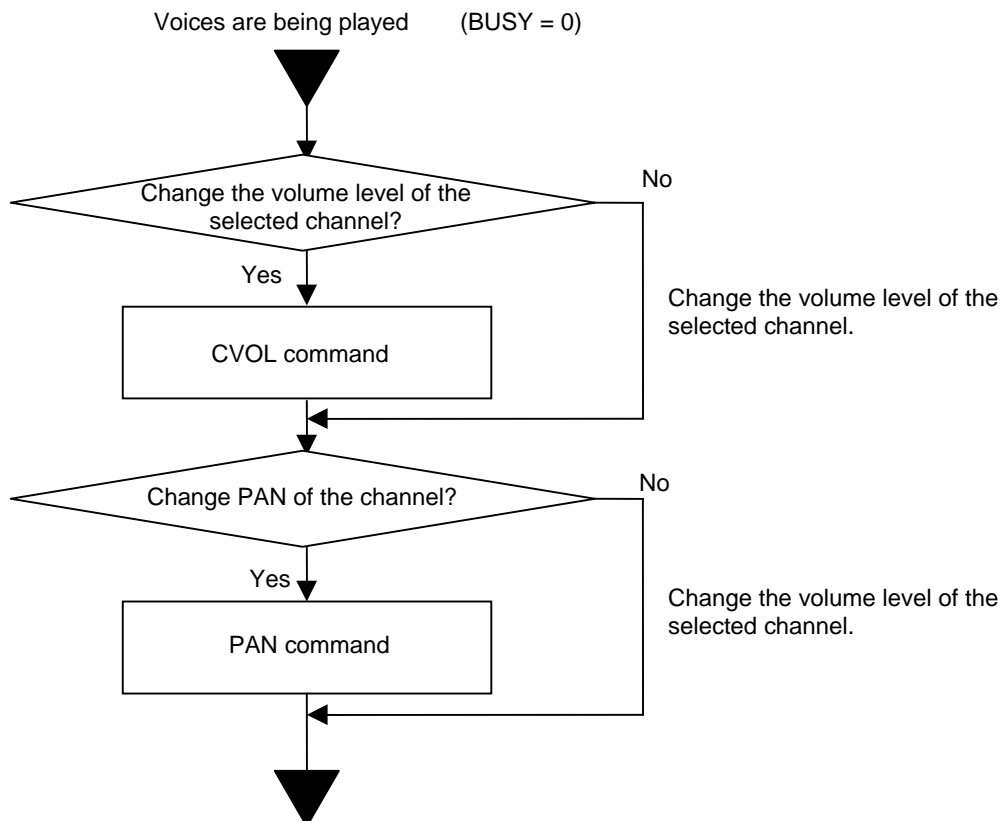
Stereo Playback

Continuous Playback

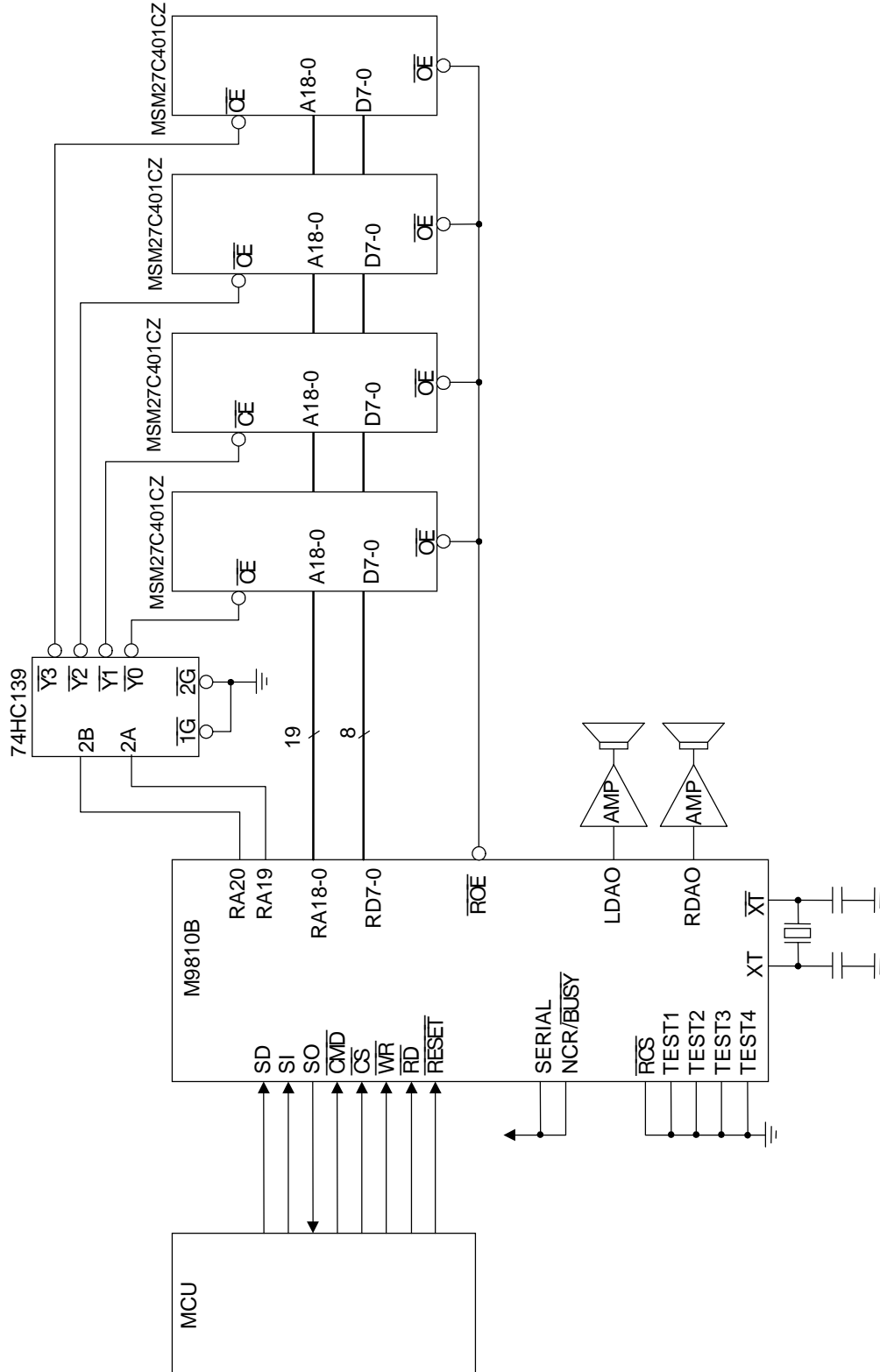


Changing Volume Level

It is possible to change the volume level of a channel that is being played. If the CVOL command is issued when voices are not being played, the changed volume level will be valid during the next playback. When the phrase control table function is used, the value of CVOL is changed by the phrase control table function because there are volume setting values in the phrase control table.



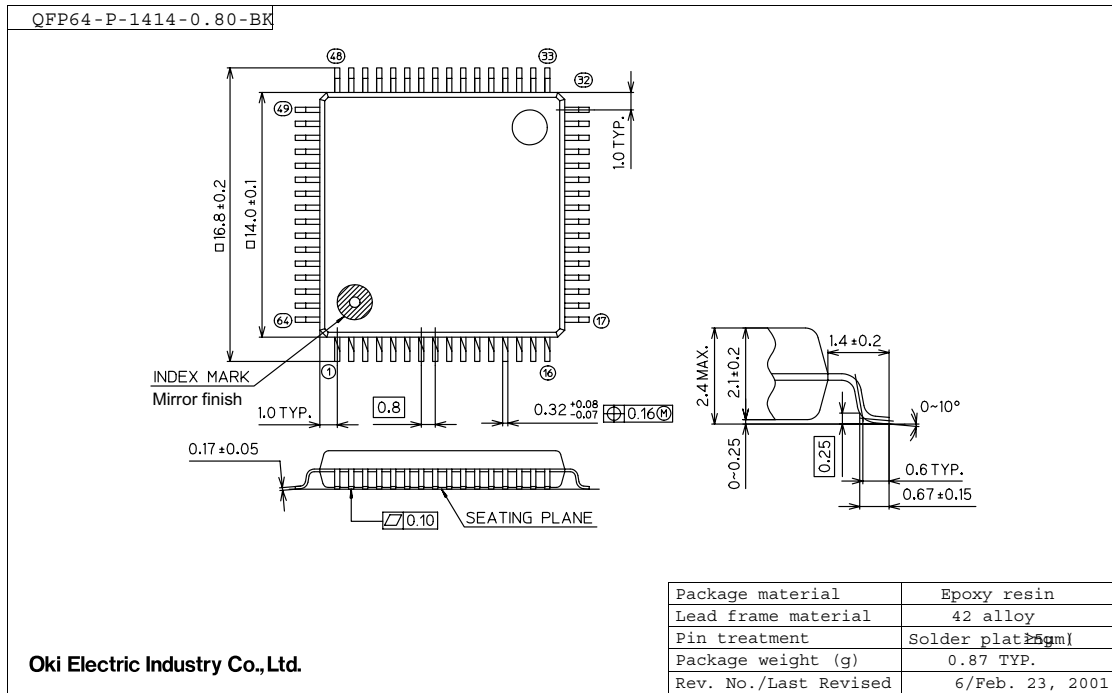
APPLICATION CIRCUITS



Application circuit example when four 4 Mbit OPT ROMs are connected (serial input interface)

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|------------------|--------------|------------------|-----------------|---|
| | | Previous Edition | Current Edition | |
| FEDL9810BFULL-01 | Jun. 2000 | – | – | Edition 1 |
| FEDL9810BFULL-02 | May. 2001 | – | – | Edition 2 |
| FEDL9810BFULL-03 | Jun 20, 2003 | 7,20,32,33 | 7,20,32,33 | Corrected the output impedance of analog signals. |
| | | 7 | 7 | Corrected the word "AOUT" to "LDAO,RDAO" In Analog Characteristics table. |

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