1. GENERAL DESCRIPTION

1.1 MT1379

The MT1379 Progressive Scan DVD-Player Combo Chip is a single-chip MPEG video decoding chip that integrates audio/video stream data processing, TV encoder, four video DACs with Macrovision. copy protection, DVD system navigation, system control and housekeeping functions.

The features of this chip can be listed as follows:

General Features:

- Progressive scan DVD-player combo chip
- Integrated NTSC/PAL encoder.
- Built-in progressive video output
- DVD-Video, VCD 1.1, 2.0, and SVCD
- Unified track buffer and A/V decoding buffer.
- Direct interface of 32-bit SDRAM.
- Servo controller and data channel processing.

Video Related Features:

- Macrovision 7.1 for NTSC/PAL interlaced video.
- Simultaneous composite video and S-video outputs, or composite and YUV outputs, or composite and RGB outputs.
- 8-bit CCIR 601 YUV 4:2:2 output.
- Decodes MPEG video and MPEG2 main profile at main level.
- Maximum input bit rate of 15Mbits/sec

Audio Related Features:

- Dolby Digital (AC-3) and Dolby Pro Logic.
- Dolby Digital S/PDIF digital audio output.
- High-Definition Compatible Digital. (HDCD) decoding.
- Dolby Digital Class A and HDCD certified.
- SRS TrueSurround ..
- CD-DA.
- MP3.

1.2 MEMORY

1.2.1 SDRAM Memory Interface

The MT1379 provides a glueless 16-bit interface to DRAM memory devices used as OSD, MPEG stream and video buffer memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing. The memory interface controls access to both external SDRAM memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

1.3 DRIVE INTERFACES

The MT1379 supports the DV34 interface, and other RF and servo interfaces used by many types of DVD loaders. These interfaces meet the specifications of many DVD loader manufacturers.

1.4 FRONT PANEL

The front panel is based around an Futaba VFD and a common NEC front panel controller chip, (uPD16311). The MT1379 controls the uPD16311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the MT1379 for decoding.

1.5 REAR PANEL

A typical rear panel is included in the reference design. This rear panel supports:

- Six channel or two channel audio outputs
- Optical and coax S/PDIF outputs.
- Composite, S-Video, and SCART outputs

The six-video signals used to provide CVBS, S-Video, and RGB are generated by the MT1379's internal video DAC. The video signals are buffered by external circuitry.

Six channel audio output by the MT1379 in the form of three I^2S (or similar) data streams. The S/PDIF serial stream is also generated by the MT1379 output by the rear panel. The six channel audio DACs (AK4356,PCM1606) are used for six channel audio output with MT1379, and similarly AK4382A ,CS4392 Audio DACs are used for two channel audio output with MT1379.

2. SYSTEM BLOCK DIAGRAM and MT1379 PIN DESCRIPTION

2.1 MT1379 PIN DESCRIPTION

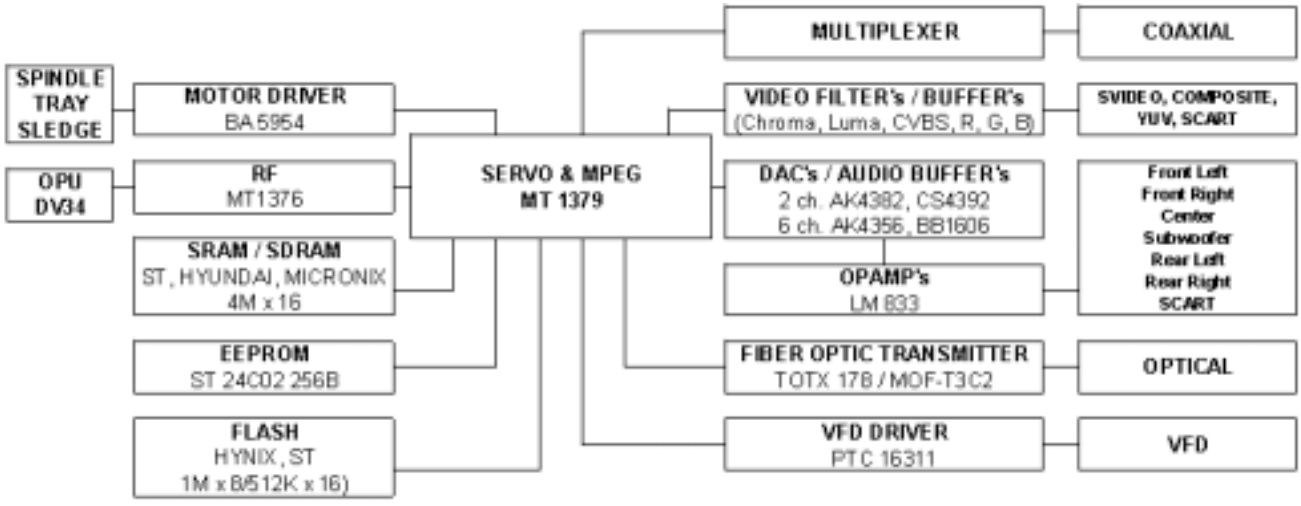
SYMBOL	TYPE	PIN NUMBERS	DEFINITION
DVSS	Ground	20,28,60,77,92,102 115,125,135,145 178,189	Ground pin for internal digital circuitry
IREF	Analog Input	1	Current reference input. It generates reference Current for data PLL. Connect an external 100K Resistor to this pin and PLLVSS.
PLLVSS	Ground	2	Ground pin for PLL and analog circuitry
LPIOP	Analog Output	3	Positive output for low pass filter(LFP)
LPION	Analog Output	4	Negative output for LFP
LPFON	Analog Output	5	Negative output of loop filter amplifier(LFA)
LPFIP	Analog Input	6	Positive input of LFA
LPFIN	Analog Input	7	Negative input of LFA
LPFOP	Analog Output	8	Positive output of LFA
JITFO	Analog Output	9	RF jitter meter output
JITFN	Analog Input	10	Negative input of the operational amplifier for RF jigger meter
PLLVDD3	Power	11	3.3V power pin for data PLL and related analog circuitry
FOO	Analog Output	12	Focus servo output. PDM output of focus servo compensator
TRO	Analog Output	13	Tracking servo output. PDM output of tracking servo compensator
TROPENPWM	Analog Output	14	Tray open output,controlled by microcontroller. This is PWM output for TRWMEN27hRW2=1 or is digital output for TRWMEN27hRW2=0
PWMOUT1-2	Analog Output	15-16	1st and 2nd general PWM output.
DVDD2	Power	17,42,72,82,120,140,182	2.5V power pin for internally fully digital circuitry.
DMO	Analog Output	18	Disk motor control output. PWM output.
FMO	Analog Output	19	Feed motor control PWM output.
FG	Input	21	Motor Hall sensor input
HIGHA0-5	Inout 2~16MA,SR PU	22-27	Microcontroller address 8-13
HIGHA6-7	Inout 2~16MA,SR PU	29-30	Microcontroller address 14-15
AD7-4	Inout 2~16MA,SR	31-34	Microcontroller address/data 7-4
DVDD3	Power	35,66,97,111,130,150,185 ,192	3.3 power pin for internal digital circuitry
AD3-0	Inout 2~16MA,SR	36-39	Microcontroller address/data 3-0
IOA0-1	Inout 2~16MA,SR PU	40-41	Microcontroller adress 0-1/IO
IOA2-7	Inout 2~16MA,SR PU	43-48	Microcontroller adress 2-7/IO
A16-17	Output 2~16MA,SR	49-50	Flash adress 16-17
IOA18-20	Inout 2~16MA,SR SMT	51-52	Flash adress 18-19
APLLVSS	Ground	54	Ground pin for audio clock circuitry
APLLVDD3	Power	55	3.3V power pin for audio clock circuitry
ALE	Inout 2~16MA,SR,PU,S MT	56	Microcontroller address latch enable
IOOE#	Inout 2~16MA,SR SMT	57	Flash output enable, active low I/O
IOWR#	Inout 2~16MA,SR,SMT	58	Flash write enable, active low/IO
IOCS#	Inout 2~16MA,SR,PU,S MT	59	Flash chip select,active low/IO
UP1_2-6,7	Inout 4MA,SR,PU,SMT	61-65,67	Microcontroller port 1-2…1-7
UP3_0-1	Inout	68,69	Microcontroller port 3-0,3-1

	4MA,SR,PU,SMT		
INT0#	Inout 2~16MA,SR,PU,SMT	70	Microcontroller interrupt 0, active low
IR	Input SMT	71	IR control signal input
UP3_4,5	Inout	73-74	Microcontroller port 3-4,3-5
UWR#	Inout 2~16MA,SR,PU,SMT	75	Microcontroller write strobe,active low
URD#	Inout 2~16MA,SR,PU,SMT	76	Microcontroller write strobe,active low
RD7-4,3-0	DRAM data 7-4,3-0	78-81,83-86	DRAM data 7-4,3-0
RWE#	Output 2~16MA,SR	87	DRAM write enable, active low.
CAS#	Output 2~16MA,SR	88	DRAM column adress strobe,active low
RAS#	Output 2~16MA,SR	89	DRAM row adress strobe,active low
RCS#	Output 2~16MA,SR	90	DRAM chip select, active low
BA0	Output 2~16MA,SR	91	DRAM bank adress 0
RD15-12,11-8	Inout 2~16MA,SR,PU/PD,SMT	93-96,98-101	DRAM data 15-12,11-8
CLK	Output 2~16MA,SR	103	DRAM clock
CLE	Output 2~16MA,SR	104	DRAM clock enable
RA11	Output 2~16MA,SR	105	DRAM adress bit 11 or serial data 3(channel 7/8)
RA9,8,7,6-4,10,0-3	Output 2~16MA,SR	106,107,110,112-114,119,121-124	DRAM adresses
DMVDD3	Power	108	3.3V Power pin for DRAM clock circuitry
DMVSS	Ground	109	Ground pin for DRAM clock circuitry
DQM1,0-3,2	Output 2~16MA,SR	116,117-136,137	Mask for DRAM input/output byte 1,0
BA1	Output 2~16MA,SR	118	DRAM bank address 0
RD31-28,27-24	Inout 2~16MA,SR PU/PD SMT	126-129,131-134	DRAM corresponding data
RD23-22,21-18	Inout 2~16MA,SR PU/PD SMT	138-139,141-144	DRAM data 23-22,21-18/Videoin Data PortA 7-6,5-2
RD17-16	Inout 2~16MA,SR PU/PD SMT	146-147	DRAM data 17-16/Videoin Data PortA 1-0
ABCK	Output 4MA	148	Audio bit clock
ALRCK	Inout 4MA,PD,SMT	149	Audio L/R channel clock,Trap value in power-on reset 1:ext. 0:int.
ACLK	Inout 4MA	151	Audio DAC master clock(384/256 audio sample frequency)
MC_DATA	Input	152	Microphone serial input
SPDIF	Output 2~16MA,SR :ON/OFF	153	SPDIF output
ASDATA0	Inout 4MA PD SMT	154	(1)Audio serial data 0(L/R)(2)Trap value in power on reset 1:factory test mode 0:normal mode
ASDATA1	Inout 4MA PD SMT	155	Audio serial data 1(surround L/R),Trap value in power-on reset
ASDATA2	Inout 4MA PD SMT	156	Audio serial data 2(center/left),Trap value in power-on reset
ASDATA3	Inout 4MA PD SMT	157	Audio serial data 3(surround L/R),Trap value in power-on reset,videoin data portb 1
ASDATA4	Inout 4MA PD SMT	158	Audio serial data 4(center/left),Trap value in power-on reset,videoin data portb 2
DACVDDC	Power	159	3.3V power pin for VİDEO DAC circuitry
VREF	Analog input	160	Bandgap refernce voltage
FS	Analog Output	161	Full scale adjustment
YUV0/CIN	Output 4MA,SR	162	Video data output bit 0/Compensation capacitor
DACVSSC	Ground	163	Ground pin for VIDEO DAC circuitry
YUV1/C	Output 4MA,SR	164	Video data output bit 1/Compensation capacitor
DACVDDB	Power	165	3.3V power pin for VİDEO DAC circuitry
YUV2/Y	Output 4MA,SR	166	Video data output bit 2/ Analog Y output
DACVSSB	Ground	167	Ground pin for VIDEO DAC circuitry
YUV3/CVBS	Output 4MA,SR	168	Video data output bit 3/ Analog composite output
DACVDDA	Power	169	3.3V power pin for VİDEO DAC circuitry
YUV4/G	Output 4MA,SR	170	Video data output bit 4/Green or Y
DACVSSA	Ground	171	Ground pin for VIDEO DAC circuitry
YUV5/B	Output 4MA,SR	172	Video data output bit 5/Blue or CB
YUV6/R	Output 4MA,SR	173	Video data output bit 5/Red or CR
ICE	Input PD,SMT	174	Microcontroller ICE mode enable

BLANK#	Inout 4MA,SR,SMT	175	Video blank area, active low/ Videoin field_601
VSYN	Inout,4MA,SR,SMT	176	Vertical Sync/Videoin Vsync_601
YUV7	Inout 4MA,SR,SMT	177	Video data output bit 7/Videoin Data PortB 3
HSYN	Inout 4MA,SR,SMT	179	Horizontal sync/ Vido in Hsync_601
SPMCLK	Input	180	Audio DAC master clock of SPDIF input/Videoin Data PortB 4
SPDATA	Input	181	Audio data of SPDIF input/Vidoin Data PortB 5
SPLRCK	Input	183	Audio L/R channel clock of SPDIF input/Videoin Data PortB 6
SPBCK	Input	184	Audio bit clock of SPDIF input/Videoin Data PortB 7
XTALO	Output	186	Crystal Output
XTALI	Input	187	Crystal Input
PRST	Input PD,SMT	188	Power on reset input, active high
VFO13	Output	190	The 1st,3rd header VFO pulse output
IDGATE	Output	191	Header detect signal output
UDGATE	Output	193	DVD_RAM recording data gate signal output
WOBSI	Input	194	Wobble signal input
SDATA	Output	195	RF serial data output
SDEN	Output	196	RF serial data latch enable
SLCK	Output	197	RF serial clock output
BDO	Input	198	Flag of defect data input status
ADCVSS	Ground	199	Ground pin for ADC circuitry
ADIN	Analog Input	200	General A/D input
RFSUBI	Analog Input	201	RF subtraction signal input terminal
TEZISLV	Analog Input	202	Tracking error zero crossing low pass input
TEI	Analog Input	203	Tracking error input
CSO	Analog Input	204	Central servo input
FEI	Analog Input	205	Focus error input
RFLEVEL	Analog Input	206	Sub beam add input or RFRP low pass input
RFRP_DC	A Input	207	RF ripple detect input
RFRP_AC	Analog Input	208	RF ripple detect input(through AC coupling)
HRFZC	Analog Input	209	High frequency RF ripple zero crossing
PWMVREF	A Input	210	A reference voltage input for PWM circuitry. Atypical value of 4.0 v
PWM2VREF	A Input	211	A reference voltage input for PWM circuitry. Atypical value of 2.0 v
ADCVDD3	Power	212	3.3 power pin for ADC circuitry
RFDTSLVP	Analog Output	213	Positive RF data slicer level output
RFDTSLVN	Analaog Output	214	Negative RF data slicer level output
RFIN	Analog Input	215	Negative input of RF differential signal
RFIP	Analog Input	216	Positive input of RF differential signal

2.1 SYSTEM BLOCK DIAGRAM

A sample system block diagram for the MT1379 DVD player board design is shown in the following figure:



3. AUDIO OUTPUT

The MT1379 supports two-channel and six-channel analog audio output. In a system configuration with six analog outputs, the front left and right channels can be configured to provide the stereo (2 channel) outputs and Dolby Surround, or the left and right front channels for a 5.1 channel surround system.

The MT1379 also provides digital output in S/PDIF format. The board supports both optical and coaxial SPDIF outputs.

4. AUDIO DACS

The MT1379 supports several variations of an I^2S type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or LSB first) is possible using the MT1379 internal configuration registers. The I^2S format uses four stereo data lines and three clock lines. The I^2S data and clock lines can be connected directly to one or more audio DAC to generate analog audio output.

The two-channel DAC is an AKM AK4382A. The DACs support up to 192kHz sampling rate.

The outputs of the DACs are differential, not single ended so a buffering circuit is required. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering.

5 .VIDEO INTERFACE

5.1 Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the MT1379. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4: 2:2 to YUV4: 2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Video Post-Processing

The MT1379 video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

6. FLASH MEMORY

The decoder board supports 70ns Flash memories. Currently 4 configurations are supported:

FLASH_512K_8b
FLASH_1024K_8b
FLASH_512Kx2_8b
FLASH_512Kx2_16b

The MT1379 permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

7. SERIAL EEPROM MEMORY

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

8. AUDIO INTERFACE AUDIO SAMPLING RATE AND PLL COMPONENT CONFIGURATION

The MT1379 audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I^2S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I^2S format while six channels Dolby Digital (5.1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I^2S interface supports the 112, 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I^2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the MT1379 supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The MT1379 incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock. The MCLK pin is for the audio DAC clock and can either be an output from or an input to the MT1379. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the MT1379 based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

9. FRONT PANEL

9.1 VFD CONTROLLER

The VFD controller is a NEC uPD16311. This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix. The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The MT1379 can control this chip directly using PIO pins or can allow the front panel PIC to control the VFD.

10. CONNECTORS

10.1 SCART CONNECTORS

Pinout of the scart connector:

1 → Audio Right Out
2 → Audio Right In
3 → Audio Left / Monu Out
4 → Audio Gnd
5 → Blue Gnd
6 → Audio Left / Mono In
7 → Blue
8 → Control Voltage
9 → Green Gnd
10 → Comms Data 2
11 → Green
12 → Comms Data 1
13 → Red Gnd
14 → Comms Data Gnd
15 → Red
16 → Fast Blanking
17 → Video Gnd
18 → Fast Blanking Gnd
19 → Composite Video In
20 → Composite Video Out
21 → Shield

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded co-ax cable become essential.

Scart Signals:

Audio signals
0.5V RMS, <1K output impedance, >10K input impedance.

Red, Green, Blue
0.7Vpp ±2dB, 75R input and output impedance. Note that the Red connection (pin 20) can alternatively carry the S-Video Chrominance signal, which is 0.3V.
Composite Video / CSync
1Vpp including sync, ±2dB, 75R input and output impedance.Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR 405.1 (625-line TV)

Fast Blanking
75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

0 to 0.4V: TV is driven by the composite video input signal (pin 19). Left unconnected, it is pulled to 0V by its 75R termination.

1V to 3V: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 100R forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

Control Voltage

0 to 2V = TV, Normal.
5 to 8V = TV wide screen
9.5 to 12V = AV mode

11. CIRCUIT DESCRIPTION

11.1 POWER SUPPLY:

- Socket PL1 is the 220VAC input.
- 2.5A fuse F1 is used to protect the device against short circuit.
- Line filters and capacitors L1, C1, L5 and L6 are used to block the parasitic coming from the mains. They also prevent the noise, produced in the circuit, from being injected to the line.
- Voltage is rectified by using diodes D1, D2, D3 and D4. Using capacitor C3 (470μf) a DC voltage is produced. (310- 320VDC).
- The current in the primary side of the transformer TR3 comes to the SMPS IC (IC3 TOP223Y). The SMPS IC has a three-pin TO-220 case and a cooler is mounted on it. It has a built-in oscillator, overcurrent and overvoltage protection circuitry and runs at 100kHz. It starts with the current from the primary side of the transformer and follows the current from the feedback winding.
- Voltages on the secondary side are as follows: -22V, -12V, 3.3V, 5V, 15V.
- D14 TL431 is a constant current regulator. TL431 watches the 5 volts and supplies the required current to IC2. There are a LED and a photo transistor in IC2. The LED inside the IC2 transmits the value of the current from D14 to phototransistor. Depending on the current gain of the phototransistor IC3 keeps the voltage on the 5-volt-winding constant.
- Adjustable voltage regulator IC5 (LM317) supplies 12 Volts.
- When the device enters stand-by mode, transistor Q2 starts to conduct and pulls the adjust pin of IC5 to ground, where this cuts 12Volts off.
- –22 Volts is used to feed the VFD (Vacuum Fluorescent Display) driver IC on the front panel.
- Transistor Q4 and zener diode D14 are used to regulate +12 Volts. This voltage is used to feed op-amps on the back panel.

11.2 FRONT PANEL:

- All the functions on the front panel are controlled by U7 (MT1379) on the mainboard.
- U7 sends the commands to IC2 uPD16311 via socket PL1 (pins 3,4 and 5).
- There are 16 keys scanning function, 2 LED outputs, 1 Stand-by output and VFD drivers on IC2.
- Pin 52 is the oscillator pin and is connected via R5 56K.
- LED D6 is red in stand-by mode and green when the device is on. When entering stand-by mode, pin 48 goes HIGH (+5V) and controls the transistor Q2 on the power board.
- Vacuum fluorescent display MD2 is specially designed for DVD.
- The scanned keys are transmitted via IC2 pin 5 and 6 to U1 on the mainboard.
- IR remote control receiver module IC3 (TSOP1836) sends the commands from the remote control directly to U1.
- Socket PL2 carries the VFD filament voltage and –22 Volts.

11.3 BACK PANEL:

- There are 1 SCART connector (PL4), 2 pieces RCA audio jacks, for audio output, 1 coaxial digital audio output JK3 and 1 laser digital audio output PL5 on the back panel.
- TOTX176 is used for laser output.
- For coaxial audio output SPDIF is used.
- Q22 .. Q27 transistors are to mute the audio outputs while switching the state of the unit(power on/off)
- There are two op-amps in U14, U16 and U18. They are used for left,right,rear left and right, subwoofer center audio channels. The feedback resistor is amplifying the gain.
- SCART pin 8 controls 16:9 and 4:3 mode using Q28,Q29 and Q30.
- When the pin8 output of the scart becomes 5 Volts, 4:3 mode is selected and 16:9 mode is selected when this output becomes 0. The circuit is adjusted to output 12 Volts for 4:3 mode and 6 Volts for 16:9 mode.
- Transistors Q28,Q29 and Q30 transmit these voltages when the device is turned on and cuts them off when it is turned off.
- FBL on pin 16 transmits 5 Volts via transistors Q12 and Q14 when the device is on.
- Socket PL2, which is coming from the mainboard, transmits RED, GREEN, BLUE and VIDEO signals to SCART over the buffer stage.
- LUMA and CHROMA signals of S-Video are transmitted to S-Video socket via transistors Q11 and Q13 respectively.

12.SOFWARE UPTATE

12.1 Version Page (Hidden Menu)

To see Version Page;
- Press DISPLAY button from remote
- Press “1”-“3”-“5”-“7” at Setup Menu

- Setup Menu screen refresh and “Version” selection can be seen under “Preferences Setup”
- Select “Version” for Version Page
- First 6 lines contains current VERSION information.1st and 5th line is for customers
  Other lines (Sub-Ver, 8032, Servo, Risc) for factory use only;

  1st line contains build information example: 02.01.**EF65**
  5th line contains hardware option example: **A6AO.bin**
  7th line contains **Region Code (Management)**

  - Press “DISPLAY” button on remote control to exit hidden menu.

5th line also shows CD update file name. It defines also Hardware options.

12.2 Build Names for Hardware Options

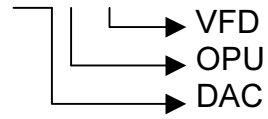
DVD5500 MTK Concept has 3 different hardware option:

1. 2 OPU Option
2. 2 VFD Option
3. 4 DAC Option

This means there are 16 different software.

There is a naming standard for software builds according to
player’s hardware options like;

X X X X. bin



VFD Type: **O** = Old VFD / **N** = New small VFD
OPU Type: **A** = ASA SANYO HD60 / **F** = FUSS HITACHI HOP 1200
DAC Type: **A6** = AK4356 / **A2** = AK4382 / **P6** = PCM1606 / **C2** = CS4392

Example:
A6AO.bin = AK4356, ASA, OLD VFD
C2FN.bin = CS4392 ,ASA, NEW small VFD

Service CD should contains following 16 files;

A6AO.bin	A6AN.bin	A6FO.bin	A6FN.bin
P6AO.bin	P6AN.bin	P6FO.bin	P6FN.bin
A2AO.bin	A2AN.bin	A2FO.bin	A2FN.bin
C2AO.bin	C2AN.bin	C2FO.bin	C2FN.bin

Note: Update CD should have no volume ID.

12.3 CD UPTADE PROCEDURE:

1) Any Player can be updated automatically with Update CD which contains proper files (see Service Cd.Jpg)
2) Burn up CD within proper files
2) There should be no Volume Name for CD
3) Open Tray and place update CD

4) You can see "Upgrade File Detected. Press Play to start" OSD message
5) Press Play button to start upgrade
6) You can see "File copying" OSD message for a few second
7) Tray is open automatically
8) No need for CD in tray;Take it from tray.

9) During upgrade procedure "CD upgrade start, Please wait.." indicator at OSD, and "UPG" indicator at VFD
10) Upgrade procedure takes about a few minutes, please wait if tray is open.
11) When CD update is finished tray is closed, screen is refreshed, update is finished.

12) To see Version Page;
- Press DISPLAY button from remote
- Press “1”-“3”-“5”-“7” at Setup Menu
- Setup Menu screen refresh and “Version” selection can be seen under “Preferences Setup”
- Select “Version”or version Page
- 1st line contains Build number like EFXX
- 5th line contains hardware options
- Press “DISPLAY” button on remote control to exit hidden menu.

12.4 Region Management

At version Page by using arrow keys you can change region.