1 Applications

This present specifications are applied to IC MT1389L.

2 Type

MT1389L

3 Usage

Single Chip IC for DVD Player

4 Structure

0.16um CMOS process, Silicon material, Monolithic IC, 128pin LQFP, 3.3/1.8 Dual operation voltages.

5 Function

5-1 General Description

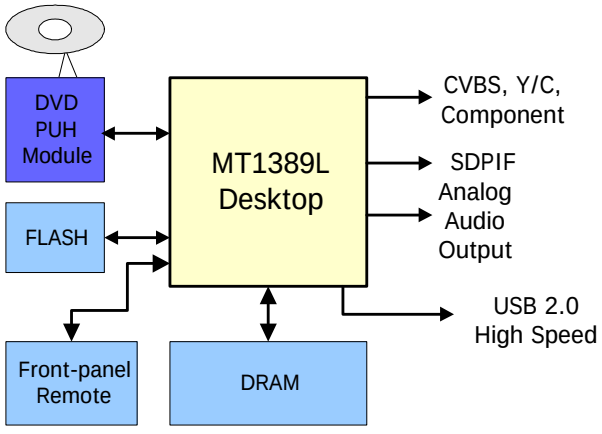
MediaTek MT1389L is a cost-effective DVD system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high quality TV encoder and state-of-art de-interlace processing. The MT1389L enables consumer electronics manufacturers to build high quality, USB2.0, MS/SD/MMC reader, feature-rich DVD players, portable DVD players or any other home entertainment audio/video devices.

World-Leading Technology: Based on MediaTek's world-leading DVD player SOC architecture, the MT1389L is the New generation of the DVD player SOC. It integrates the MediaTek 3rd generation front-end digital RF amplifier and the Servo/MPEG AV decoder.

Rich Feature for High Valued Product: To enrich the feature of DVD player, the MT1389 equips a simplified MPEG-4 advanced simple profile (ASP) video decoder to fully support the DivX[1] Home Theater profile. It makes the MT1389-based DVD player be capable of playback MPEG-4 content which become more and more popular.

Incredible Audio/Video Quality: The progressive scan of the MT1389L utilized advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It also supports a 3:2 pull down algorithm to give the best film effect. The 108MHz/12-bit video DAC provides users a whole new viewing experience. Built-in 6ch audio DACs and 2ch audio ADCs could give the variable function solutions.

High Performance Memory Storage Device: As the core of Portable DVD players need more capability to support current multimedia contents. The MT1389L provides the interface for the 3-in-1 card reader, which supports Memory-Stick, Secure Digital Memory Card, and MultiMediaCard, to connect with the mainstream digital camera FLASH cards. For the USB application, we adopt **USB2.0 High speed** specification to reach rich-contents transference. **USB 2.0 High speed** will support for high-speed devices. **USB 2.0 High Speed** is suitable for high-performance devices such as high-density storage devices. In addition, **USB 2.0 High Speed** supports old USB 1.0/1.1 software and peripherals, offering impressive and even better compatibility to customers.



DVD Player System Diagram Using MT1389L

Key Features

- RF/Servo/MPEG Integration
- DivX Home Theater Level MPEG4 ASP Video decoder
- Support Nero-Digital
- Support DivX Ultra
- High Performance Audio Processor
- Progressive Scan
- 108MHz/12-bit, 4 CH TV Encoder
- Internal 6CH Audio DAC
- Internal 2CH Audio ADC
- USB2.0 High Speed (Host/Device)
- 3-in-1 MS/SD/MMC reader

Applications

Standard DVD Players

[1] DivX is a trademark of DivXNetworks

[2] **USB High Speed** : 480Mbit/sec. USB Full Speed : 12Mbit/sec.

5-2 Key Features

- RF/Servo/MPEG Integration
- Embedded 6ch Audio DAC
- Embedded 2ch Audio ADC for Karaoke
- High Performance Audio Processor
- High Performance Progressive Video Processor
- Support Nero-Digital
- Support DivX Ultra
- High Quality 108MHz/12-bit, 4 CH TV Encoder
- USB 2.0 High-Speed

5-3 Applications

- Standard DVD Players
- DVD Players Home Theater Application
- Portable DVD Players
- TV/DVD Combo Systems

5-4 General Feature lists

■ **Super Integration DVD player single chip**
- High performance analog RF amplifier
- Servo controller and data channel processing
- MPEG-1/MPEG-2/JPEG video
- Dolby AC-3/DTS Decoder
- Unified memory architecture
- Versatile video scaling & quality enhancement
- OSD & Sub-picture
- Built-in clock generator
- Built-in high quality TV encoder
- Built-in progressive video processor
- Audio effect post-processor
- Built-in 5.1-ch Audio DAC
- Built-in 2-ch Audio ADC for Karaoke
- USB 2.0 High-Speed
- MS/SD/MMC 3-in-1 card reader

■ **Speed Performance on Servo/Channel Decoding**
- DVD-ROM up to 4XS
- CD-ROM up to 24XS

■ **Channel Data Processor**
- Digital data slicer for small jitter capability
- Built-in high performance data PLL for channel data demodulation
- EFM/EFM+ data demodulation
- Enhanced channel data frame sync protection & DVD-ROM sector sync protection

■ **Servo Control and Spindle Motor Control**
- Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
- Built-in ADCs and DACs for digital servo control
- Provide 2 general PWM
- Tray control can be PWM output or digital output

■ **Embedded Micro controller**
- Built-in 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 1024-bytes on-chip RAM
- Up to 2M bytes FLASH-programming interface
- Supports 5/3.3-Volt. FLASH interface
- Supports power-down mode
- Supports additional serial port

■ **DVD-ROM/CD-ROM Decoding Logic**
- High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
- Automatic sector Mode and Form detection
- Automatic sector Header verification
- Decoder Error Notification Interrupt that signals various decoder errors
- Provide error correction acceleration

■ **Buffer Memory Controller**
- Supports 16Mb/32Mb/64Mb SDRAM
- Supports 16-bit SDRAM data bus
- Provides the self-refresh mode SDRAM
- Block-based sector addressing

■ **Video Decode**
- Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
- Decodes MPEG-4 Advanced Simple Profile
- Support DivX 3.11/4.x/5.x Home Theater Profile
- Support Nero-Digital
- Support DivX Ultra
- Smooth digest view function with I, P and B picture decoding
- Baseline, extended-sequential and progressive JPEG image decoding
- Support CD-G titles

■ **Video/OSD/SPU/HLI Processor**
- Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
- 65535/256/16/4/2-color bitmap format OSD,
- 256/16 color RLC format OSD
- Automatic scrolling of OSD image

■ **Audio Effect Processing**
- Dolby Digital (AC-3)/EX decoding
- DTS/DTS-ES decoding
- MPEG-1 layer 1/layer 2 audio decoding

- High Definition Compatible Digital (HDCD)
- Windows Media Audio (WMA)
- Dolby ProLogic II
- Concurrent multi-channel and downmix out
- IEC 60958/61937 output
  - PCM / bit stream / mute mode
  - Custom IEC latency up to 2 frames
- Pink noise and white noise generator
- Karaoke functions
  - Microphone echo
  - Microphone tone control
  - Vocal mute/vocal assistant
  - Key shift up to +/- 8 keys
  - Chorus/Flanger/Harmony/Reverb
- Channel equalizer
- 3D surround processing include virtual surround and speaker separation

■ **TV Encoder**

- Four 108MHz/12bit DACs
- Support NTSC, PAL-BDGHINM, PAL-60
- Support 525p, 625p progressive TV format
- Automatically turn off unconnected channels
- Support PC monitor (VGA)
- Support Macrovision 7.1 L1, Macrovision 525P and 625P
- CGMS-A/WSS
- Closed Caption

■ **Progressive Scan Video**

- Automatic detect film or video source
- 3:2 pull down source detection
- Advanced Motion adaptive de-interlace
- Minimum external memory requirement

■ External Interface

- USB2.0 High Speed (Host/Device)
- Memory-Stick, Secure Digital Memory Card, and MultiMediaCard Interface

■ **Outline**

- 128-pin LQFP package
- 3.3/1.8-Volt. Dual operating voltages

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5-5 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- 4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
Analog Interface (66)				
125	RFIP		Analog Input	AC coupled DVD RF signal input RFIP
126	RFIN	OPOUT	Analog Input	AC coupled DVD RF signal input RFIN
127	RFG	OPINP	Analog Input	Main beam, RF AC input path
128	RFH	OPINN	Analog Input	Main beam, RF AC input path
1	RFA		Analog Input	RF main beam input A
2	RFB		Analog Input	RF main beam input B
3	RFC		Analog Input	RF main beam input C
4	RFD		Analog Input	RF main beam input D
5	RFE		Analog Input	RF sub beam input E
6	RFF		Analog Input	RF sub beam input E
7	AVDD18_2		Analog power	Analog 1.8V power
8	AVDD33_1		Analog Power	Analog 3.3V power
9	XTALI		Input	27MHz crystal input
10	XTALO		Output	27MHz crystal output
11	AGND33		Analog Ground	Analog Ground
12	V20		Analog output	Reference voltage 2.0V
13	V14		Analog output	Reference voltage 1.4V
14	REXT		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS
15	MDI1		Analog Input	Laser power monitor input

Pin	Main	Alt.	Type	Description
16	MDI2		Analog Input	Laser power monitor input
17	LDO1		Analog Output	Laser driver output
18	LDO2		Analog Output	Laser driver output
19	AVDD33_2		Analog Power	Analog 3.3V power
20	DMO		Analog Output	Disk motor control output. PWM output
21	FMO		Analog Output	Feed motor control. PWM output
22	TRAY_OPEN		Analog Output	Tray PWM output/Tray open output
23	TRAY_CLOSE		Analog Output	Tray PWM output/Tray close output
24	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator
25	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
26	FG	GPIO2	Analog	1) Motor Hall sensor input 2) GPIO
27	USB_DP		Analog Inout	USB port DPLUS analog pin
28	USB_DM		Analog Inout	USB port DMINUS analog pin
29	VDD33_USB		USB Power	USB Power pin 3.3V
30	VSS33_USB		USB Ground	USB ground pin
31	PAD_VRT		Analog Inout	USB generating reference current
32	VDD18_USB		USB Power	USB Power pin 1.8V
95	DACVDDC		Power	3.3V power pin for video DAC circuitry
96	VREF		Analog	Bandgap reference voltage
97	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
98	DACVSSC		Ground	Ground pin for video DAC circuitry
99	CVBS		Analog	Analog composite output
100	DACVDDB		Power	3.3V power pin for video DAC circuitry
101	DACVDDA		Power	3.3V power pin for video DAC circuitry
102	Y/G		Analog	Green, Y, SY, or CVBS
103	B/CB/PB		Analog	Blue, CB/PB, or SC

Pin	Main	Alt.	Type	Description
104	R/CR/PR		Analog	Red, CR/PR, CVBS, or SY
105	AADVSS		Ground	Ground pin for 2ch audio ADC circuitry
106	AKIN2		Analog	1) Audio ADC input 2 2) MS_CLK set B 3) MCDATA 4) Audio Mute 5) HSYN/VSYN output 6) C5 7) GPIO
107	ADVCM		Analog	1) 2ch audio ADC reference voltageC 2) C6 3) GPIO
108	AKIN1		Analog	1) Audio ADC input 1 2) MS_D0 set B 3) Audio Mute 4) HSYN/VSYN output 5) C7 6) GPIO
109	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
110	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
111	APLLCAP		Analog InOut	APLL external capacitance connection
112	ADACVSS2		Ground	Ground pin for audio DAC circuitry
113	ADACVSS1		Ground	Ground pin for audio DAC circuitry
114	ARF / LFE	GPIO	Analog Output	1) Audio DAC sub-woofer channel output 2) While internal audio DAC not used: a. ACLK b. GPIO
115	ARS	GPIO	Analog Output	1) Audio DAC right Surround channel output 2) While internal audio DAC not used: a. ABCK b. GPIO

Pin	Main	Alt.	Type	Description
116	AR	GPIO	Analog Output	1) Audio DAC right channel output 2) While internal audio DAC not used: a. SDATA2 b. GPIO c. RXD2
117	AVCM		Analog	Audio DAC reference voltage
118	AL	GPIO	Analog Output	1) Audio DAC left channel output 2) While internal audio DAC not used: a. SDATA1 b. GPIO c. RXD1
119	ALS	GPIO	Analog Output	1) Audio DAC left Surround channel output 2) While internal audio DAC not used: a. ALRCK b. GPIO
120	ALF /CENTER	GPIO	Analog Output	1) Audio DAC center channel output 2) While internal audio DAC not used: a. ASDATA0 b. GPIO
121	ADACVDD1		Analog Power	3.3V power pin for audio DAC circuitry
122	ADACVDD2		Analog Power	3.3V power pin for audio DAC circuitry
123	AVDD18_1		Analog Power	Analog 1.8V power
124	AGND18		Analog Ground	Analog Ground
General Power/Ground (7)				
54, 90	DVDD18		Power	1.8V power pin for internal digital circuitry
79	DVSS18		Ground	1.8V Ground pin for internal digital circuitry
50, 68,84	DVDD33		Power	3.3V power pin for internal digital circuitry
60	DVSS		Ground	3.3V Ground pin for internal digital circuitry
Micro Controller , Flash Interface and GPIO(12)				
33	GPIO3	INT#	InOut 8mA, SR PD, SMT	1) General purpose IO 3 2) Microcontroller external interrupt 1
34	GPIO4		InOut 4mA, PD	General purpose IO 4

Pin	Main	Alt.	Type	Description
35	GPIO6		InOut 4mA, PD	General purpose IO 6
36	SF_CS_		InOut 8mA, SR PU, SMT	Serial Flash Chip Select
37	SF_DO		InOut 8mA, SR PD, SMT	Serial Flash Dout
38	SF_DI		InOut 8mA, SR PU, SMT	Serial Flash Din
39	SF_CK		InOut 8mA, SR PD, SMT	Serial Flash Clock
40	UP1_6	SCL	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
41	UP1_7	SDA	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
42	ICE		Input PD, SMT	Microcontroller ICE mode enable
43	PRST#		Input PU, SMT	Power on reset input, active low
44	IR		Input SMT	IR control signal input
Dram Interface (37) (Sorted by position)				
45	RD0		InOut, 4mA	DRAM data 0

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Pin	Main	Alt.	Type	Description
46	RD1		InOut 4mA	DRAM data 1
47	RD2		InOut 4mA	DRAM data 2
48	RD3		InOut 4mA	DRAM data 3
49	RD4		InOut 4mA	DRAM data 4
51	RD5		InOut 4mA	DRAM data 5
52	RD6		InOut 4mA	DRAM data 6
53	RD7		InOut 4mA	DRAM data 7
55	DQM0		InOut 4mA, PD	Data mask 0
56	RD15		InOut 4mA	DRAM data 15
57	RD14		InOut 4mA	DRAM data 14
58	RD13		InOut 4mA	DRAM data 13
59	RD12		InOut 4mA	DRAM data 12
61	RD11		InOut 4mA	DRAM data 11
62	RD10		InOut 4mA	DRAM data 10
63	RD9		InOut 4mA	DRAM data 9
64	RD8		InOut 4mA	DRAM data 8

Pin	Main	Alt.	Type	Description
65	DQM1		InOut 4mA, PD	Data mask 1
66	RCLK		InOut 4mA, PD	Dram clock
67	RA11		InOut 4mA, PD	DRAM address bit 11
69	RA9		InOut 4mA, PD	DRAM address 9
70	RA8		InOut 4mA, PD	DRAM address 8
71	RA7		InOut 4mA, PD	DRAM address 7
72	RA6		InOut 4mA, PD	DRAM address 6
73	RA5		InOut 4mA, PD	DRAM address 5
74	RA4		InOut 4mA, PD	DRAM address 4
75	RWE#		Output 4mA, PD	DRAM Write enable, active low
76	CAS#		Output 4mA, PD	DRAM column address strobe, active low
77	RAS#		Output 4mA, PD	DRAM row address strobe, active low
78	BA0		InOut 4mA, PD	DRAM bank address 0
80	BA1		InOut 4mA, PD	DRAM bank address 1
81	RA10		InOut 4mA, PD	DRAM address 10

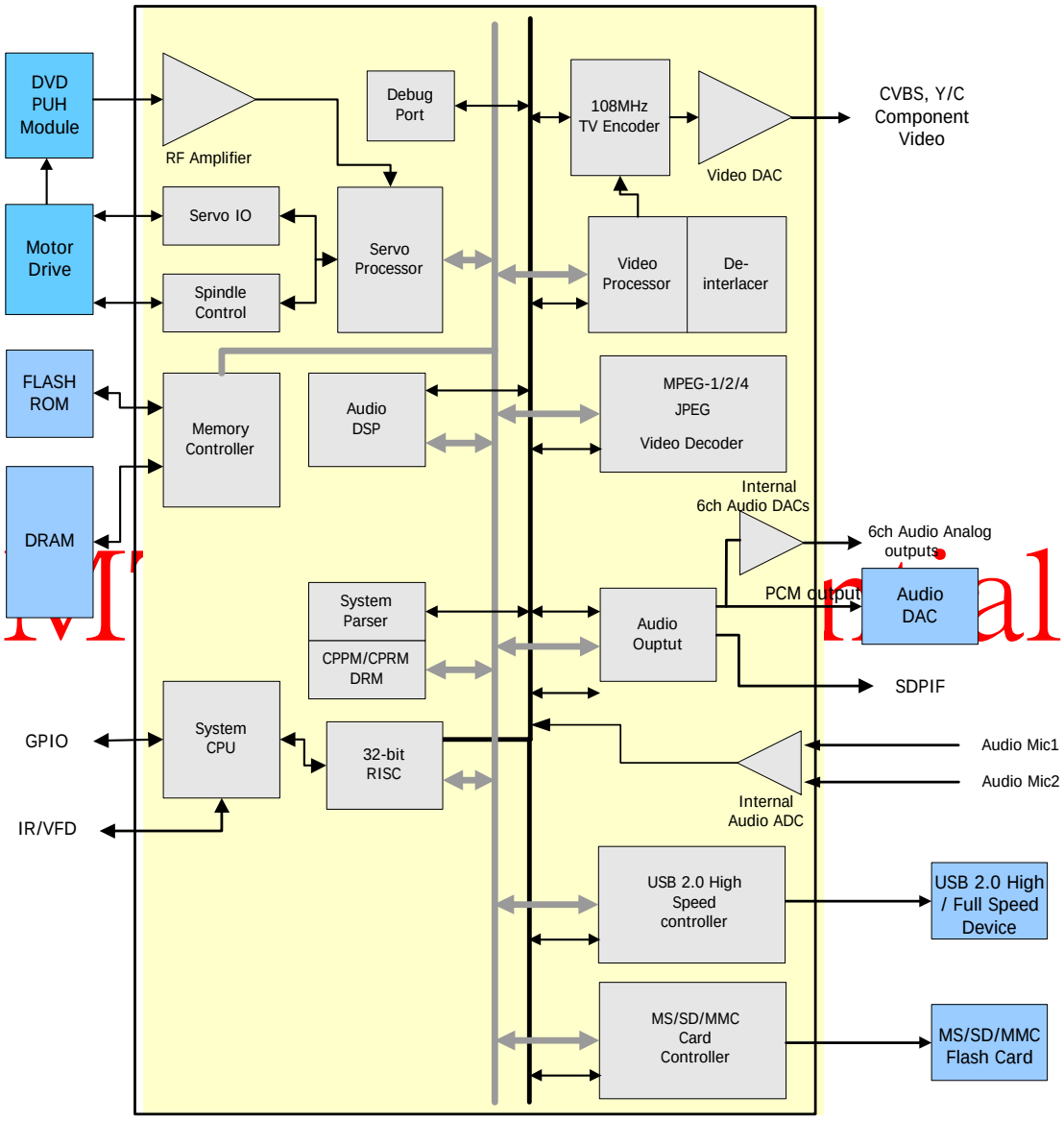
Pin	Main	Alt.	Type	Description
82	RA0		InOut 4mA, PD	DRAM address 0
83	RA1		InOut 4mA, PD	DRAM address 1
85	RA2		InOut 4mA, PD	DRAM address 2
86	RA3		InOut 4mA, PD	DRAM address 3
87	GPIO7	CKE	InOut 4mA, PD	1) GPIO 7 2) Dram Clock Enable 3) MS_CLK set A 4) Audio Mute 5) HSYN/VSYN input 6) C0
			GPIO (6)	
88	GPIO8		InOut 4mA, PD	1) GPIO8 2) MS_BS set A 3) SD_CLK set A 4) ASDATA2 5) ACLK 6) Audio Mute 7) HSYN/VSYN input 8) C1
89	GPIO9		InOut 4mA, PU	1) GPIO9 2) MS_D0 set A 3) SD_CMD set A 4) ASDATA1 5) ABCK 6) C2 7) RXD1

Pin	Main	Alt.	Type	Description
91	GPIO10		InOut 4mA, PD	1) GPIO10 2) SD_CLK set B 3) SD_D0 set A 4) ASDATA0 5) ALRCK 6) HSYN/VSYN output 7) C3 8) TXD1
92	GPIO11		InOut 4mA, PD	1) GPIO11 2) SD_CMD set B 3) MS_BS set B 4) Audio Mute 5) HSYN/VSYN output 6) C4
93	SPDIF	GPIO12	InOut 2mA, PD	0) SPDIF output 1) GPIO12
94	GPIO13		InOut 4mA, PD	1) GPIO13 2) SD_D0 set B 3) ALRCK 4) Audio Mute 5) YUVCLK

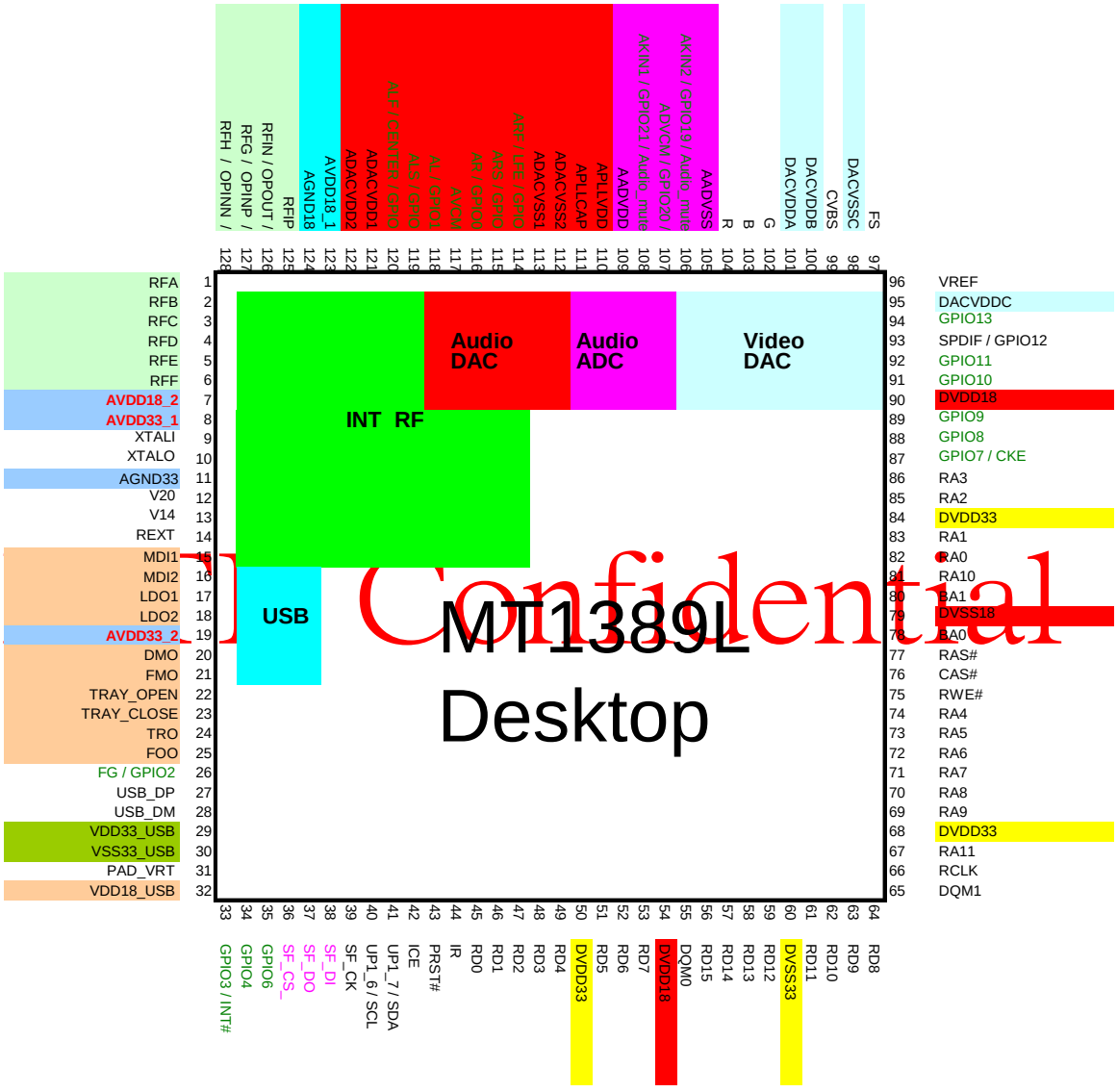
Note:

1. The Main column is the main function, Alt. means alternative function.
2. The multi-function GPIO pins are set to green characters.

5-6 Functional Block



6 Pin Assignment



7 Absolute Maximum Ratings

Symbol	Parameters	Value	Unit
VDD3	3.3V Supply voltage	-0.3 to 3.6	V
VDD2	1.8V Supply voltage	-0.3 to 2.1	V
VDDA	Analog Supply voltage	-0.3 to 3.6	V
V_{IN}(3.3V)	Input Voltage (3.3V IO)	-0.3 to 3.63	V
V_{IN}(5V-tolerance)	Input Voltage (5V-tolerance IO)	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.3 to VDD3+0.3	V
T_{STG}	Storage Temperature	-45 to 150	°C

8 Recommend Operation Condition

Symbol	Parameters	Min	Typ	Max	Unit
T_{OP}	Operating Temperature	0		70	°C
T_J	Junction Operation Temp.	0	25	115	°C
VDD3	3.3V Supply voltage	3.0	3.3	3.6	V
VDD2	1.8V Supply voltage	1.7	1.8	2.0	V
VDDA	Analog Supply voltage	3.0	3.3	3.6	V
V_{IH} (1.8V)	Input voltage high (1.8V IO)	1.05	-	-	V
V_{IL} (1.8V)	Input voltage low (1.8V IO)	-	-	0.69	V
V_{IH} (3.3V)	Input voltage high (3.3V IO)	2.0	-	-	V
V_{IL} (3.3V)	Input voltage low (3.3V IO)	-	-	0.8	V
I_{IH}	High level input current			10	UA
I_{IL}	Low level input current	-10			UA
P_D	Power dissipation		1.5		W
P_{DOWN}	Power down mode			0.1	W
fclk	Input frequency of clock		27		MHz

9 Electrical Characteristics

9-1 DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{OH} (1.8V)	Output voltage high (1.8V IO) (*I_{OH} = 2 ~ 16mA)	1.22	-	-	V
V_{OL} (1.8V)	Output voltage low (1.8V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
V_{OH} (3.3V)	Output voltage high (3.3V IO) (*I_{OH} = 2 ~ 16mA)	2.4	-	-	V
V_{OL} (3.3V)	Output voltage low (3.3V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
Rpu	Pull-up Resistance	40	75	190	KΩ
Rpd	Pull-down Resistance	40	75	190	KΩ
FOO_{OFF}	Offset voltage between FOO zero output and V_{REF}	-50	0	50	mV
TRO_{OFF}	Offset voltage between TRO zero output and V_{REF}	-40	0	40	mV
DMO_{OFF}	Offset voltage between DMO zero output and V_{REF}	-30	0	30	mV

Note * : The driving current of some IO pad are programmable according to the different application and environment . All setting will be defined according to the F/W progress and test result.

9-2 Built-in Audio-DAC Characteristics

Note *: All parameters is measured on MediaTek's DVD player reference DVD board, the actual performance depends on different PCB design.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{out}	Output swing level: Digital i/p level =0 dBFS , ADACVDD =3.3V (V_{out} = 1.0 * ADACVDD / 3.3)	0.9	1.0	1.1	V_P
Ro	Output impedance @ 1kHz		50	100	
R_{L_min}	Minimum resister load	5			K
C_{L_max}	Maximum capacitor load			20	PF
S/(THD+N)	S/(THD+N) @ 0 dBFS; f_{in} = 1kHz; Fs = 48kHz, A-weighted		90		dBr(A)
DR	Dynamic Range		88		dBr(A)
SNR	Signal to noise ratio; A-weighted		95		dBr(A)
Channel Separation	Close-talk of Left and Right Channel		85		dB

9-3 Built-in Video-DAC Specifications

Input Codes for Video Application:

	NTSC	NTSC w/setup	525_I	525_I w/setup	525_P
WHITE (235)	Programable,	Programable,	Programable,	Programable,	Programable,

	Current setting: 3297	Current setting: 3297	Current setting: 3297	Current setting: 3297	Current setting: 3290
BLACK (16)	960	1120	960	1120	1008
PEDESTAL	960	960	960	960	1008
SYNC TIP	64	64	64	64	64

	525_P w/s	**PAL**	**625_I**	**625_P**	**RGB**
WHITE (235)	---	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 2282
BLACK (16)	---	1008	1008	1008	0
PEDESTAL	---	1008	1008	1008	-
SYNC TIP	---	64	64	64	-

9-4 Video Output Voltage Level:

High Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 2.2 KOhm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3237 V, R_{LOAD} = 150 Ohm

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

Low Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 560 Ohm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3 V, R_{LOAD} = 37.5 Ohm (75 Ohm || 75 Ohm)

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

9-5 Video DAC DC Electrical Characteristics

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(Operating Free-Air Temperature, AVDD 3.3V, DVDD = 3.3V).

Analog Output		**MIN**	**TYP**	**MAX**	**UNIT**
Full Scale Output Current CVBS/Y/C/R/G/B	(low impedance mode)	33.6	34.6	34.9	mA
Full Scale Output Current CVBS/Y/C/R/G/B	(high impedance mode)	8.40	8.65	8.73	mA
LSB current CVBS/Y/C/R/G/B	(low impedance mode)	32.8	33.8	34.1	uA
LSB current CVBS/Y/C/R/G/B	(high impedance mode)	8.20	8.45	8.52	uA
DAC-to-DAC Mis-Matching		--	1.28	--	%
Output Compliance		0	--	1.35	V

DAC Output Delay	--	1.5	10	ns
DAC Rise/Fall Time	--	2.1	5	
Voltage Reference				
Reference Voltage Output		1.27		V
Reference Input Current		2.267		MA
Static Performance				
DAC Resolution		12		Bits
DNL Differential Non-Linearity	+/-0.2	*/-0.25	+/-0.3	LSB
INL Integral Non-Linearity	+/-0.35	*/-0.4	+/-0.49	LSB
Dynamic Performance				
Differential Gain		0.8	1.5	%
Differential Phase		0.6	1.5	°
S/N Ratio	70			dB
Power Supply				
Supply Voltage	3.0	3.3	3.6	V

带格式的: 项目符号和编号

3.6 RF specification

Item	Designator	Conditions	Min	Typ	Max	Unit
3.3V POWER			3.00	3.30	3.60	Volts
Power Down Mode		Enable power down	10	27	50	mA
		Chip Reset	90	151	200	mA
Reference Voltage	V20	Force current =0A	1.85	1.99	2.15	Volts
Reference Voltage	VREFO	Force current =0A	1.25	1.39	1.55	Volts
Reference Voltage	V2REFO	Force current =0A	2.65	2.78	2.95	Volts
APC1(CD)	MDI1	0Ah=10 ;APC1 on MDI1=180mV	166	184	202	mV
	LDO1	0Ah=00 ;APC1 off	3.00	3.28		V
	MDI1→LDO1	0Ah=10; APC1 on	212	254	295	V/V
APC2(DVD)	MDI2	0Bh=10 ;APC2 on MDI2=180mV	166	184	202	mV

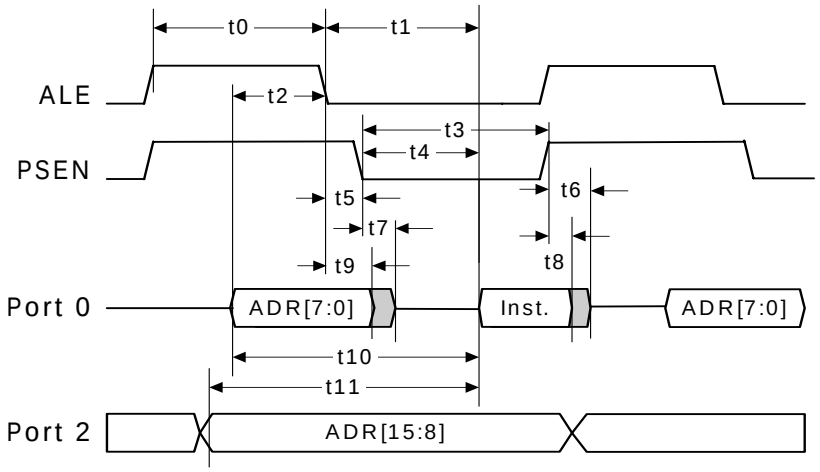
Item	Designator	Conditions	Min	Typ	Max	Unit
	LDO2	0Bh=00 ;APC2 off	3.00	3.28		V
	MDI2→LDO2	0Bh=10; APC2 on High gain	210	265	298	V/V
Focusing Error Gain	MA → FEO	05h=30; low gain With 10KHz Sin Input	7.5	10.3	11.5	dB
Focusing Error Frequency Response	MA → FEO	05h=7C; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	23.9		dB
Focusing Error Common Mode Gain	MA → FEO MB → FEO	05h=3F; low gain With 10KHz Sin Input		-34	-20	dB
Focusing Error H/L Gain	MA → FEO	Toggle 05h bit5 : FELG With 10KHz Sin Input	2.75	2.99	3.25	V/V
Focusing Error offset Adjustment step	Input Floating Measure FEO	Toggle 4Dh : FEOS[6:0]	65	103	140	mV
Focusing Error THD	MA → FEO	05h=7C; low gain With 10KHz Sin Input	30	54		dB
Central Servo Gain	MA → CSO	06h=F0; low gain With 10KHz Sin Input	12.5	14.1	15.5	dB
Central Servo Frequency Response	MA → CSO	06h=FF; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	21.4		dB
Central Servo Common Mode Gain	MA → CSO MB → CSO	06h=F0; low gain With 10KHz Sin Input		-30	-10	dB
Central Servo H/L Gain	MA → CSO	Toggle 06h bit5 : CSOLG With 10KHz Sin Input	2.75	2.97	3.25	V/V
Central Servo offset Adjustment step	Input Floating Measure CSO	Toggle 4Eh : CSOOS[6:0]	65	108	140	mV

Item	Designator	Conditions	Min	Typ	Max	Unit
Central Servo THD	MA → CSO	06h=F0; low gain With 10KHz Sin Input	30	53		dB
Tracking Error Gain	MA → TEO	07h=70; low gain With 10KHz Sin Input	13	15	17	dB
Tracking Error Frequency Response	MA → TEO	07h=70; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	24.2		dB
Tracking Error Common Mode Gain	MA → TEO MB → TEO	07h=7F; low gain With 10KHz Sin Input		-22	-10	dB
Tracking Error H/L Gain	MA → TEO	Toggle 07h bit6, 5 With 10KHz Sin Input	4	5.8	8	V/V
Tracking Error offset Adjustment step	Input Floating Measure TEO	Toggle 4Fh : TEOS[6:0]	65	110	140	mV
Tracking Error THD	MA → TEO	07h=7F; low gain With 10KHz Sin Input	30	42		dB
RFL Gain	MA → LVL	08h=60; low gain With 10KHz Sin Input	-6.5	-4.6	-3.5	dB
RFL Frequency Response	MA → LVL	08h=7F; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	22.7		dB
RFL H/L Gain I	MA → LVL	Toggle 09h bit1 : LVLATN With 10KHz Sin Input	0.3	0.52	0.7	V/V
RFL H/L Gain II	SA → LVL	Toggle 09h bit2 : SBADHG With 10KHz Sin Input	2.5	2.77	3.1	V/V
RFL offset Adjustment step	Input Floating Measure LVL	Toggle 50h : LVLOS[6:0]	65	113	140	mV
RFL THD	MA → LVL	08h=7F; low gain With 10KHz Sin Input	30	44		dB

9-7 Micro Controller Interface

带格式的: 项目符号和编号

Parameter	Symbol	Min.	Max.	Units
Oscillator Frequency	1/Tf	0	23.3	MHz
ALE Pulse Width	T0	1.5Tf-5		ns
ALE Low to Valid Instruction	T1		2.5Tf-20	ns
ALE Low to PSEN Low	T5	0.5Tf-5		ns
Address Valid to ALE Low	T2	0.5Tf-5		ns
Address Hold After ALE Low	T9	0.5Tf-5		ns
PSEN Pulse Width	T3	2.0Tf-5		ns
PSEN Low to Valid Instruction	T4		2.0Tf-20	ns
Input Instruction Hold After PSEN high	T8	0		ns
Input Instruction Float After PSEN high	T6		1.0Tf-5	ns
Port 0 Address to Valid Instruction	T10		3.0Tf-20	ns
Port 2 Address to Valid Instruction	T11		3.5Tf-20	ns
PSEN Low to Address Float	T7		0	ns

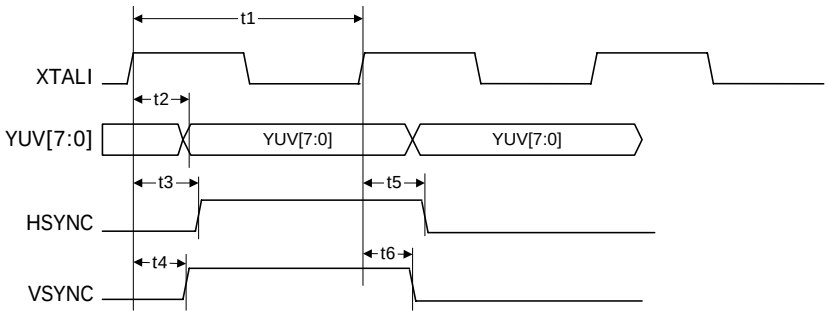


Program Memory Read Cycle Timing Diagram

9-8 Digital Video Output Interface

带格式的: 项目符号和编号

Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/T1		27		MHz
YUV digital output delay	T2			15	ns
HSYNC Rising delay	T3			15	ns
VSYNC Rising delay	T4			15	ns
HSYNC Falling delay	T5			20	ns
VSYNC Falling delay	T6			20	ns

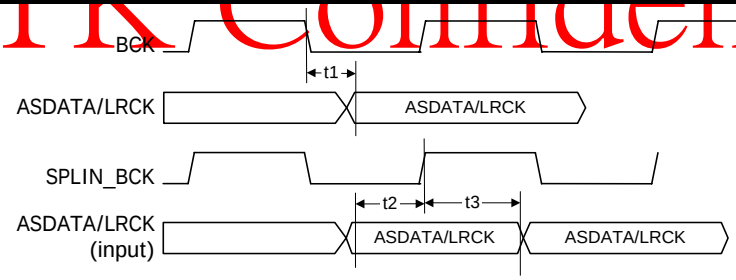


Digital Video Output Interface Timing Diagram

9-9 SPDIF I/O Interface

带格式的: 项目符号和编号

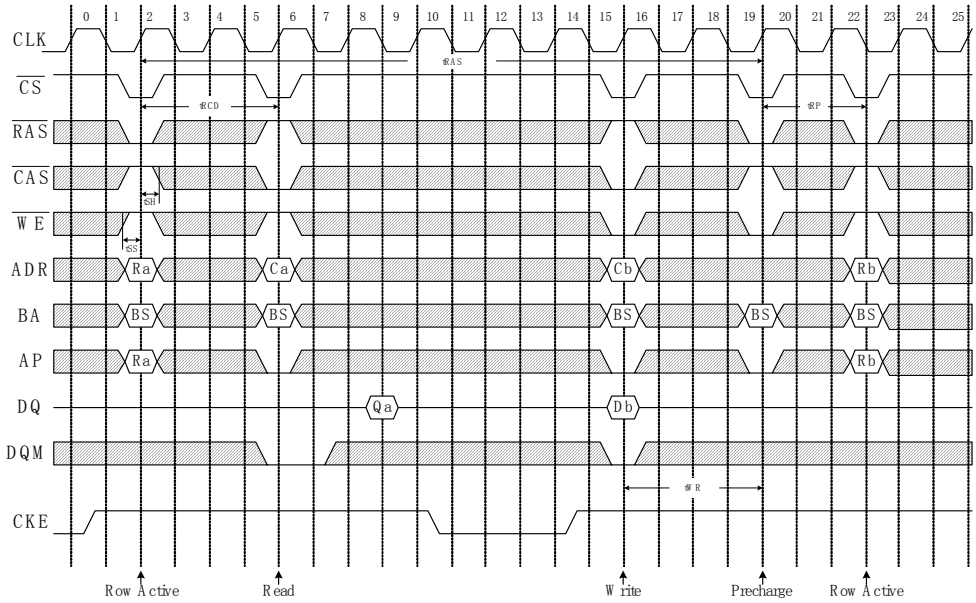
Parameter	Symbol	Min	Typ	Max	Units
BCK negative edge to ASDATA valid	T1	1.0		3.0	ns
ASDATA/LRCK input setup	T2			3.0	ns
ASDATA/LRCK input hold	T3	1.2			ns



SPDIF Input/Output Timing Diagram

9-10 DRAM Interface

带格式的: 项目符号和编号



Parameter		Symbol	-6		-7		-8		Units
			Min	Max	Min	Max	Min	Max	
CLK cycle time	CAS latency = 3	tCC	7.5	-	7.5	-	8	-	ns
	CAS latency = 2		8		10		10		
SDRAM input setup time		tSS	1.5		1.75		2		ns
SDRAM input hold time		tSH	1		1		1		ns
Active to Precharge command period		tRAS	42	100K	49	100K	48	100K	ns
Precharge to Active command period		tRP	18		20		20		ns
Active to read/write command delay		tRCD	18		20		20		ns
Write recovery time	CL = 3	tWR	6		7		8		ns
	CL = 2		10		10		10		

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

-6T (Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		42ns	18ns	18ns	6ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	2	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7T (Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		49ns	20ns	20ns	7ns/10ns
133MHz (7.5ns)	3	7	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

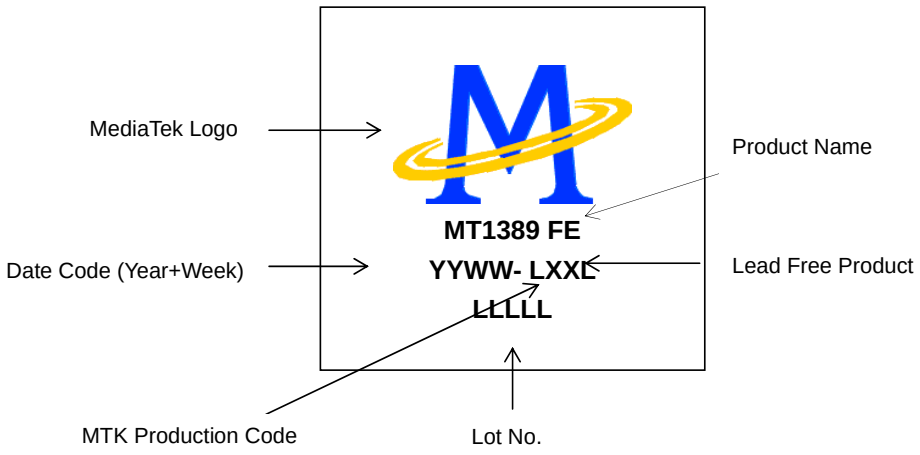
-7.5T (Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		45ns	20ns	20ns	7.5ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-8T (Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		48ns	20ns	20ns	8ns/10ns
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	3	5	2	2	1

10 Marking on Devices

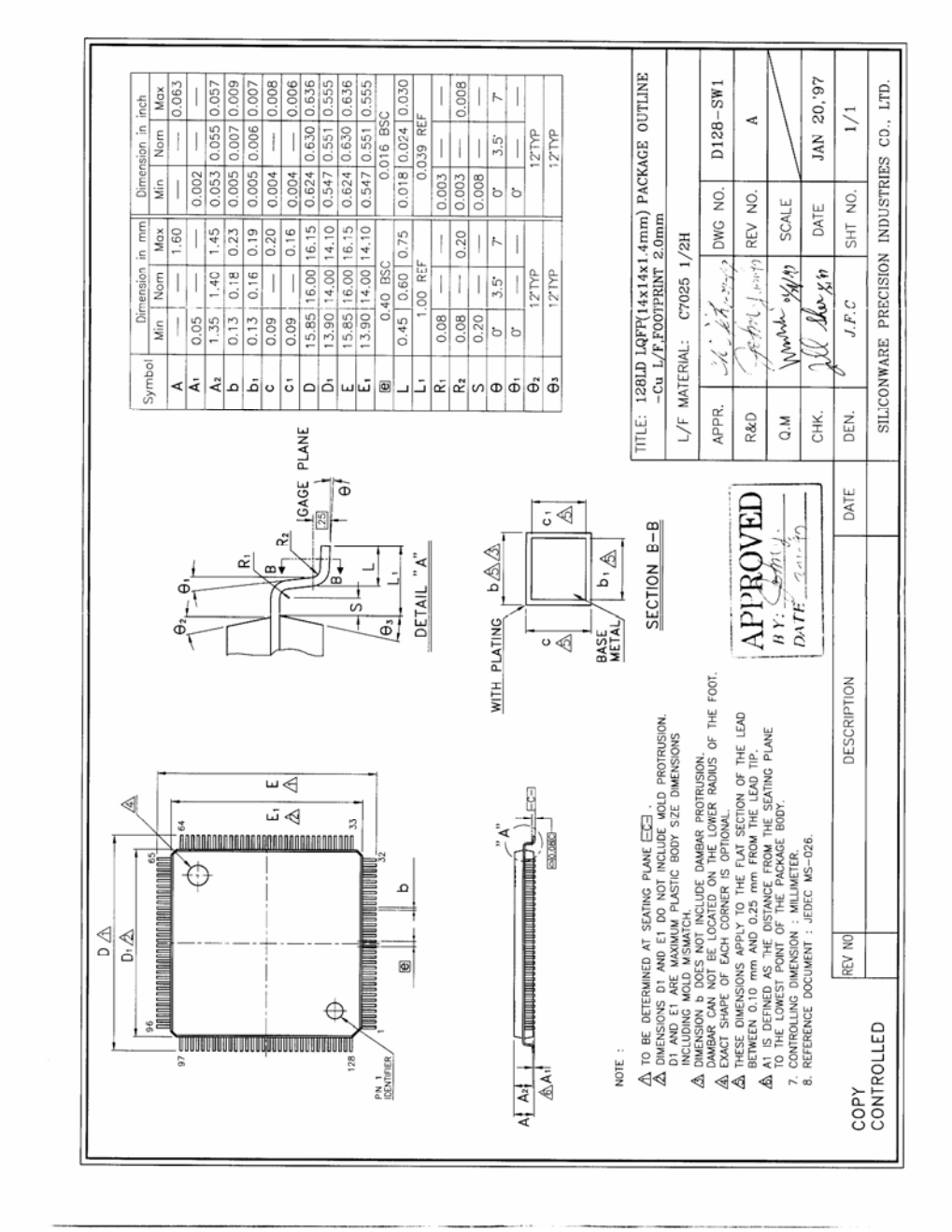


11 Package Description

带格式的：项目符号和编号

11-1 Package Outline Dimension

The bend lead are controlled under the criteria 0.075mm (2.5mil).



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2		12°TYP			12°TYP	
θ3		12°TYP			12°TYP	

11-2 Weight of the chip

0.65g

11-3 Material and Finish of Lead Terminals

For Normal Package, (Materials of terminal is Sn(85%) and Pb (15%)and thickness is 300~600u inch.

For Lead-free Package, (Materials of terminal is Sn(98%) and Bi (2%)and thickness is 300~600u inch, similar as SnPb.

11-4 Package Material

Lead frame: Cu

Epoxy: 1033BF

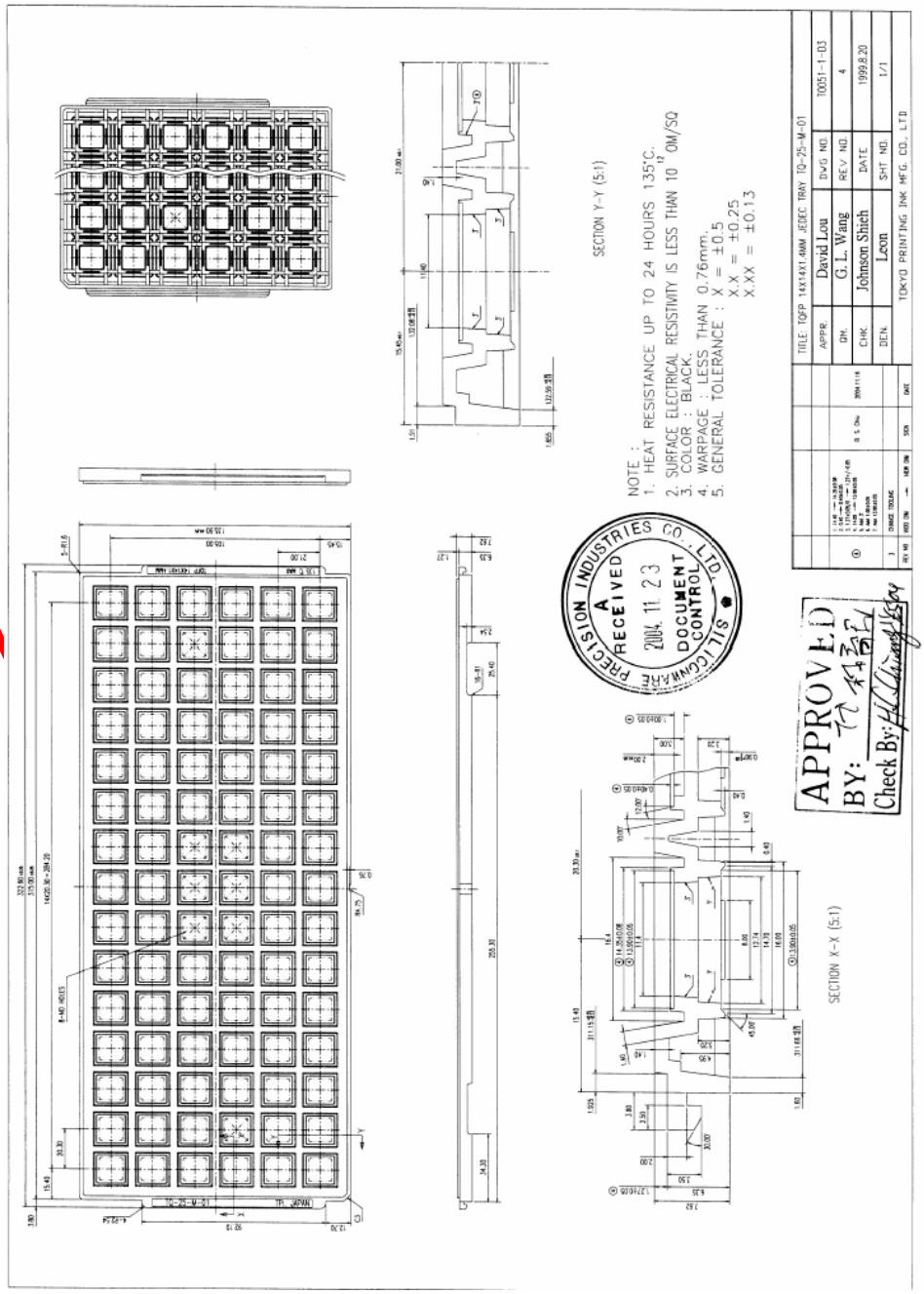
Molding compound: G700

12 Packing Description

Package	Pin / Ball count	EA / Tray	Tray / Box	Full Box Q'ty	Box / Carton	Full carton Q'ty
LQFP	128	90	10	900	6	5400

12-1 Tray Description

40ea/ Hard Tray (150^{o}C resistance).



12-2 Desiccants

Size: 110*120 mm.

Weight: 66g

12-3 Aluminum Foil Bag

Size: 250*500 mm.

Thickness: 0.12 +/- 0.005 mm.

Surface impedance: 10^{8}-10^{12} Ohm/SQ

12-4 Box Description

Material: 3 Layer B corrugated paper.

Strength: 1176000 PA.

Box size: 355(L)*157(W)*90.5(H) mm.

Printing: Black (words, warning, index)

12-5 Side Plank

Material: 5 Layer AB corrugated paper

Strength: 1793400 PA.

Size: 405(L)*237(W) mm.

Fixture: 3 pieces of EPE (recyclable material).

Thickness: 20 mm.

12-6 Carton Description

Material: 5 Layer AB corrugated paper.

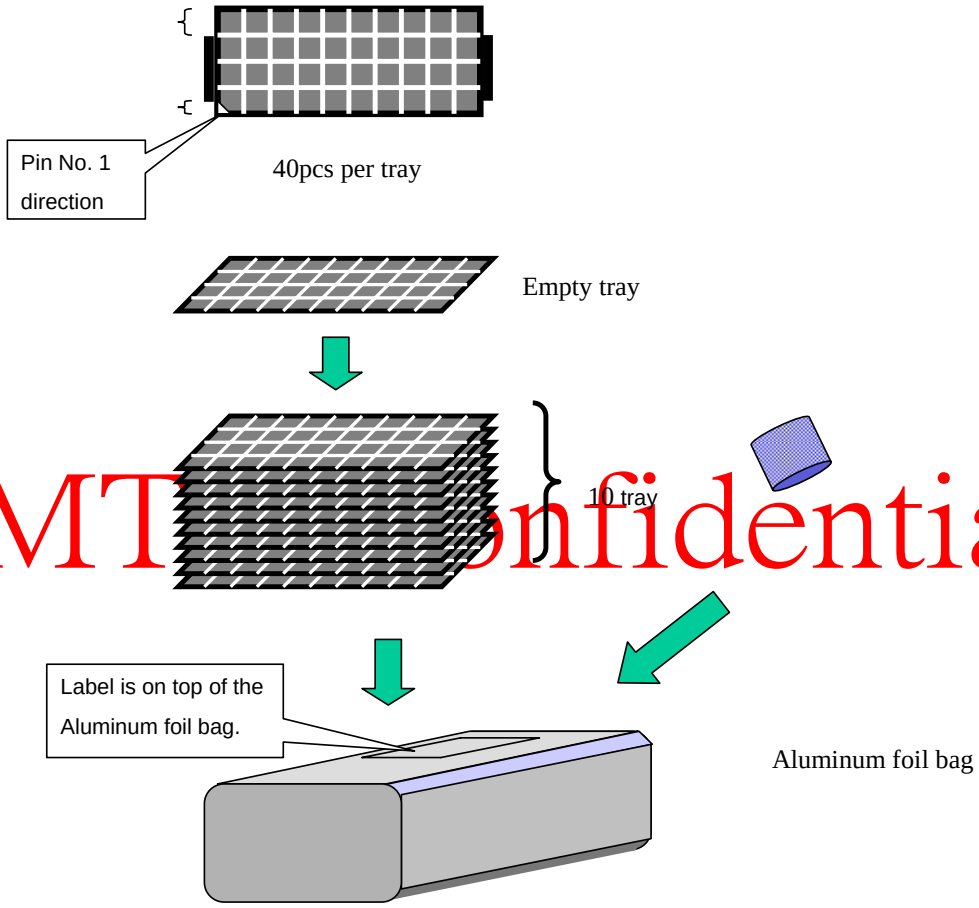
Strength: 1793400 PA.

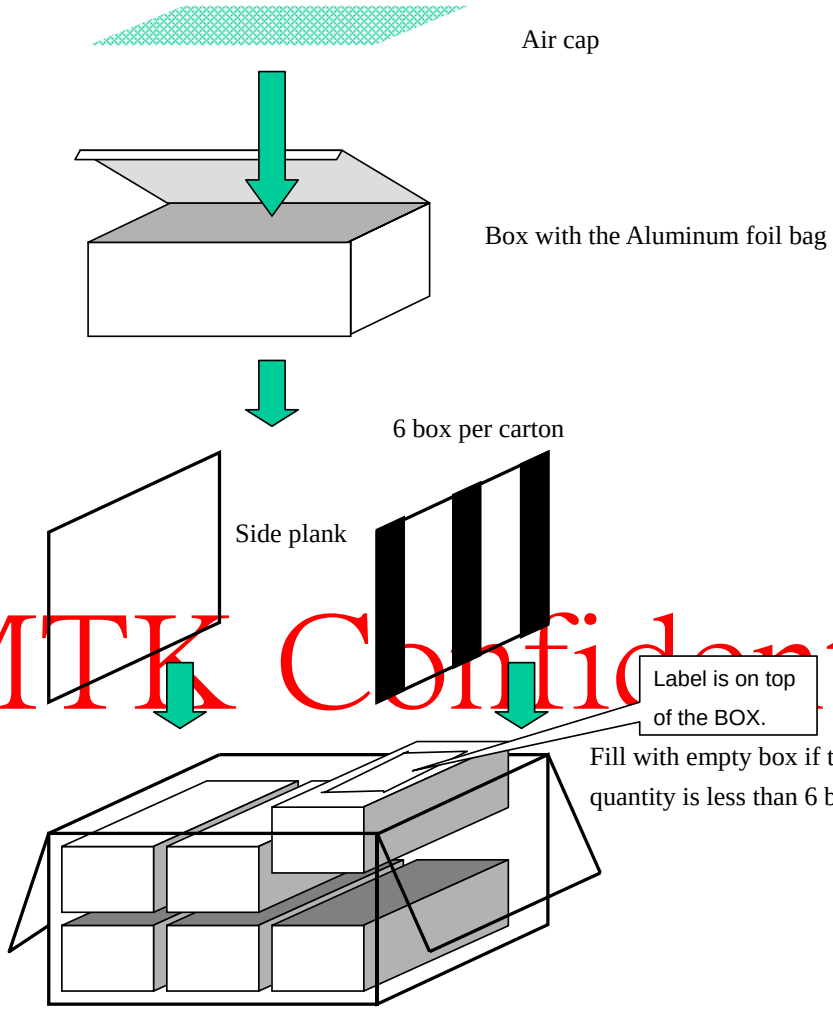
Carton size: 558(L)*428(W)*264(H) mm.

Printing: Black (words, warning, index)

带格式的: 项目符号和编号

12-7 Packing Flow





带格式的: 项目符号和编号

13 Solder-Reflow Condition

13-1 Reflow Condition

MTK can guarantee 3 times IR reflow base on the reflow curve.

Average ramp-up rate (217°C to peak) : 3 °C /sec. max.

Preheat : 150~200°C、60~180 seconds

Temperature maintained above 217°C : 60~150 seconds

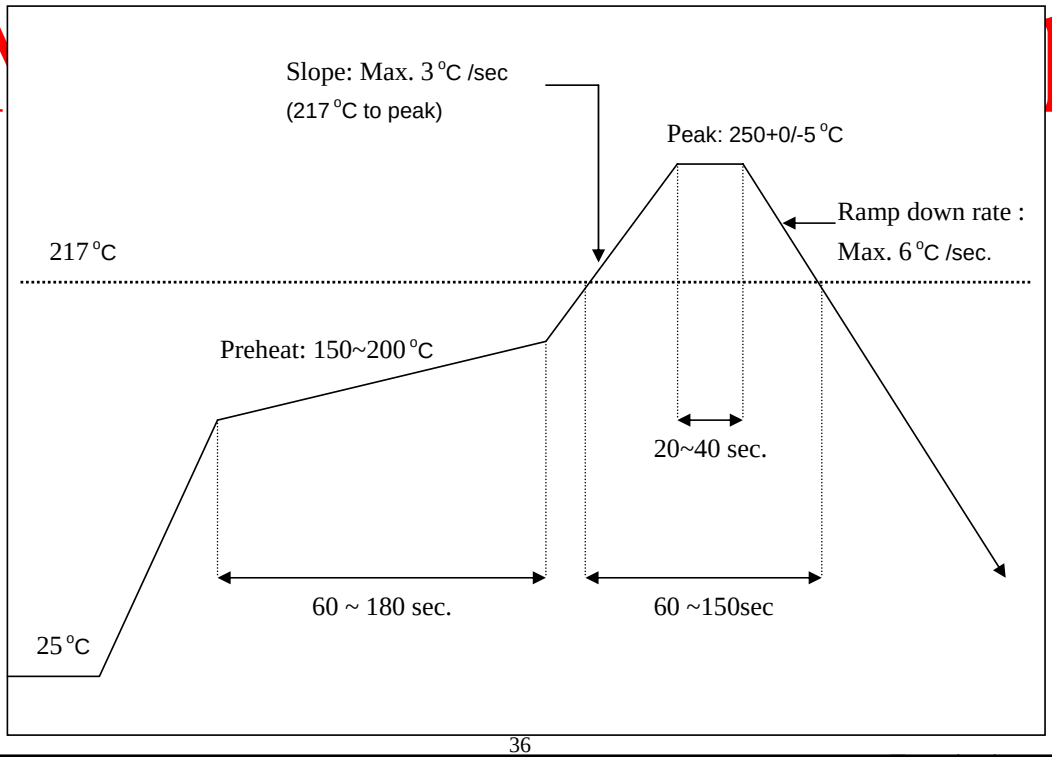
Time within 5°C of actual peak temperature : 20 ~ 40 sec.

Peak temperature : 250+0/-5°C

Ramp-down rate : 6°C /sec. max.

Time 25°C to peak temperature : 8 minutes max.

Cycle interval : 5 minus



13-2 Pre-process and Heat Treatment

带格式的: 项目符号和编号

Procedure: (MRT L3)

[Package opening] → [Baking] → [Humidification] → [Reflow]

A. Conditions between each step of procedure

Be lift for duration of 2 hours or longer at temperature of 30 °C or lower and a humidity of 60% R.H. or lower.

B. Baking 125 °C, 24 hours.

C. Humidification: 30 °C, 60% R.H., 192 Hours

D. Reflow: 3 x 260oC

14 Manual Solder Condition

带格式的: 项目符号和编号

The specimen should be in the as-delivered condition. Set the soldering iron at a temperature of 300 +/- 10 °C (at the iron bit). Place the iron and flux-cored solder in parallel with each and every terminal/lead on the back of the board for a duration which does not exceed 5 seconds without applying any mechanical stress on the component body.

It can also be applied under 350 +/- 10 °C at the iron bit within 3 seconds, please treat it carefully under such condition.

The chip can't do DIP soldering.

15 Storage Condition

15-1 Storage Duration

A. Notice the Sealing time.

B. 12 monthly and storage condition: <= 40°C , <= 90% R.H.

C. Warehouse control: First in and First out.

15-2 After Open the Bag

A. SMT: Should finish the SMT process within 168 hours

B. Check the humidity check card: The value should < 20% (blue), if the value >= 30% (red), it means the IC has got moisture.

C. Factory environment control: <= 30°C, <= 60% R.H.

16 Other

If a doubt related to the present specifications arises, the problem will be solved based on discussion between the both parties.