MT3333 All-in-One GNSS Datasheet

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Document Revision History

Revision	Date	Description
0.3	26th October 2016	Initial public release
1.0	5 December 2016	Copy editing.

Table of contents

Lists of figures

1. Introduction

1.1. Overview

MediaTek MT3333 is a high-performance single-chip multi-GNSS solution that includes CMOS RF, digital baseband, ARM7 CPU and embedded NOR flash. It's able to achieve the industry's highest level of sensitivity, accuracy and Time-to-First-Fix (TTFF) with the lowest power consumption. Its small footprint lead-free package and minimal additional BOM requirements provide significant reductions in the design, manufacturing and testing resources required to create devices.

The main features that help reduce device BOM are:

- Built in Low Noise Amplifier (LNA) that eliminates the need for an external antenna.

- Built-in image-rejection mixer that removes the need for an external Surface Acoustic Wave (SAW) filter.

- Built-in automatic center frequency calibration band pass filter that means an external filter is not required.

- Built-in power management that enables MT3333 to be easily integrated into your system without an extra voltage regulator. With both linear and highly efficient switching type regulators embedded, MT3333 supports direct battery connection and doesn't need an external low-dropout (LDO) regulator, which offers flexibility in circuit design.

In addition, 12 multi-tone active interference cancellers (ISSCC2011 award) can eliminate the need to design interference cancelation, simplifying PCB design. The integrated Phase-Locked Loop (PLL) with Voltage Controlled Oscillator (VCO) provides excellent phase noise performance and fast locking time. A battery backed-up memory and a real-time clock are also provided to accelerate location acquisition at system restart.

MT3333 supports various location and navigation applications, including GPS, GLONASS, Galileo, BeiDou, SBAS ranging (WAAS, EGNOS, GAGAN and MSAS), QZSS, DGPS (RTCM) and A-GPS.

The excellent low-power consumption characteristics of MT3333 (37 mW for acquisition and 27 mW for tracking) means that — without changing the specified battery — power sensitive devices, especially portable applications, will be able to offer device users longer operating times. Combined with advanced software features including EASY™, EPO™ and LOCUS™, MT3333 provides always-on positioning with minimal average power consumption. These great features provide you with outstanding performance for portable applications, such as DSC, mobile phones, PMP and gaming devices.

1.2. Features

- Specifications
  - GPS/GLONASS/Galileo/BeiDou receiver
  - Supports multi-GNSS including QZSS and SBAS ranging
  - Supports WAAS, EGNOS, MSAS and GAGAN
  - 12 multi-tone active interference cancellers (ISSCC2011 award)
  - RTCM ready
  - Indoor and outdoor multi-path detection and compensation
  - Supports FCC E911 compliance and A-GPS[1]
  - Maximum fixed update rate up to 10 Hz
- Advanced software features
  - EPO™ orbit prediction
  - EASY™ self-generated orbit prediction
  - LOCUS™ logger function
  - Supports time service application, which is achieved by the PPS vs NMEA feature.
- Reference oscillator
  - TCXO
    - Frequency: 16.368 MHz, 12.6 ~ 40.0 MHz
    - Frequency variation: ±2.5 ppm
  - Crystal
    - Frequency: 26 MHz, 12.6 ~ 40.0 MHz
    - Frequency accuracy: ±10 ppm
- RF configuration
  - SOC, integrated in single chip with CMOS process
- ARM7EJ-S CPU
  - Up to 158 MHz processor clock
  - Dynamic clock rate control
- Memory:
  - 8Mb internal flash
  - External SPI serial flash of up to 128 Mb
- Pulse-per-second (PPS) GPS time reference
  - Adjustable duty cycle
  - Typical accuracy: ±10 ns
- Power scheme
  - Built-in 1.8 volts Switching Mode Power Supply (SMPS)

- Direct lithium battery connection (2.8 ~ 4.3 volts)
  - Built-in 1.1 volts RTC LDO, 1.1 volts core LDO and 2.8 volts TCXO LDO
- Built-in reset controller
  - Does not need an external reset control IC
- Internal real-time clock (RTC)
  - 32.768 kHz ± 20 ppm crystal
  - 1.1 volts RTC clock output
  - Supports external pin to wake up MT3333
- Backup mode
  - A Force_On pin to simplify the backup mode application circuit
- Serial interfaces
  - 3 UARTs
  - SPI and I2C
  - GPIO interface (up to 16 pins)
- NMEA
  - NMEA 0183 standard V4.1 and backward compliance
  - Supports 219 datums
- Sensitivity
  - Acquisition: -148 dBm (cold) / -163 dBm (hot)
  - Tracking: -165 dBm
- Ultra-low power consumption (GPS+GLONASS)
  - Acquisition: 37 mW
  - Tracking: 27 mW
- Package
  - VFBGA: 4.3 mm x 4.3 mm, 57 balls, 0.5 mm pitch
- Slim hardware design
  - Mimimun solution footprint of 52 mm^2
  - Single RF Front-End for Multi-GNSS frequency bands
- Compatibility
  - Pin-to-pin compatiblity with MT3339

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[1] When combined with a suitable cellular network modem.

2. Pin Assignment and Descriptions

2.1. Pin descriptions

Pin#	Symbol	Type	Description
System interface (2 pins)			
A4	HRST_B	2.8V LVTTL input	System reset.
B4	XTEST	2.8V LVTTL input	Test mode
Peripheral interface (8 pins)			
B7	RX0	2.8V, LVTTL I/O	Serial input for UART 0
B8	TX0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 0 Default: pull-up Default: 8mA driving
G8	RX1	2.8V, LVTTL I/O	Serial input for UART 1
H8	TX1	2.8V, LVTTL I/O	Serial output for UART 1
C8	RX2	2.8V, LVTTL I/O	Serial input for UART 2
F7	TX2	2.8V, LVTTL I/O	Serial output for UART 2
D7	SCK1	2.8V, LVTTL I/O	SPI clock output
A6	SCS1#	2.8V, LVTTL I/O	SPI slave selection 1
Debugging interface (6 pins)			
G7	GIO6	2.8V, LVTTL I/O	GPIO
C6	GIO7	2.8V, LVTTL I/O	GPIO
E6	GIO8	2.8V, LVTTL I/O	GPIO
B6	GIO9	2.8V, LVTTL I/O	GPIO
D6	GIO10	2.8V, LVTTL I/O	GPIO
A7	GIO11	2.8V, LVTTL I/O	GPIO
External system interface (4 pins)			
C4	EINT0	2.8V, LVTTL I/O	External interrupt 0
C5	EINT1	2.8V, LVTTL I/O	External interrupt 1
C7	EINT2	2.8V, LVTTL I/O	External interrupt 2
D8	EINT3	2.8V, LVTTL I/O	External interrupt 3
RTC interface (6 pins)			
H6	AVDD43_RTC	Analog power	RTC LDO input
H7	AVDD11_RTC	Analog power	RTC LDO output
H5	XIN	Analog input	RTC 32KHz XTAL input
H4	XOUT	Analog output	RTC 32KHz XTAL output
G6	32K_OUT	1.2V LVTTL I/O	RTC domain GPIO pin, able to configure to low power detection indicator signal
G5	FORCE_ON	1.2V LVTTL input	Logic high to force power on this chip

Pin#	Symbol	Type	Description
RF and analog			
B1	AVDD18_RXFE	RF power	1.8V supply for RF core circuits
A3	T1P	Analog signal	RF testing signal
B3	T1N	Analog signal	RF testing signal
A2 B2 C2 D2	AVSS_RF	RF ground	RF ground pins
C1	AVDD18_CM	RF power	1.8V supply for XTAL OSC, bandgap, thermal sensor and level shifter
D1	OSC	Analog signal	Input for crystal oscillator or TCXO
A1	RF_IN	RF signal	LNA RF Input pin
F5	DVDD11_CORE1	Digital power	Digital 1.1V core power input
A5	DVDD11_CORE2	Digital power	Digital 1.1V core power input
E5	DVSS11_CORE	Digital ground	Digital 1.1V core ground
E8	DVDD28_IO1	Digital power	Digital 1.8/2.8V IO power input
B5	DVDD28_IO2	Digital power	Digital 1.8/2.8V IO power input
E7	DVSS28_IO	Digital ground	Digital 1.8/2.8V IO ground
F6	DVDD28_SF	Digital power	Digital 2.8V serial flash power input
D5	DVSS28_SF	Digital ground	Digital 2.8V serial flash ground
F1	VREF	Analog	Bandgap output pin
F2	AVSS43_MISC	Analog ground	GND pin for buck controller, TCXO LDO and start-up block
E1	AVDD43_VBAT	Analog power	TCXO LDO input pin
G2	AVDD_TCXO_SW	Analog power	TCXO power switch output pin
G1	AVDD28_TLDO	Analog power	TCXO LDO output pin
E2	AVDD28_CLDO	Analog power	Core LDO input pin
H1	AVDD11_CLDO	Analog power	Core LDO output pin
F3	AVSS11_CLDO	Analog ground	GND pin for core LDO
G3	AVSS43_DCV	SMPS	SMPS GND pin
H2	DCV	SMPS	SMPS output pin
H3	AVDD43_DCV	SMPS	SMPS input pin.
F4	DCV_FB	SMPS	SMPS feedback pin

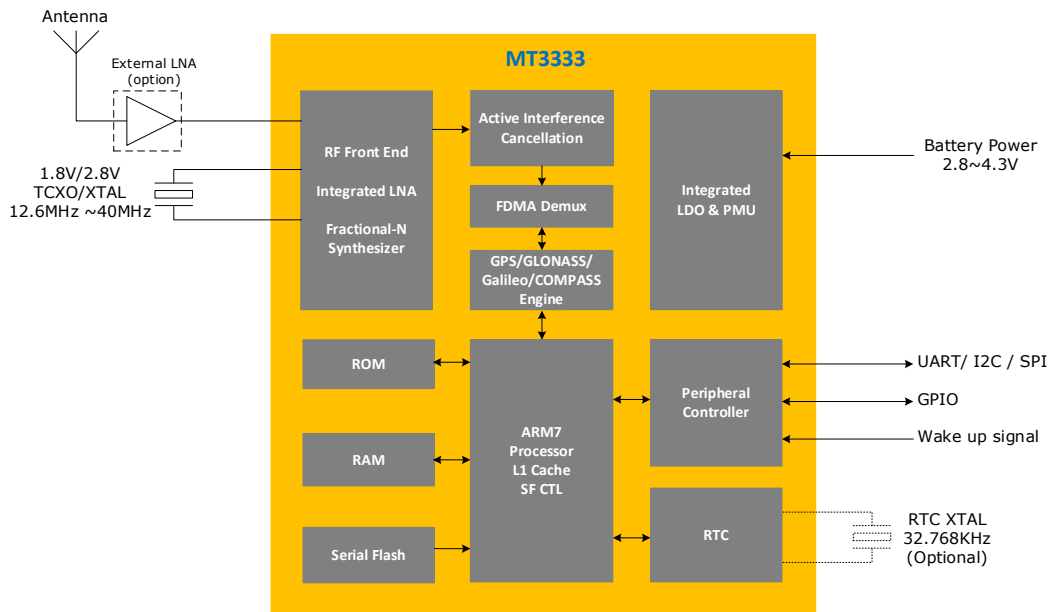# 3.   System Block Diagram

Figure 3-1: MT3333 system block diagram

4. Radio Subsystem Features

4.1. Low Noise Amplifier (LNA) and mixer

The MT3333 includes an LNA that offers devices two antenna options:

- A multi-GNSS antenna connected directly to the internal LNA in high-gain mode, ideal for low-cost solutions without an external LNA.

- An external antenna and high gain external LNA connected to the internal LNA in low-gain mode, which offers high linearity. In this configuration, external LNA gain ranging from 15 to 20 dB is recommended. The maximum total external RF front end gain including active antenna and external LNA can be 43dB.

The down-conversion mixer then converts the amplified signal to the Intermediate Frequency (IF) signal. The down-conversion mixer is a single-ended passive mixer, with a current mode interface between the mixer and multi-modes low pass filter.

4.2. Voltage Controlled Oscillator (VCO) and synthesizer

The frequency synthesizer includes a crystal oscillator, VCO, divider, phase frequency detector (PFD), charge pump (CP) and loop filter, which are all integrated on the MT3333 chip. The VCO is auto-calibrated to its required sub-band when the chip is powered on.

4.3. Low Pass Filter (LPF)

The current-mode LPF provides modes for the various combinations of GNSS constellations supported by MT3333.

4.4. Analog-to-Digital Converter (ADC)

The differential IF signal is quantized by a high performance ADC. The ADC sampling clock is provided by the divided clock from the local oscillator (LO).

4.5. Active Interference Canceller (AIC)

The AIC can detect 12 different single-tone interference signals. It can then track the phase and frequency of these 12 interference signals to provide continuous cancellation.

5. Processor Subsystem Features

5.1. ARM7EJ-S

The ARM7EJ-S processor provides the flexibility necessary to build Java-enabled, real-time embedded devices requiring small size, low-power and high performance. It builds on the features and benefits of the established ARM7TDMI core and is delivered in synthesizable form.

ARM7EJ-S includes a JTAG interface that provides a standard development and debugging interface. The interface can connect to a variety of off-the-shelf emulators. These emulators can provide single-step, trap and access to all the internal registers of the processor subsystem.

5.2. Cache

MT3333 provides a cache to speed up program execution and reduce external flash access times. It supports cache buffer and can be repurposed as internal memory when it is not used fully.

5.3. Boot ROM

The embedded boot ROM provides for the loading of user code through a serial interface into SRAM. The serial interface (UART, SPI or I2C) is determined by strap control.

5.4. Real Time Clock (RTC)

There is a built-in 1.1 volts low-dropout (LDO) regulator for the RTC domain, which can be bypassed when an external LDO is used. The RTC LDO is a voltage regulator that has a very low quiescent current. A small ceramic capacitor can be used as the output capacitor, and the stable operation region ranges from very light load (≈0mA) to about 3 mA.

Also within the RTC power domain the MT3333 provides a very low leakage battery backed-up memory. This memory contains all the necessary multi-GNSS information for quick start-up and a small number of user configuration variables.

5.5. Switching Mode Power Supply (SMPS)

A built-in SMPS provides a 1.8 volts power supply for the digital 1.1 volts Core Low-Dropout (CLDO) regulator and RF input power. In the active mode, the SMPS operates in automatic pulse width modulation (PWM) and pulse frequency modulation (PFM) switching mode. In low power mode, the SMPS operates with reduced switching frequency in the PFM mode.

5.6. Timer function

The timer function supports time tick generation with 31.25 ms resolution.

5.7. General Purpose Input/Output (GPIO) in the RTC domain

The 32K_OUT pin in the RTC domain can output a 32.768 kHz clock. This can be used to support a low clock rate operation mode, for applications or peripherals that need an external clock source. This pin can be programmed to be the input pin to receive a wake-up signal from an external accelerator sensor IC, when MT3333 is in the low-power mode.

5.8.   Low power detection

A low power detection circuit is included. Whenever the independent power source (AVDD11_RTC) voltage becomes low, the low power detection circuit will provide an indicator signal at pin 32K_OUT (output high in normal condition and low in low-power condition).

5.9.   Clock module

The clock module generates all internal clocks required by the processor, correlator, internal memory, bus interface and so on. The referenced input clock is generated from the RF subsystem.

5.10.   Reset controller

The built-in reset controller generates reset signals for all digital blocks. It has power-on reset feature and hardware trapping function. The power-on reset level is 2.7 ± 0.1 volts. The software reset function for different circuit blocks are also included for flexible applications.

In Figure 5-2, the voltage drop time T_{drop_vbat} and T_{drop_cldo} depend on the capacitance connection of their power net. But $T_{drop\_vbat} > T_{drop\_cldo}$ should be guaranteed for the correct operation of reset behavior during power off sequence. It is strongly recommend using external LDOs without output discharged function or make sure T_{drop_vbat} > 1 ms.
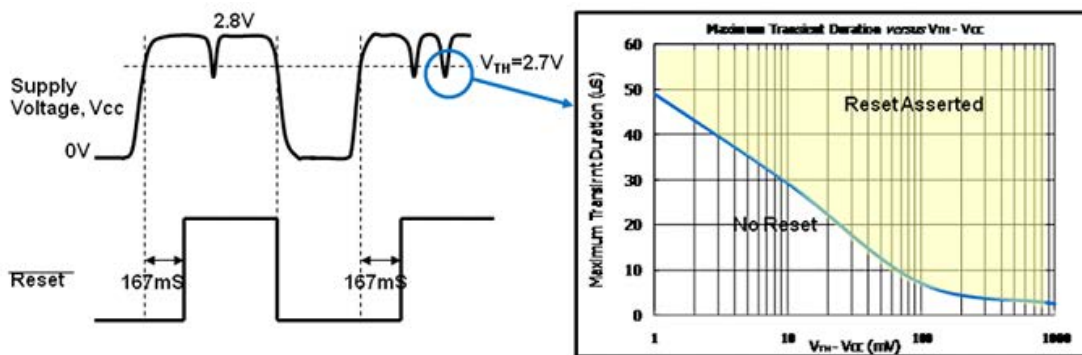
Figure 5-1: Power on reset diagram
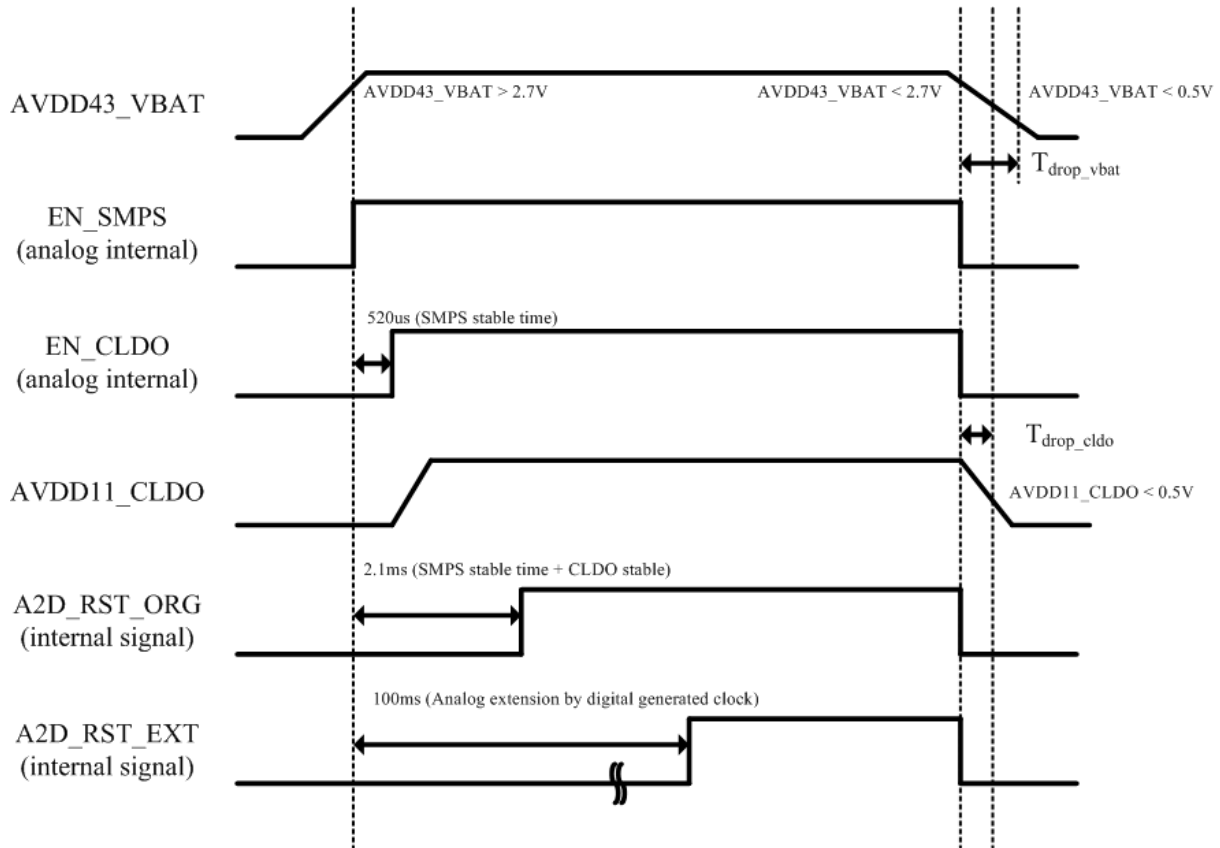
Figure 5-2: Power on/off reset behavior

5.11.   Serial interfaces

MT3333 supports three serial interfaces: UART, SPI and I2C. The active serial interface type is determined by strap pins. Note that firmware with SPI and I2C support is available on request, the standard chipset firmware supports UART only.

5.11.1.   Universal Asynchronous Receiver/Transmitter (UART)

MT3333 has three full duplex serial ports that can be used for serial data communication. UART communication functions provided include: UART data transmission/receive and NMEA sentences input/output. In general, UART0 is used for NMEA output and PMTK command input, while UART1 is RTCM input. You can adjust the UART2 port as desired. UART provides signal or message outputs.

5.11.2.   Serial Peripheral Interface (SPI)

Note: SPI support is available in firmware on request.

The SPI port manages the communication between digital baseband (BB) and external devices. MT3333 supports both master and slave modes. In the master mode only 4 bytes of register can be transferred. In slave mode 4-byte-register or SRAM FIFO options are available. In the SRAM FIFO mode, the size of the data blocks transmitted and received is 256 bytes. The clock phase and clock polarity are selectable. MT3333 supports a manual or automatic indicator for data transfer in the slave mode.

5.11.3. Inter-Integrated Circuit (I2C)

Note: I2C support is available in firmware on request.

I2C support in MT3333 offers multi-master and slave modes. The multi-master mode supports 7-bit and 10-bit address modes up to 400 Kb/s fast mode and 3.4 Mb/s high-speed mode. In addition, MT3333 supports a manual or automatic indicator for data transfer in the slave mode. Device addresses in the slave mode are programmable and support fast mode and high-speed mode data transmission and reception.

5.12. Interrupt control unit

The interrupt control unit manages all internal and external sources of interrupts, which include timer, watch-dog, all interfaces (UART, I2C and SPI) and external user interrupt pins. These interrupt sources can be used as wake-up events when the chipset is in low power mode.

5.13. Flash

External SPI serial flash of up to 128 Mb is supported. A MediaTek Flash tool is provided for downloading firmware into the 8Mb internal flash.

5.14. General-Purpose Input/Output (GPIO) unit

MT3333 supports a variety of peripherals through up to 16 programmable GPIO ports. The number of available GPIO ports will depend on which serial interface is in use. The unit manages all GPIO lines and supports a simple control interface. GPIO provides signal or message outputs.

5.15. Pulse Per Second (PPS) output

The PPS signal can be provided through the designated output pin for external applications. In addition to its limit of being active every second it's possible to set up the duration, frequency and active high/low by programming user-defined settings.

5.16. External Clock (ECLK) pin

An external clock signal can be applied to MT3333 using the ECLK pin and is used to obtain the relation between the external clock and GPS local clock.

With precise external clock input, the clock drift of the GPS local clock can be correctly estimated. Using this information, the Doppler search range is narrowed down. This technology is beneficial because it speeds up the satellite acquisition process. Particularly in the cold start case, due to limited prior information about the satellites' location and local clock uncertainty, a receiver will execute a search across the full frequency range. Consequently, a longer acquisition time can be expected. However, the ECLK technology is able to reduce the frequency uncertainty so that the search process will be completed in a shorter time. Efficient acquisition and lower power consumption are achieved with ECLK technology.

5.17. SYNC

SYNC is a timestamp signal input pin for introducing external timing information to the GPS receiver. It's used to obtain the relationship between the external timing and the GPS receiver local timing, from which the GPS time of week (TOW) can be correctly estimated.

This technology is beneficial for time to first fix (TTFF), particularly in weak signal environments. In hot start, with prior information about the GPS receiver's location and satellite ephemeris data, the GPS receiver uses the correct

GPS TOW to accurately predict the signal code chip/phase. As a result, the code search range can be narrowed down and a fast TTFF is achieved.

5.18. Power scheme

- Internal SMPS is used as the source power of the internal RF/BB LDO. It is also used as 1.8 volts I/O power, external TCXO/LNA voltage source via built-in TCXO switch. The internal SMPS can switch to the LDO mode to supply power to each of the about block

- The minimum/maximum input voltage of AVDD43_VBAT and AVDD43_DCV is 2.8/4.3 volts.

- The power-on reset voltage threshold of AVDD43_VBAT is 2.7 ± 0.1 volts. The maximum TLDO drop out voltage at half load (25 mA) is 0.2 volts. If one external LDO is used to provide power to MT3333, the 3.3 volts external LDO will be recommended after taking TLDO drop-out into consideration.

- The power efficiency in SMPS mode will be better than that in the internal LDO mode.

- I/O supports 1.8 and 2.8 volts. The power comes from SMPS output for 1.8 volts application or TLDO output (AVDD28_TLDO) for 2.8 volts application.

- The power for internal flash comes from AVDD28_TLDO.

- TCXO power is from AVDD_TCXO_SW that can select either from AVDD28_TLDO (2.8V) or from AVDD28_CLDO (1.8V) by setting up power-on strap.

- RTC LDO input power comes from backup battery or uses coin battery.

- Here are 3 power schemes: low power (Figure 5-3), low cost (Figure 5-4) and external PMU (Figure 5-5).

- The power on and power off sequence of external PMU mode is shown in Figure 5-6.
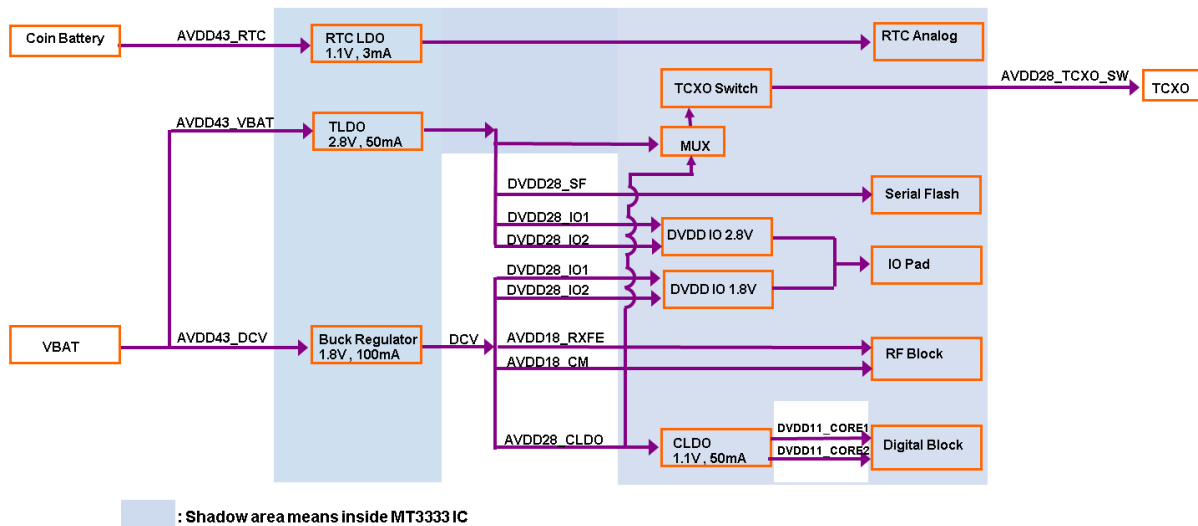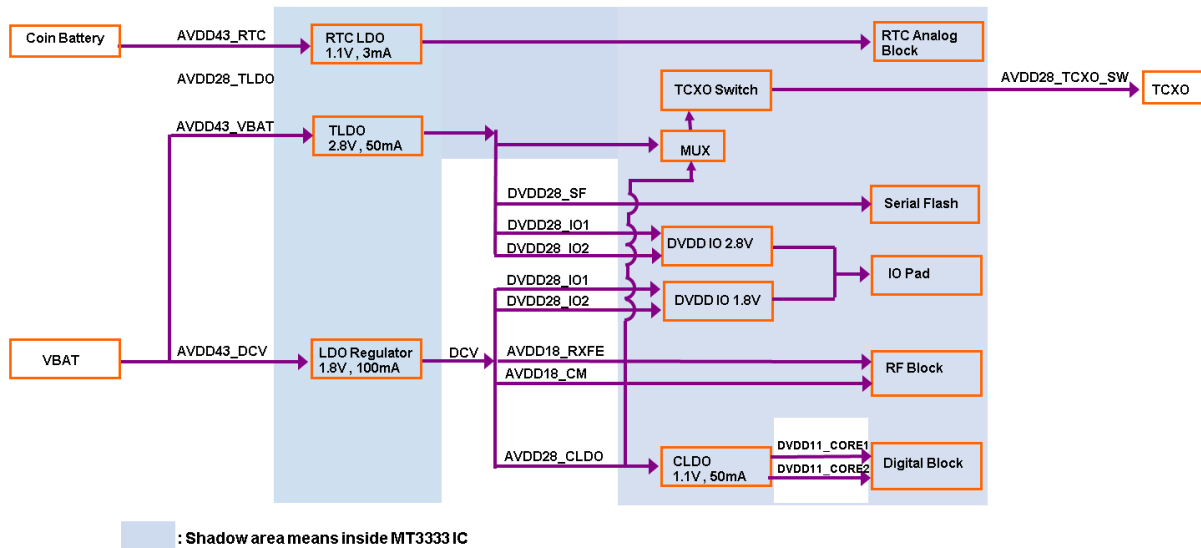

Figure 5-3: Power supply connection (low power)

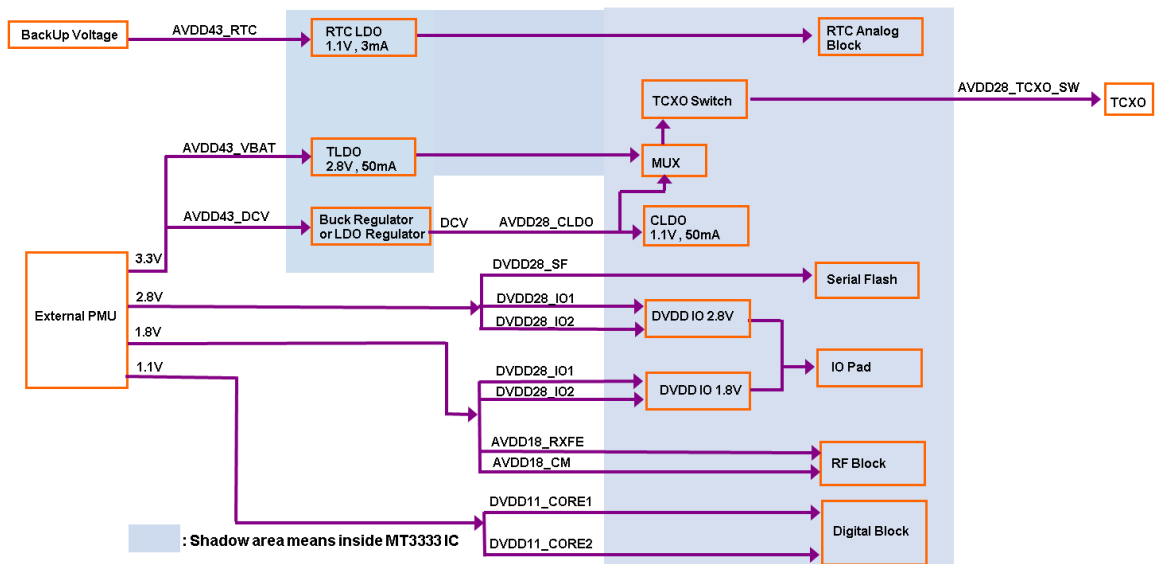*Figure 5-4: Power supply connection (low cost)*

Figure 5-5: Power supply connection (external LDO)
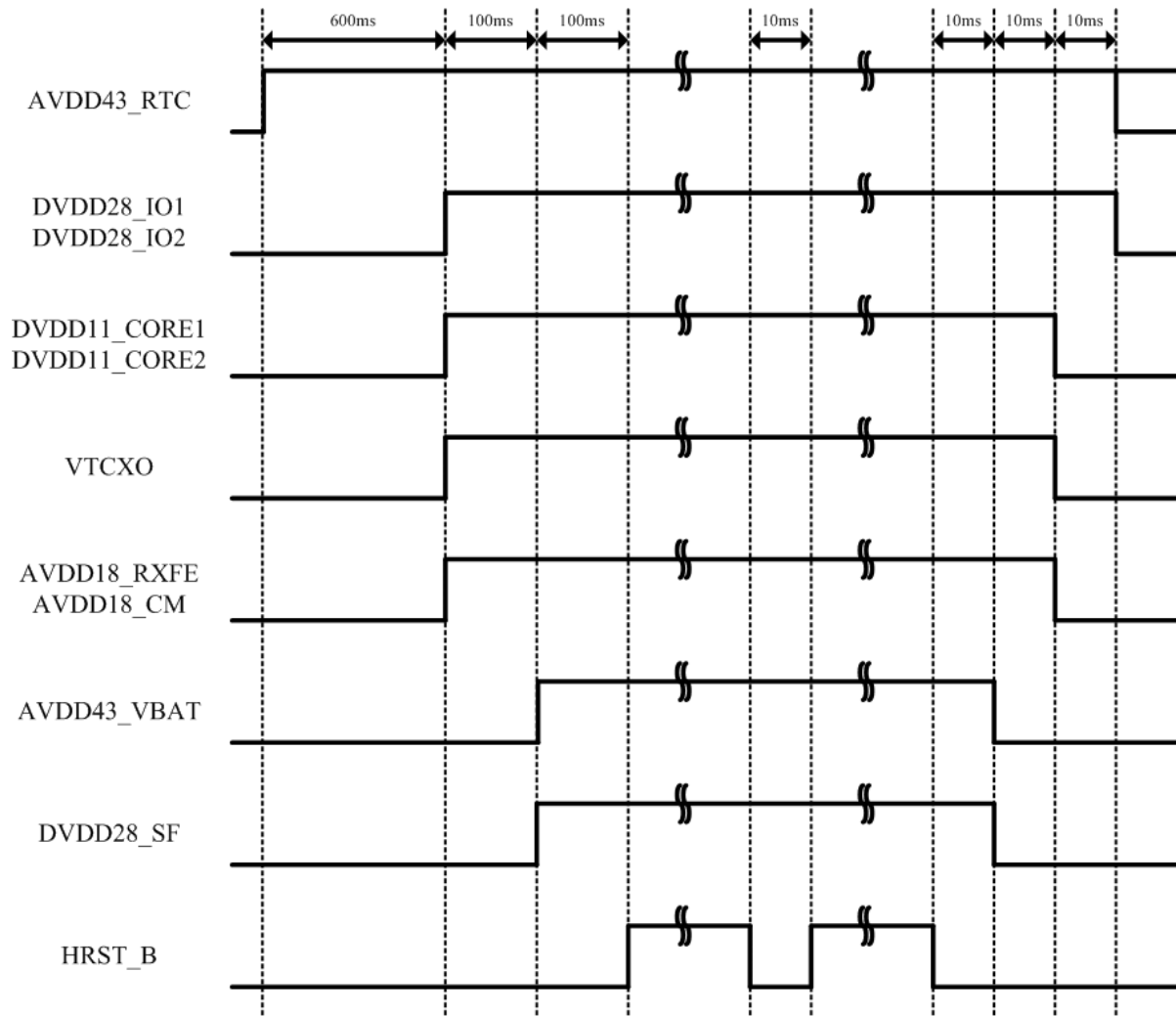
Figure 5-6: Power on/off sequence for external LDO mode

6. Electrical Characteristics

6.1. DC characteristics

6.1.1. Absolute maximum ratings

Symbol	Parameter	Rating	Unit
AVDD43_DCV	SMPS power supply	-0.3 ~ 4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	-0.3 ~ 4.3	V
AVDD28_CLDO	1.1 volts CLDO power supply	-0.3 ~ 3.6	V
DVDD28_SF	Embedded flash power supply	-0.3 ~ 3.6	V
DVDD28_IO1 DVDD28_IO2	IO 2.8/1.8 volts power supply	-0.3 ~ 3.6	V
DVDD11_CORE1 DVDD11_CORE2	Baseband 1.1 volts power supply	-0.3 ~ 1.21	V
AVDD43_RTC	RTC 1.1 volts LDO power supply	-0.3 ~ 4.3	V
AVDD18_RXFE	1.8 volts supply for RF core circuits	-0.3 ~ 3.6	V
AVDD18_CM	1.8 volts supply for common RF block in LDO mode	-0.3 ~ 3.6	V
T_{STG}	Storage temperature	-50 ~ +125	˚C
T_A	Operating temperature	-45 ~ +85	˚C

6.1.2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD43_DCV	SMPS power supply	2.8	3.3	4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	2.8	3.3	4.3	V
DVDD11_CORE1 DVDD11_CORE2	1.1 volts baseband core power	0.99	1.1	1.21	V
DVDD28_IO1 DVDD28_IO2	2.8 volts digital I/O power	2.52	2.8	3.08	V
	1.8 volts digital I/O power	1.62	1.8	1.98	V
DVDD28_SF	Embedded flash power supply	2.7	2.8	3.6	V
AVDD18_RXFE	1.35 volts supply for RF core circuits in bypass mode	1.3	1.35	1.98	V
	1.8 volts supply for RF core circuits in LDO mode	1.62	1.8	3.08	V
AVDD18_CM	1.35 volts supply for common RF block in bypass mode	1.3	1.35	1.98	V
	1.8 volts supply for common RF block in LDO mode	1.62	1.8	3.08	V
T_A	Operating temperature	-40	25	85	˚C

Symbol	Parameter	Min.	Typ.	Max.	Unit
T$_j$	Commercial junction operating temperature	0	25	115	˚C
	Industry junction operating temperature	-40	25	125	˚C

6.1.3. General DC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
I$_{IL}$	Input low current	No pull-up or down	-1	1	uA
I$_{IH}$	Input high current	No pull-up or down	-1	1	uA
I$_{OZ}$	Tri-state leakage current		-10	10	uA

6.1.4. DC electrical characteristics for 2.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		2.52	2.8	3.08	V
V$_{IL}$	Input low voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V$_{IH}$	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V$_{OL}$	Output low voltage	VDDIO = min I$_{OL}$ = -2 mA	-	-	0.15*VDDIO	V
V$_{OH}$	Output high voltage	VDDIO = min I$_{OH}$ = -2 mA	0.85*VDDIO	-	-	V
R$_{PU}$	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
R$_{PD}$	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

6.1.5. DC electrical characteristics for 1.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
V$_{IL}$	Input low voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V$_{IH}$	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V$_{OL}$	Output low voltage	VDDIO = min I$_{OL}$ = -2 mA	-	-	0.15*VDDIO	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	KΩ

6.1.6. DC electrical characteristics for 1.1 volts operation (for FORCE_ON and 32K_OUT)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		0.99	1.1	1.21	V
V_{IL}	Input low voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	130		560	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.1 V	130		560	KΩ

6.2. Analog characteristics

6.2.1. SMPS DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_DCV	SMPS input supply voltage	2.8	3.3	4.3	V	
DCV	SMPS output	1.74	1.84	1.94	V	
I_{CC}	SMPS output current	-	-	100	mA	
ΔV_PWM	Ripple of PWM mode	-	-	40	mV	With L=1uH, C=4.7uF
ΔV_PFM	Ripple of PFM mode	-	-	90	mV	With L=1uH, C=4.7uF

6.2.2. TCXO LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_VBAT	TCXO LDO input supply voltage	2.8	3.3	4.3	V	Will change to bypass mode under 3.1 volts
AVDD28_TLDO	TCXO LDO output	2.71	2.8	2.89	V	
I_{cc}	LDO output current	-	-	50	mA	Not including external devices
	PSRR-30 KHz	35	-	-	dB	Co = 1 uF, ESR = 0.05, Iload = 25 mA
	Load regulation	-84	10	84	mV	

6.2.3. TCXO SWITCH DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_TLDO	2.66	-	-	V	
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_CLDO	1.71	-	-	V	
I_{max}	TCXO SWITCH current limit	-	-	30	mA	

6.2.4. 1.1 volts core LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD28_CLDO	1.2 volts LDO input supply voltage	1.62	1.8	3.08	V	
AVDD11_CLDO	1.1 volts LDO output	1.05	1.12	1.2	V	
I_{cc}	LDO output current	-	-	50	mA	
	Load regulation	-	-	-	mV	

6.2.5. 1.1 volts RTC LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_RTC	RTC LDO input supply voltage	2	4	4.3	V	
AVDD11_RTC	RTC LDO output	0.99	1.1	1.21	V	
I_{cc}	LDO output current	-	-	3	mA	
I_{leak}	Leakage current	2.2	15	25	uA	Including LDO and RTC domain circuit, at 25 degree room temperature

6.2.6.   32 kHz crystal oscillator (XOSC32)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD11_RTC	Analog power supply	0.99	-	1.21	V	
Dcyc	Duty cycle	-	50	-	%	

7. Interface Characteristics

7.1. RS-232 interface timing

Required baud rate (bps)	Programmed baud rate (bps)	Baud rate error (%)	Baud rate error (%)
4,800	4,800.000	0.0000	0.002
9,600	9,600.000	0.0000	0.002
14,400	14,408.451	0.0587	0.0567
19,200	19,164.319	0.0587	0.0567
38,400	38,422.535	0.0587	0.0567
57,600	57,633.803	0.0587	0.0567
115,200	115,267.606	0.0587	0.0567
230,400	230,535.211	0.0587	0.0567
460,800	454,666.667	-1.3310	-1.3330
921,600	909,333.333	-1.3310	-1.3330

Notes:

1) UART baud rate settings with UART_CLK frequency = 16.368 MHz (UART_CLK uses the system reference clock).

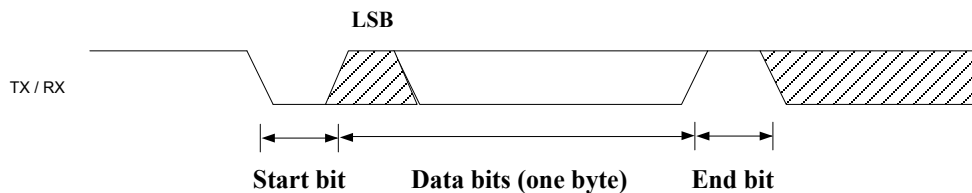2) The baud rate error is optimized. Each baud rate needs to adjust its counter to obtain the optimized error.

Figure 7-1: Timing diagram of the RS-232 interface

7.2. SPI interface timing

Description	Symbol	Min.	Max.	Unit	Note
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T – 3t	0.5T - 2t	ns	1, 2
SO hold time	T4	0.5T + 2t	0.5T + 3t	ns	1, 2
SIN setup time	T5	3t	-	ns	1, 2
SIN hold time	T6	10	-	ns	1

Notes:

1) The definition of SPI clock cycle (T) is (SPI_IPLL/12) MHz ~ (rf_clk/1,020) MHz.

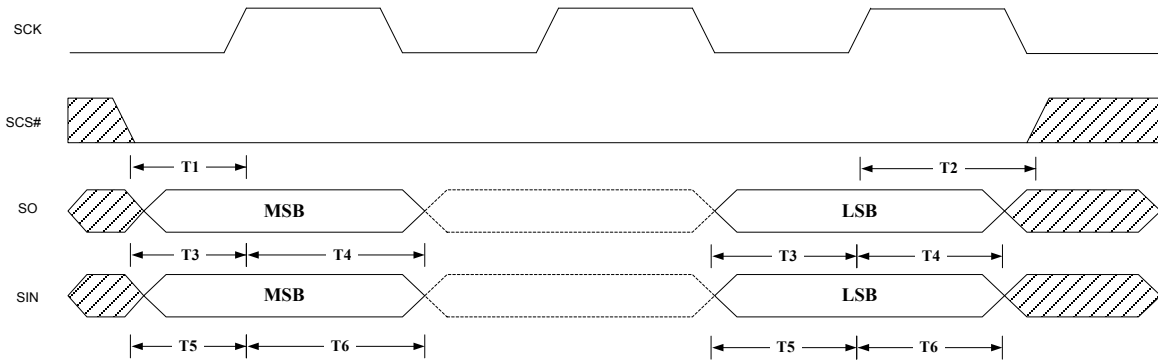2) It indicates the period of SPI controller clock, which is SPI_IPLL clock or `rf_clk`.

Figure 7-2: Timing diagram of the SPI interface

7.3. I2C interface timing

Symbol	Period
T1	(MM_CNT_PHASE_VAL0+1)/TCXO_CLK
T2	(MM_CNT_PHASE_VAL1+1)/TCXO_CLK
T3	(MM_CNT_PHASE_VAL2+1)/TCXO_CLK
T4	(MM_CNT_PHASE_VAL3+1)/TCXO_CLK

Note: The condition of I2C clock cycle (I2C_CLK) is (TCXO_CLK/4) MHz ~ (TCXO_CLK/(MM_CNT+4)) MHz. The MM_CNT is the sum of MM_CNT_PHASE_VAL0, MM_CNT_PHASE_VAL1, MM_CNT_PHASE_VAL2 and MM_CNT_PHASE_VAL3 in full speed mode.
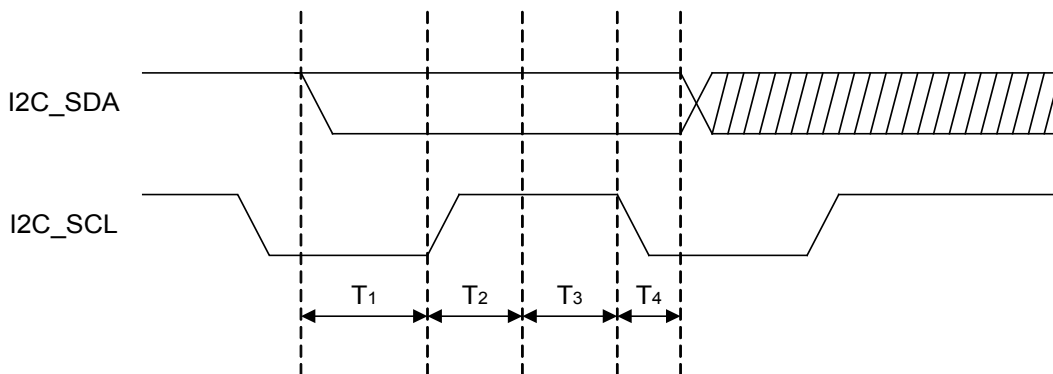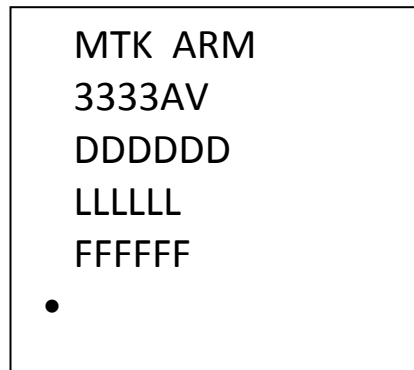

Figure 7-3: Timing diagram of the I2C interface

8. Package Description

8.1. Ordering information

Order #	Marking	Temp. range	Package
MT3333AV		-40 ~ +85 ℃	VFBGA

8.2. Top mark

```
MTK  ARM
3333AV
DDDDD
LLLLLL
FFFFFF
   ●
```

A :	8M NOR flash
V :	VFBGA package
DDDDD :	Date code
LLLLLL :	U1 Lot number
FFFFFF :	U2 Lot number

ESD CAUTION

MT3333 is an electrostatic discharge (ESD) sensitive device and may be damaged by ESD or spike voltage. Although MT3333 has built-in ESD protection circuitry, please handle with care to avoid performance degradation or permanent malfunction.

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