



DOUBLE DATA RATE (DDR) SDRAM

MT46V16M8 – 4 Meg x 8 x 4 banks
For the latest data sheet revisions, please refer to the Micron Website: www.micron.com/dramds

FEATURES

- 200 MHz Clock, 400 Mb/s/p data rate
- $V_{DD} = +2.65V \pm 0.10V$
- $V_{DDQ} = +2.65V \pm 0.10V$
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- $\overline{\text{RAS}}$ lockout ($\overline{\text{RAP}} = \overline{\text{RCD}}$)

OPTIONS

- | | PART NUMBER |
|--|--------------------|
| • Configuration
16 Meg x 8 (4 Meg x 8 x 4 banks) | 16M8 |
| • Plastic Package
66-Pin TSOP
(400mil with 0.65mm pin pitch) | TG |
| • Timing - Cycle Time
5ns @ CL = 3 ⁽¹⁾ | -5 |
| • Self Refresh
Standard | none |

NOTE: 1. Supports modules with 3-4-4 timing

GENERAL DESCRIPTION

The DDR400 SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 200 MHz ($t_{CK}=5\text{ns}$) with a peak data transfer rate of 400Mb/s. DDR400 continues to use the JEDEC standard SSTL_2 interface and the $2n$ -prefetch architecture.

The standard DDR200/DDR266 data sheets also pertain to the DDR400 device and should be referenced for a complete description of DDR SDRAM functionality and operating modes. However, to meet the faster DDR400 operating frequencies, some of the AC timing parameters, DC levels and operating temperatures are slightly tighter. This addendum data sheet will concentrate on the key differences required to support the enhanced speeds.

The Micron 128Mb data sheet provides full specifications and functionality unless specified herein.

CONFIGURATION

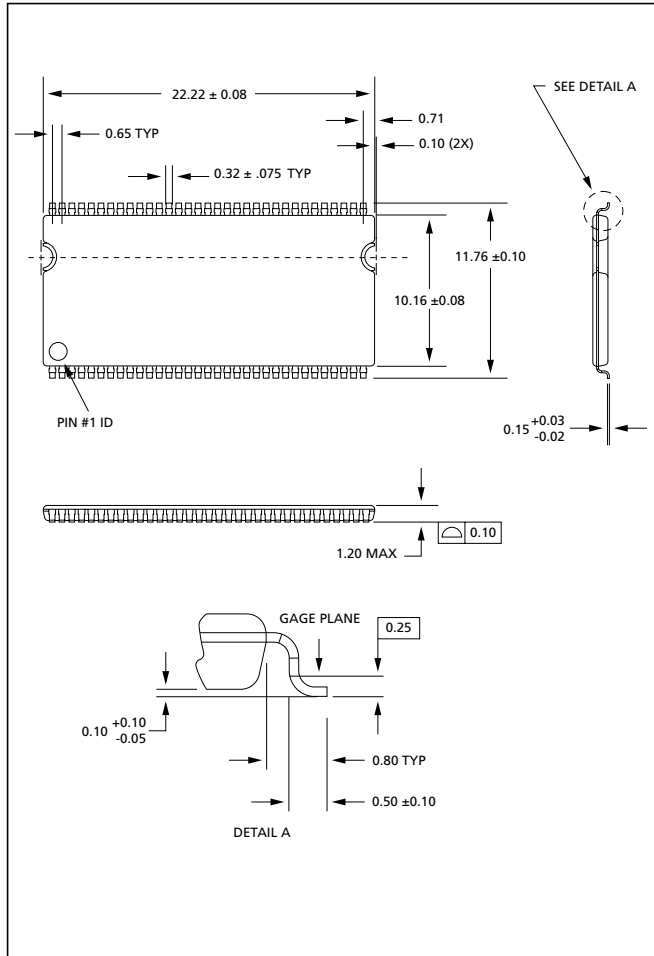
Architecture	16 Meg x 8
Configuration	4 Meg x 8 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	1K (A0–A9)

KEY TIMING PARAMETERS

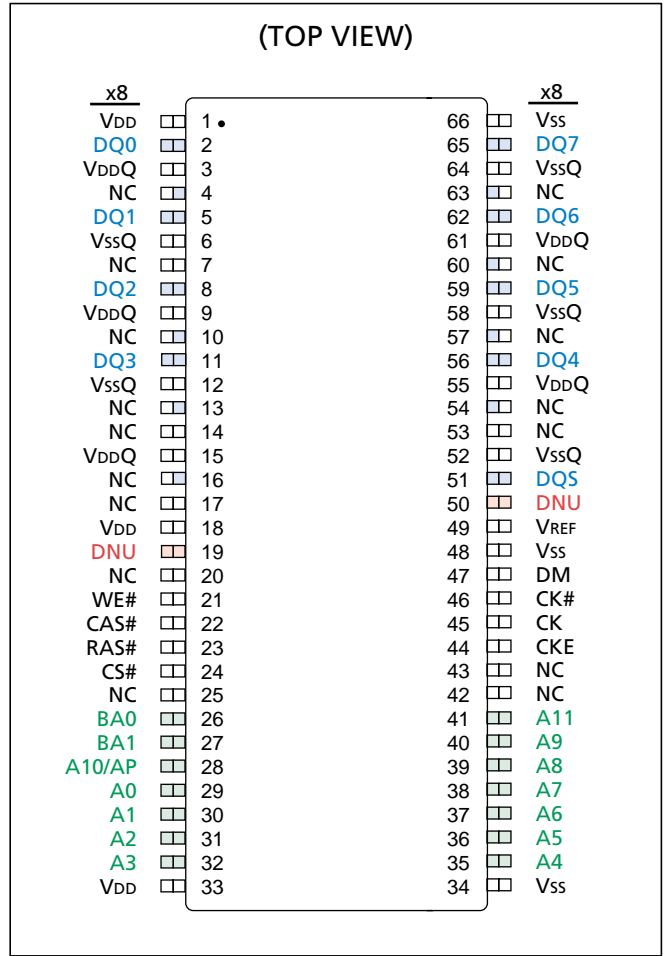
SPEED GRADE	CLOCK RATE	DATA-OUT WINDOW ²	ACCESS WINDOW	DQS-DQ SKEW
	CL = 3 ¹			
-5	200 MHz	2.15ns	±0.50ns	+0.35ns

- NOTE:** 1. CL = CAS (Read) Latency
2. With a 50/50 clock duty cycle

66-PIN TSOP PACKAGE DIMENSION



66-PIN TSOP PACKAGE PIN ASSIGNMENT



- NOTE:**
1. All dimensions in millimeters.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V _{DD} is applied.
24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
47	DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29-32 32, 35, 36 36, 38, 39 40, 29, 41	A0, A1, A2 A3, A4, A5 A6, A7, A8 A9, A10, A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
2, 5, 8 11, 56, 59 62, 65	DQ0-2 DQ3-5 DQ6-7	I/O	Data Input/Output.
51	DQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.

(continued on next page)



PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 7, 10, 13, 14, 16, 17, 20, 20, 25, 42, 43, 53, 54, 57, 60, 63	NC	-	No Connect: These pins should be left unconnected.
19, 50	DNU	-	Do Not Use: Must float to minimize noise on Vref
3, 9, 15, 55, 61	V _{DDQ}	Supply	DQ Power Supply: +2.65V ±0.10V. Isolated on the die for improved noise immunity.
6, 12, 52, 58, 64	V _{SSQ}	Supply	DQ Ground. Isolated on the die for improved noise immunity.
1, 18, 33	V _{DD}	Supply	Power Supply: +2.65V ±0.10V.
4, 48, 66	V _{SS}	Supply	Ground.
49	V _{REF}	Supply	SSTL_2 reference voltage.

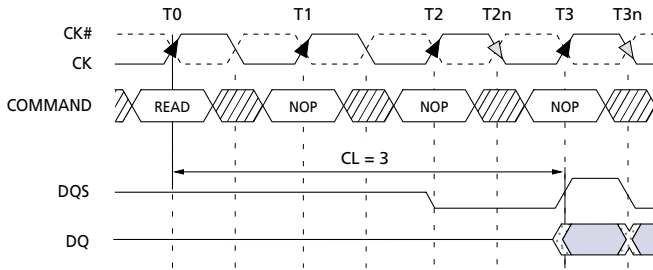
READ LATENCY

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in the CAS Latency Diagram and Mode Register Definition Diagram.

If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

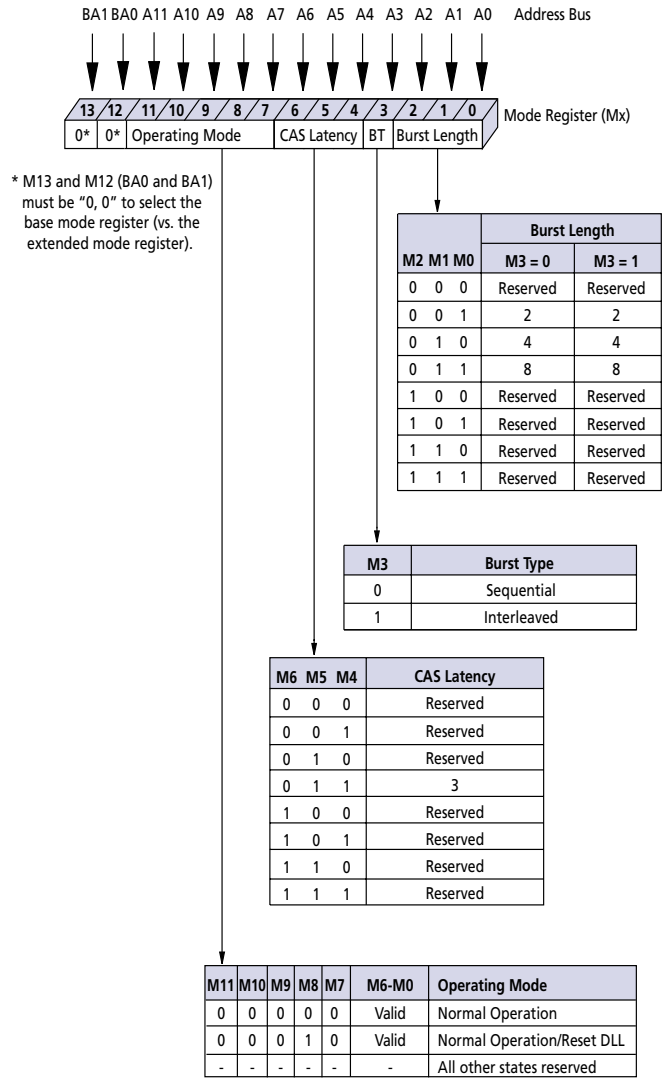
CAS Latency Diagram



Burst Length = 4 in the cases shown
Shown with nominal t_{AC} and nominal t_{DSDQ}

TRANSITIONING DATA DON'T CARE

Mode Register Definition Diagram





ABSOLUTE MAXIMUM RATINGS*

V_{DD} Supply Voltage Relative to V_{SS}..... -1V to +3.6V
 V_{DDQ} Supply Voltage Relative to V_{SS}.... -1V to +3.6V
 V_{REF} and Inputs Voltage Relative to V_{SS} .. -1V to +3.6V
 I/O Pins Voltage Relative to V_{SS} . -0.5V to V_{DDQ} +0.5V
 Operating Temperature, T_A (ambient) .. 0°C to +50°C
 Storage Temperature (plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1–5, 16; refer to DDR200/266 data sheet for all notes)
 (0°C ≤ T_A ≤ +50°C; V_{DD} = +2.65V ±0.10V, V_{DDQ} = +2.65V ±0.10V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{DD}	2.55	2.75	V	36, 41
I/O Supply Voltage	V _{DDQ}	2.55	2.75	V	36, 41, 44
I/O Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V	6, 44
I/O Termination Voltage (system)	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V	7, 44
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.15	V _{DD} + 0.3	V	28
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	V _{REF} - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	I _I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-5	5	µA	
OUTPUT LEVELS: Full drive option - x8 High Current (V _{OUT} = V _{DDQ} -0.373V, minimum V _{REF} , minimum V _{TT}) Low Current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OH} I _{OL}	-16.8 16.8	- -	mA mA	37, 39

AC INPUT OPERATING CONDITIONS

(Notes: 1–5, 16; refer to DDR200/266 data sheet for all notes)
 (0°C ≤ T_A ≤ +50°C; V_{DD} = +2.65V ±0.10V, V_{DDQ} = +2.65V ±0.10V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} + 0.310	-	V	14, 28, 40
Input Low (Logic 0) Voltage	V _{IL(AC)}	-	V _{REF} - 0.310	V	14, 28, 40
I/O Reference Voltage	V _{REF(AC)}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V	6



CAPACITANCE (TSOP)

(Notes: 1-5, 14-17, 33; refer to DDR200/266 data sheet for all notes)
($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.65\text{V} \pm 0.10\text{V}$, $V_{DD} = +2.65\text{V} \pm 0.10\text{V}$)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance:					
DQs, DQS, DM	DC _{IO}	–	0.50	pF	13, 24
DQ0-DQ7	DC _{IO}	–	0.50	pF	13, 24
Delta Input Capacitance: Command and Address	DC _{I1}	–	0.50	pF	13, 29
Delta Input Capacitance: CK, CK#	DC _{I2}	–	0.25	pF	13, 29
Input/Output Capacitance: DQs, DQS, DM	C _{IO}	4.0	5.0	pF	13
Input Capacitance: Command and Address	C _{I1}	2.0	3.0	pF	13
Input Capacitance: CK, CK#	C _{I2}	2.0	3.0	pF	13
Input Capacitance: CKE	C _{I3}	2.0	3.0	pF	13



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1-5, 14-17, 33; refer to DDR200/266 data sheet for all notes)
(0°C ≤ T_A ≤ 50°C; V_{DDQ} = +2.65V ±0.10V, V_{DD} = +2.65V ±0.10V)

AC CHARACTERISTICS PARAMETER	SYMBOL	-5 (TSOP)		UNITS	NOTES
		MIN	MAX		
Access window of DQs from CK/CK#	t ^{AC}	-0.6	+0.6	ns	
CK high-level width	t ^{CH}	0.45	0.55	t ^{CK}	30
CK low-level width	t ^{CL}	0.45	0.55		
Clock cycle time	t ^{CK}	5	5	ns	45,52
DQ and DM input hold time relative to DQS	t ^{DH}	0.45	na	ns	26,31
DQ and DM input setup time relative to DQS	t ^{DS}	0.45		ns	26,31
DQ and DM input pulse width (for each input)	t ^{DIPW}	1.4		ns	31
Access window of DQS from CK/CK#	t ^{DQSCK}	-0.50	+0.50	ns	
DQS input high pulse width	t ^{DQSH}	0.4		t ^{CK}	
DQS input low pulse width	t ^{DQSL}	0.4		t ^{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access	t ^{DQSQ}		0.35	ns	25, 26
Write command to first DQS latching transition	t ^{DQSS}	0.75	1.25	t ^{CK}	
DQS falling edge to CK rising - setup time	t ^{DSS}	0.22		t ^{CK}	
DQS falling edge from CK rising - hold time	t ^{DSH}	0.22		t ^{CK}	
Half clock period	t ^{HP}	t ^{CH} , t ^{CL}		ns	34
Data-out high-impedance window from CK/CK#	t ^{HZ}		+0.60	ns	18,42
Data-out low-impedance window from CK/CK#	t ^{LZ}	-0.60		ns	18,43
Address and control input hold time (fast slew rate)	t ^{IH_F}	0.75		ns	14
Address and control input setup time (fast slew rate)	t ^{IS_F}	0.75		ns	14
Address and control input hold time (slow slew rate)	t ^{IH_S}	na		ns	14
Address and control input setup time (slow slew rate)	t ^{IS_S}	na		ns	14
Address and control input pulse width	t ^{IPW}	1.8		ns	
LOAD MODE REGISTER command cycle time	t ^{MRD}	10		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t ^{QH}	t ^{HP} - t ^{QHS}		ns	25, 26
Data Hold Skew Factor	t ^{QHS}		0.50	ns	
ACTIVE to AUTOPRECHARGE command	t ^{RAP}	20		ns	46
ACTIVE to PRECHARGE command	t ^{RAS}	40	70,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period	t ^{RC}	60		ns	
AUTO REFRESH command period	t ^{RFC}	70		ns	50
ACTIVE to READ or WRITE delay	t ^{RCD}	20		ns	
PRECHARGE command period	t ^{RP}	20		ns	
DQS read preamble	t ^{RPRE}	0.9	1.1	t ^{CK}	42
DQS read postamble	t ^{RPST}	0.4	0.6	t ^{CK}	
ACTIVE bank a to ACTIVE bank b command	t ^{RRD}	10		ns	
DQS write preamble	t ^{WPRE}	0.25		t ^{CK}	
DQS write preamble setup time	t ^{WPRES}	0		ns	20, 21
DQS write postamble	t ^{WPST}	0.4	0.6	t ^{CK}	19
Write recovery time	t ^{WR}	15		ns	
Internal WRITE to READ command delay	t ^{WTR}	2		t ^{CK}	
Data valid output window	na	t ^{QH} - t ^{DQSQ}		ns	25
REFRESH to REFRESH command interval	t ^{REFC}		140.6	μs	23
Average periodic refresh interval	t ^{REFI}		15.6	μs	23
Terminating voltage delay to V _{DD}	t ^{VTD}	0		ns	
Exit SELF REFRESH to non-READ command	t ^{XSNR}	75		ns	
Exit SELF REFRESH to READ command	t ^{XSRD}	200		t ^{CK}	



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
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