SYNCHRONOUS DRAM

MT48LC8M16A2 – 2 MEG X 16 X 4 BANKS

For the latest data sheet, please refer to the Micron Web site: www.micron.com/dramds

FEATURES

- Supports PC100 and PC133 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode; standard and low power
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- 64ms, 4,096-cycle refresh

OPTION / MARKING

- Configuration
  8 Meg x 16 (2 Meg x 16 x 4 banks) — 8M16
  WRITE Recovery (^{t}WR) — A2
  ^{t}WR = "2 CLK"[1]
- Package
  Plastic Package – OCPL[2]
  54-pin TSOP II (400 mil) — TG
- Timing (Cycle Time)
  6.0ns @ CL = 3 — -6A
- Self Refresh
  Standard — None
- Operating Temperature Range
  Commercial (0°C to +70°C) — None

NOTE:

1. Refer to Micron Technical Note: TN-48-05.
2. Off-center parting line.

Part Number:

MT48LC8M16A2TG-6A

ADDENDUM CHANGES

The standard 128Mb SDRAM data sheets also pertain to the x16 device and should be referenced for a complete description of SDRAM functionality and operating modes. However, to meet the faster speed grades, some of the AC timing parameters are slightly different. This addendum data sheet will concentrate on the key differences required to support the enhanced speeds.

The Micron 128Mb data sheet provides full specifications and functionality unless specified herein.

	8 MEG X 16
Configuration	2 Meg x 16 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	512 (A0–A8)

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-6A	167 MHz	5.4ns	1.5ns	0.8ns

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IDD SPECIFICATIONS AND CONDITIONS

Notes: 1, 5, 6, 11, 13; notes appear in the standard data sheet; $V_{DD}/V_{DD}Q$ = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	-6A	UNITS	NOTES
Operating Current: Active Mode; Burst = 2; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}	170	mA	3, 18, 19, 32
Standby Current: Power-Down Mode; All banks idle; CKE = LOW		I_{DD2}	2	mA	32
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}	50	mA	3, 12, 19, 32
Operating Current: Burst Mode; Continuous burst; READ or WRITE; All banks active		I_{DD4}	165	mA	3, 18, 19, 32
Auto Refresh Current CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	I_{DD5}	330	mA	3, 12, 18, 19, 32, 33
	^{t}RFC = 15.625µs	I_{DD6}	3	mA	
Self Refresh Current: CKE ≤ 0.2V	Standard	I_{DD7}	2	mA	4

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes 5, 6, 8, 9,11; Notes appear on in the standard data sheet

AC CHARACTERISTICS			-6A			
PARAMETER		SYMBOL	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	$^tAC(3)$		5.4	ns	27
Address hold time		^tAH	0.8		ns	
Address setup time		^tAS	1.5		ns	
CLK high-level width		^tCH	2.5		ns	
CLK low-level width		^tCL	2.5		ns	
Clock cycle time	CL = 3	$^tCK(3)$	6		ns	23
CKE hold time		^tCKH	0.8		ns	
CKE setup time		^tCKS	1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		ns	
Data-in hold time		^tDH	0.8		ns	
Data-in setup time		^tDS	1.5		ns	
Data-out high-impedance time	CL = 3	$^tHZ(3)$		5.4	ns	10
Data-out low-impedance time		^tLZ	1		ns	
Data-out hold time (load)		^tOH	3		ns	
Data-out hold time (no load)		^tOH_N	1.8		ns	28
ACTIVE to PRECHARGE command		^tRAS	42	120,000	ns	
ACTIVE to ACTIVE command period		^tRC	60		ns	
ACTIVE to READ or WRITE delay		^tRCD	18		ns	
Refresh period (4,096 rows)		^tREF		64	ms	
AUTO REFRESH period		^tRFC	60		ns	
PRECHARGE command period		^tRP	18		ns	
ACTIVE bank a to ACTIVE bank b command		^tRRD	12		ns	7
Transition time		^tT	0.3	1.2	ns	
WRITE recovery time[1]		^tWR	1 CLK + 6ns		ns	
			12		ns	25
Exit SELF REFRESH to ACTIVE command		^tXSR	67		ns	20

NOTE:

1. Auto precharge mode only. The precharge timing budget (^tRP) begins 6ns for -6A after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.

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AC FUNCTIONAL CHARACTERISTICS

Notes appear in the standard data sheet.

PARAMETER	SYMBOL	-6A SPEED	UNITS	NOTES
READ/WRITE command to READ/WRITE command	^{t}CCD	1	^{t}CK	17
CKE to clock disable or power-down entry mode	^{t}CKED	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode	^{t}PED	1	^{t}CK	14
DQM to input data delay	^{t}DQD	0	^{t}CK	17
DQM to data mask during WRITEs	^{t}DQM	0	^{t}CK	17
DQM to data high-impedance during READs	^{t}DQZ	2	^{t}CK	17
WRITE command to input data delay	^{t}DWD	0	^{t}CK	17
Data-in to ACTIVE command	^{t}DAL	5	^{t}CK	15, 21[1]
Data-in to PRECHARGE command	^{t}DPL	2	^{t}CK	16, 21
Last data-in to burst STOP command	^{t}BDL	1	^{t}CK	17
Last data-in to new READ/WRITE command	^{t}CDL	1	^{t}CK	17
Last data-in to PRECHARGE command	^{t}RDL	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command	^{t}MRD	2	^{t}CK	26
Data-out to high-impedance from PRECHARGE command (CL=3)	^{t}ROH(3)	3	^{t}CK	17

NOTE:

1. The Note 21 in the standard data sheet does not apply for this speed grade and should read "Based on ^{t}CK = 6ns"

DATA SHEET DESIGNATION

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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