

# DRAM

# 1 MEG x 4 DRAM

## STATIC-COLUMN

**DRAM**

### FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 275mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR), and HIDDEN
- STATIC-COLUMN access cycle

### OPTIONS

- Timing

70ns access	-7
80ns access	-8

- Packages

Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

- Part Number Example: MT4C4003JDJ-7

### MARKING

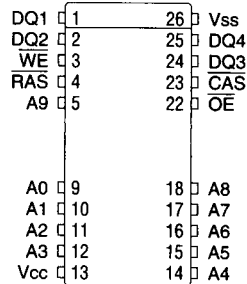
### GENERAL DESCRIPTION

The MT4C4003J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time.  $\overline{\text{RAS}}$  is used to latch the first 10 bits and  $\overline{\text{CAS}}$  the latter 10 bits. READ and WRITE cycles are selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin(s) remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the output pin(s), data-out (Q) is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains LOW (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by  $\overline{\text{WE}}$  and OE.

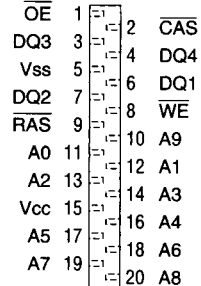
STATIC-COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a

### PIN ASSIGNMENT (Top View)

#### 20-Pin SOJ (DC-1)



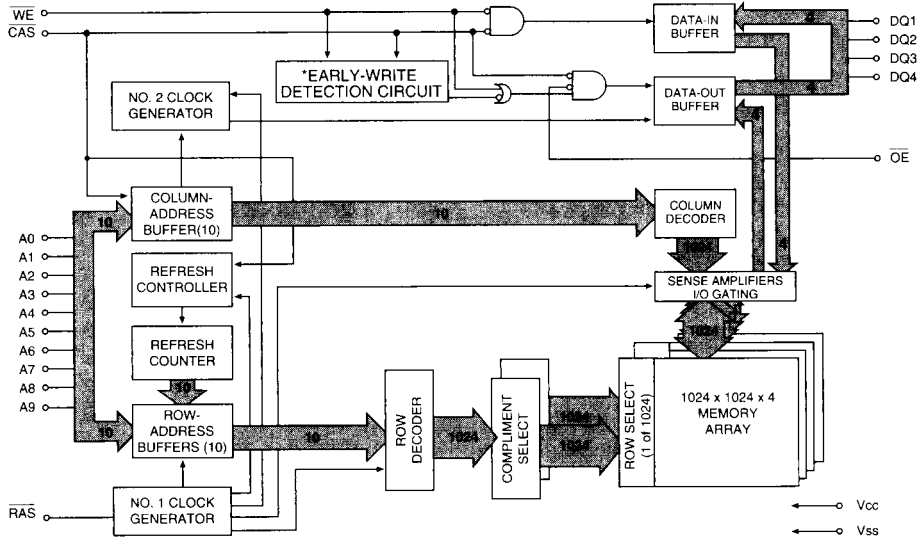
#### 20-Pin ZIP (DB-2)



row-address-defined (A0-A9) page boundary. After the first read, any column-address transition will result in new data-out. Unlike PAGE-MODE, which requires  $\overline{\text{CAS}}$  to be toggled for each successive PAGE-MODE access, STATIC-COLUMN allows  $\overline{\text{CAS}}$  to be left LOW for successive STATIC-COLUMN accesses. Returning  $\overline{\text{RAS}}$  HIGH terminates the STATIC-COLUMN operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE) or  $\overline{\text{RAS}}$  REFRESH cycle ( $\overline{\text{RAS}}$ -ONLY, CBR, or HIDDEN) so that all 1,024 combinations of  $\overline{\text{RAS}}$  addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic  $\overline{\text{RAS}}$  addressing.

**FUNCTIONAL BLOCK DIAGRAM**  
**STATIC-COLUMN**



- \*NOTE:** 1.  $\overline{WE}$  LOW prior to  $\overline{CAS}$  LOW, EW detection circuit output is a HIGH (EARLY-WRITE)  
2.  $\overline{CAS}$  LOW prior to  $\overline{WE}$  LOW, EW detection circuit output is a LOW (LATE-WRITE)

**TRUTH TABLE**

FUNCTION	RAS	CAS	WE	OE	ADDRESSES		DATA-IN/OUT	
					r	c	DQ1-DQ4	
Standby	H	H→X	X	X	X	X	High-Z	
READ	L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE	L	L	L	X	ROW	COL	Data-In	
READ-WRITE	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	
STATIC-COLUMN READ	1st Cycle	L	L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	L	H	L	n/a	COL	Data-Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	X	ROW	COL	Data-In
	2nd Cycle	L	L	L	X	n/a	COL	Data-In
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH	L	H	X	X	ROW	n/a	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH	H→L	L	H	X	X	X	High-Z	

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to V<sub>SS</sub> ..... -1V to +7V  
 Operating Temperature, T<sub>A</sub> (ambient) ..... 0°C to +70°C  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 3, 4, 6, 7) (V<sub>CC</sub> = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V <sub>IH</sub>	2.4	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ 6.5V (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 5.5V)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS					
Output High Voltage (I <sub>OUT</sub> = -5mA)	V <sub>OH</sub>	2.4		V	
Output Low Voltage (I <sub>OUT</sub> = 4.2mA)	V <sub>OL</sub>		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-7	-8		
STANDBY CURRENT: (TTL) (RAS = CAS = V <sub>IH</sub> )	I <sub>CC1</sub>	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = V <sub>CC</sub> - 0.2V)	I <sub>CC2</sub>	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC [MIN])	I <sub>CC3</sub>	100	90	mA	3, 4, 28
OPERATING CURRENT: STATIC-COLUMN Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC [MIN])	I <sub>CC4</sub>	70	60	mA	3, 4, 28
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V <sub>IH</sub> : 'RC = 'RC [MIN])	I <sub>CC5</sub>	100	90	mA	3, 28
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC [MIN])	I <sub>CC6</sub>	100	90	mA	3, 5

**CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C <sub>I1</sub>		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C <sub>I2</sub>		7	pF	2
Input/Output Capacitance: DQ	C <sub>IO</sub>		7	pF	2

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.V ±10%)

**DRAM**

AC CHARACTERISTICS	SYM	-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	<sup>1</sup> RC	130		150		ns	
READ-WRITE cycle time	<sup>1</sup> RWC	185		205		ns	
STATIC-COLUMN READ or WRITE cycle time	<sup>1</sup> SC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	<sup>1</sup> SRWC	100		110		ns	
Access time from $\overline{\text{RAS}}$	<sup>1</sup> RAC		70		80	ns	14
Access time from $\overline{\text{CAS}}$	<sup>1</sup> CAC		20		20	ns	15
Output Enable	<sup>1</sup> OE		20		20	ns	23
Access time from column-address	<sup>1</sup> AA		35		40	ns	
$\overline{\text{RAS}}$ pulse width	<sup>1</sup> RAS	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ pulse width (STATIC-COLUMN)	<sup>1</sup> RASC	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time	<sup>1</sup> RSH	20		20		ns	
$\overline{\text{RAS}}$ precharge time	<sup>1</sup> RP	50		60		ns	
$\overline{\text{CAS}}$ pulse width	<sup>1</sup> CAS	20	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	<sup>1</sup> CSH	70		80		ns	
$\overline{\text{CAS}}$ precharge time	<sup>1</sup> CPN	10		10		ns	16
$\overline{\text{CAS}}$ precharge time (STATIC-COLUMN)	<sup>1</sup> CP	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	<sup>1</sup> RCD	20	50	20	60	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	<sup>1</sup> CRP	10		10		ns	
Row-address setup time	<sup>1</sup> ASR	0		0		ns	
Row-address hold time	<sup>1</sup> RAH	10		10		ns	
$\overline{\text{RAS}}$ to column-address delay time	<sup>1</sup> RAD	15	35	15	40	ns	18
Column-address setup time	<sup>1</sup> ASC	0		0		ns	
Column-address hold time	<sup>1</sup> CAH	15		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$ )	<sup>1</sup> AR	75		85		ns	
Column-address to $\overline{\text{RAS}}$ lead time	<sup>1</sup> RAL	35		40		ns	
Read command setup time	<sup>1</sup> RCS	0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$ )	<sup>1</sup> RCH	0		0		ns	19
Read command hold time (referenced to $\overline{\text{RAS}}$ )	<sup>1</sup> RRH	0		0		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	<sup>1</sup> CLZ	0		0		ns	
Output buffer turn-off delay	<sup>1</sup> OFF	3	20	3	20	ns	20, 29
Column-address hold time (referenced to $\overline{\text{RAS}}$ )	<sup>1</sup> AWR	55		60		ns	
$\overline{\text{WE}}$ command setup time	<sup>1</sup> WCS	0		0		ns	21, 27
Write command hold time	<sup>1</sup> WCH	15		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$ )	<sup>1</sup> WCR	55		60		ns	
Write command pulse width	<sup>1</sup> WP	15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	<sup>1</sup> RWL	20		20		ns	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

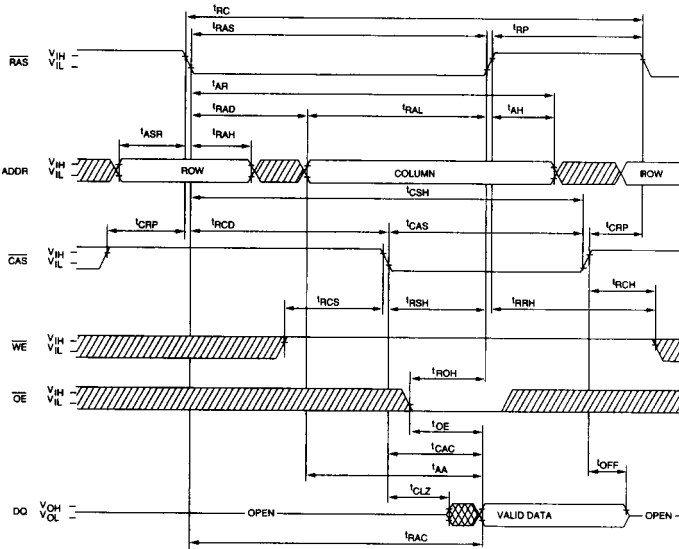
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ( $V_{CC} = 5V \pm 10\%$ )

AC CHARACTERISTICS PARAMETER	SYM	-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	20		20		ns	
Data-in setup time	$t_{DS}$	0		0		ns	22
Data-in hold time	$t_{DH}$	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$ )	$t_{DHR}$	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	100		110		ns	21
Column-address to $\overline{WE}$ delay time	$t_{AWD}$	65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	50		50		ns	21
Transition time (rise or fall)	$t_T$	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	$t_{REF}$		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	$t_{CSR}$	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	$t_{CHR}$	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	$t_{WRH}$	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	$t_{WRP}$	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	$t_{WTH}$	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	$t_{WTS}$	10		10		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	$t_{ORD}$	0		0		ns	
Output disable	$t_{OD}$		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	$t_{OEH}$	20		20		ns	26
Write inactive time	$t_{WI}$	10		10		ns	
Previous WRITE to column-address delay time	$t_{LWAD}$	20	30	20	35	ns	
Previous WRITE to column-address hold time	$t_{AHLW}$	65		75		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	$t_{ROH}$	10		10		ns	
Output data hold time from column-address	$t_{AOH}$	5		5		ns	
Output data enable from WRITE	$t_{OW}$	$t_{AA} + 5$		$t_{AA} + 5$		ns	
Access time from last WRITE	$t_{ALW}$	65		75		ns	
Column-address hold time referenced to $\overline{RAS}$ HIGH	$t_{AH}$	5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	$t_{CSC}$	$t_{CAS}$		$t_{CAS}$		ns	

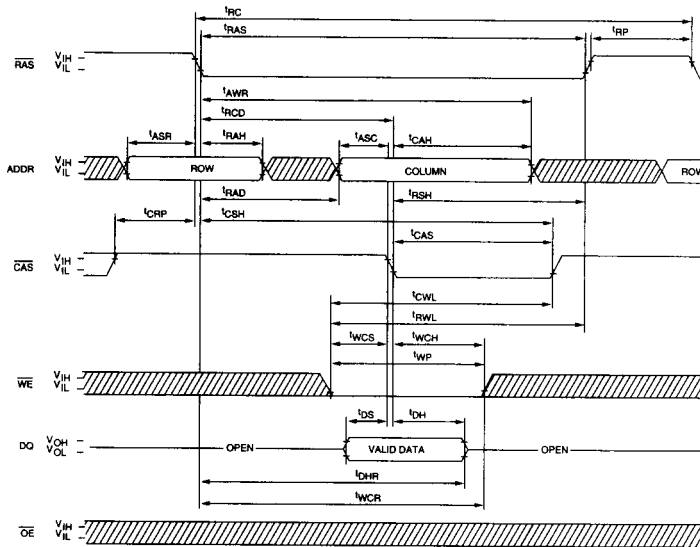
## NOTES

- All voltages referenced to  $V_{SS}$ .
- This parameter is sampled.  $V_{CC} = 5V \pm 10\%$ ;  $f = 1\text{ MHz}$ .
- $I_{CC}$  is dependent on cycle rates.
- $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of  $100\mu s$  is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$ -ONLY or CBR with  $\overline{WE}$  HIGH) before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
- AC characteristics assume  $t_T = 5ns$ .
- $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
- In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- If  $\overline{CAS} = V_{IH}$ , data output is High-Z.
- If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to two TTL gates and  $100pF$ .
- Assumes that  $t_{RCD} < t_{RCD} (MAX)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
- Assumes that  $t_{RCD} \geq t_{RCD} (MAX)$ .
- If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CPN}$ .
- Operation within the  $t_{RCD} (MAX)$  limit ensures that  $t_{RAC} (MAX)$  can be met.  $t_{RCD} (MAX)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD} (MAX)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation within the  $t_{RAD} (MAX)$  limit ensures that  $t_{RAC} (MIN)$  and  $t_{CAC} (MIN)$  can be met.  $t_{RAD} (MAX)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD} (MAX)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
- $t_{OFF} (MAX)$  defines the time at which the output achieves the open circuit condition, and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.  $t_{WCS}$  applies to EARLY-WRITE cycles.  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  apply to READ-MODIFY-WRITE cycles. If  $t_{WCS} \geq t_{WCS} (MIN)$ , the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD} (MIN)$ ,  $t_{AWD} \geq t_{AWD} (MIN)$  and  $t_{CWD} \geq t_{CWD} (MIN)$ , the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate.  $\overline{OE}$  held HIGH and  $\overline{WE}$  taken LOW after  $\overline{CAS}$  goes LOW results in a LATE-WRITE ( $\overline{OE}$ -controlled) cycle.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY-WRITE cycles and  $\overline{WE}$  leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If  $\overline{OE}$  is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{WE} = \text{LOW}$  and  $\overline{OE} = \text{HIGH}$ .
- $t_{WTS}$  and  $t_{WTH}$  are setup and hold specifications for the  $\overline{WE}$  pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of  $t_{WRP}$  and  $t_{WRH}$  in the CBR REFRESH cycle.
- LATE-WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OE}$  met ( $\overline{OE}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If  $\overline{OE}$  is taken back LOW while  $\overline{CAS}$  remains LOW, the DQs will remain open.
- The DQs open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur. If  $\overline{CAS}$  goes HIGH before  $\overline{OE}$ , the DQs will open regardless of the state of  $\overline{OE}$ . If  $\overline{CAS}$  stays LOW while  $\overline{OE}$  is brought HIGH, the DQs will open. If  $\overline{OE}$  is brought back LOW ( $\overline{CAS}$  still LOW), the DQs will provide the previously read data.
- Column-address changed one while  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$
- The  $3ns$  minimum is a parameter guaranteed by design.

## READ CYCLE

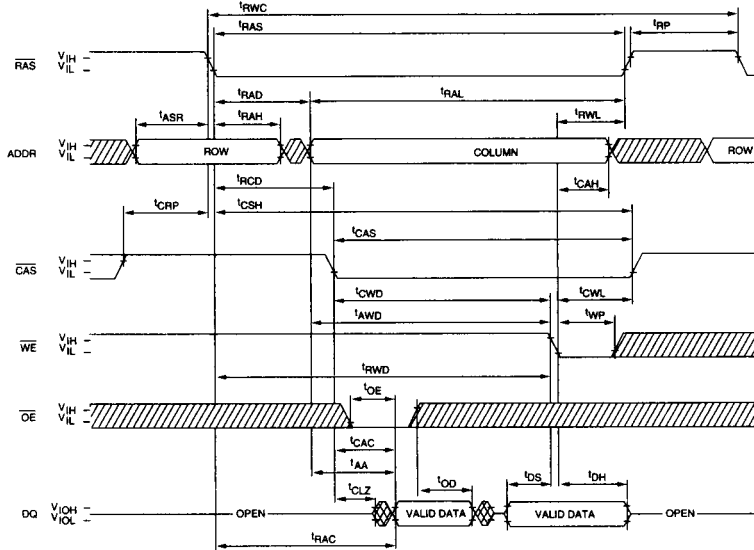


## EARLY-WRITE CYCLE

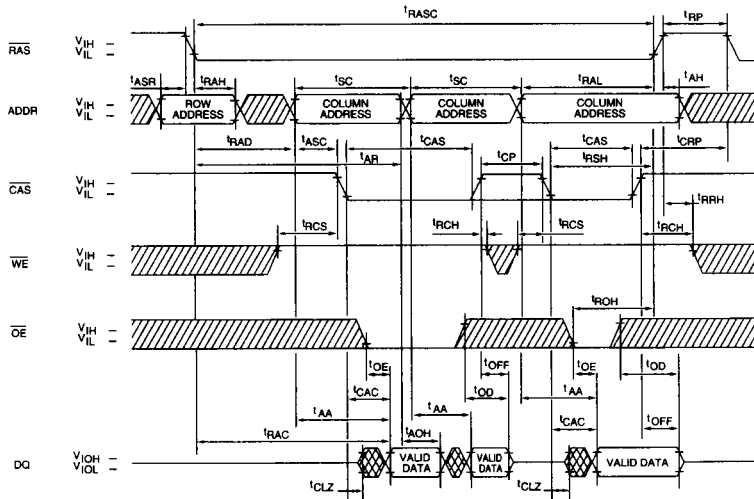


DON'T CARE  
 UNDEFINED

**READ-WRITE CYCLE**  
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



**STATIC-COLUMN READ CYCLE**

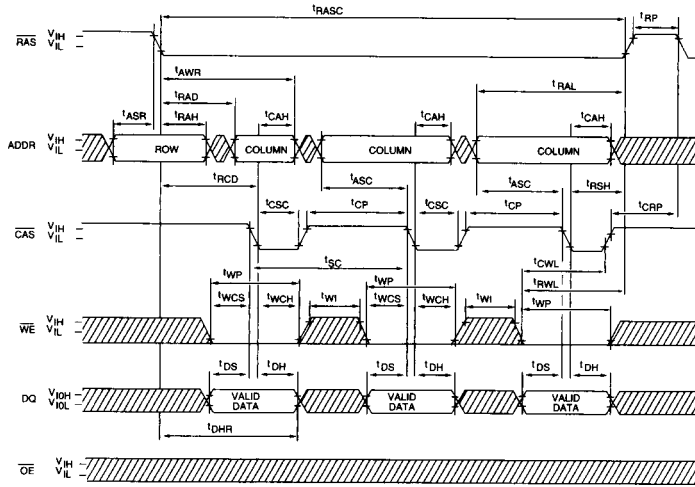


DON'T CARE  
 UNDEFINED

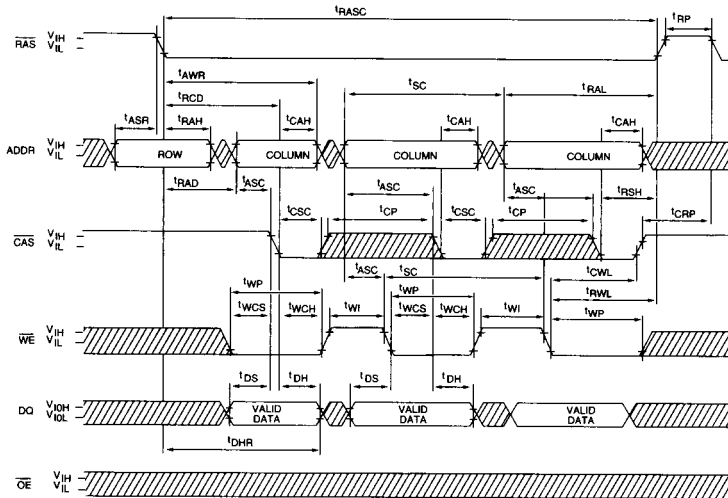
DRAM



**STATIC-COLUMN EARLY-WRITE CYCLE  
(CAS-Controlled)**

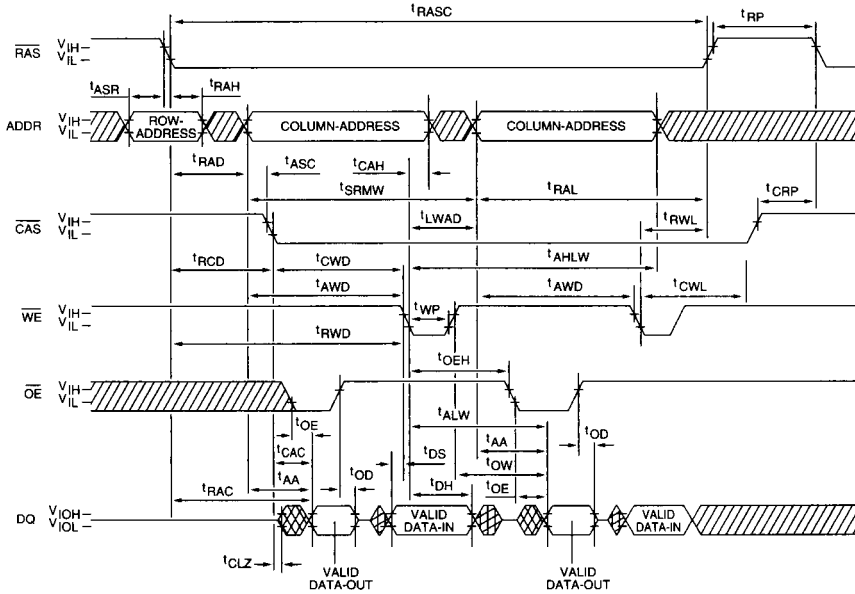


**STATIC-COLUMN EARLY-WRITE CYCLE  
(WE-Controlled)**

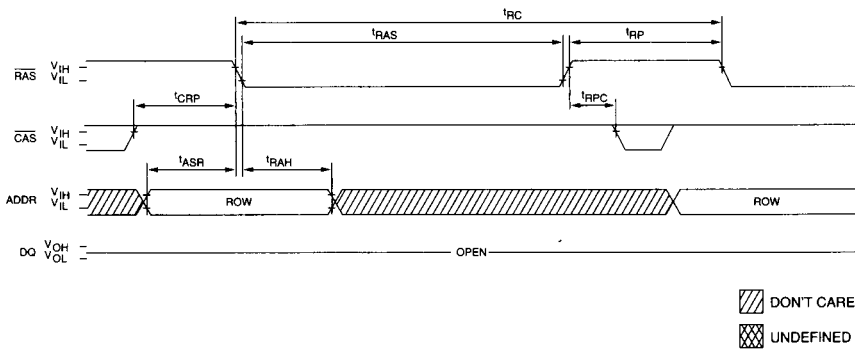


▨ DON'T CARE  
▩ UNDEFINED

**STATIC-COLUMN READ-WRITE CYCLE**  
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

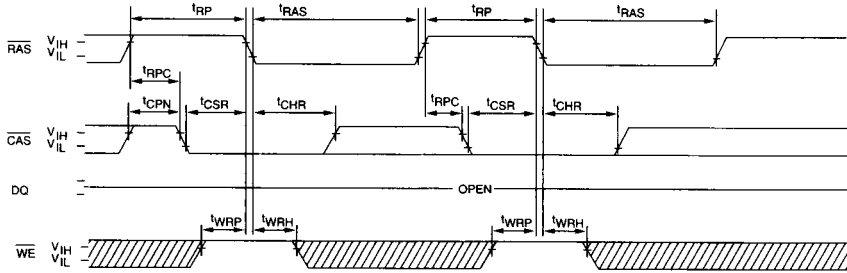


**RAS-ONLY REFRESH CYCLE**  
(ADDR = A0-A9; WE = DON'T CARE)

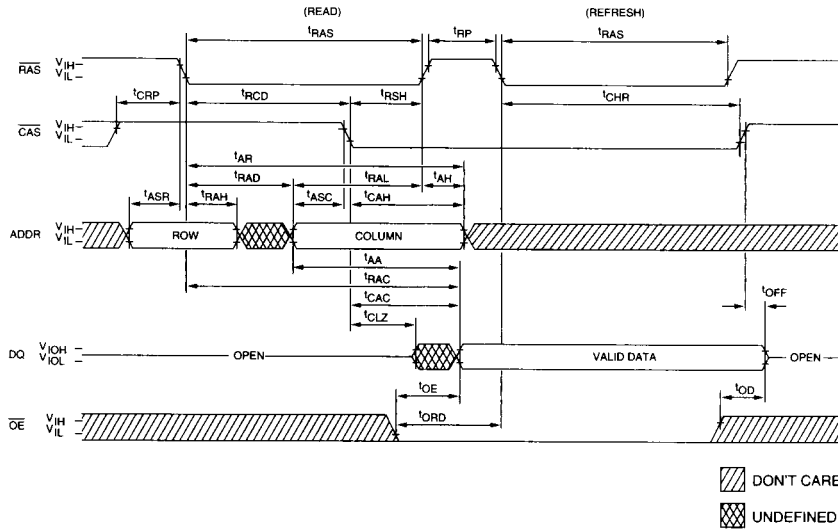


**DRAM**

**CBR REFRESH CYCLE**  
(A0-A9 and OE = DON'T CARE)



**HIDDEN REFRESH CYCLE<sup>24</sup>**  
(WE = HIGH; OE = LOW)



### 4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

#### REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the  $\overline{WE}$  pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the  $\overline{WE}$  pin held at a voltage HIGH level.

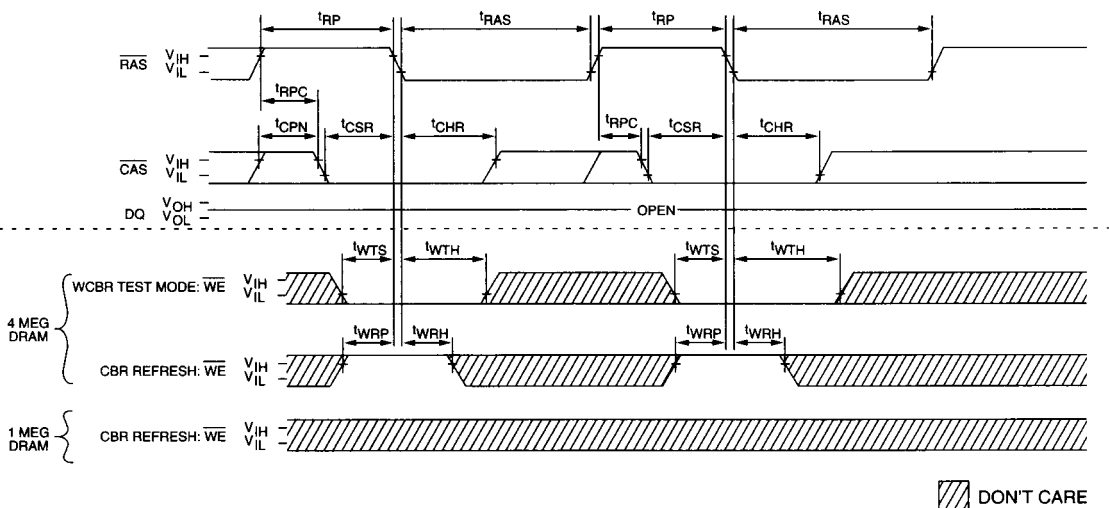
A CBR cycle with  $\overline{WE}$  LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

#### POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight  $\overline{RAS}$  cycles. The 4 Meg POWER-UP is more restrictive in that eight  $\overline{RAS}$ -ONLY REFRESH or CBR REFRESH ( $\overline{WE}$  held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a  $\overline{RAS}$ -ONLY REFRESH cycle or a CBR REFRESH cycle ( $\overline{WE}$  held HIGH).

#### SUMMARY

1. The 1 Meg CBR REFRESH allows the  $\overline{WE}$  pin to be "don't care" while the 4 Meg CBR requires  $\overline{WE}$  to be HIGH.
2. The eight  $\overline{RAS}$  wake-up cycles on the 1 Meg may be any valid  $\overline{RAS}$  cycle while the 4 Meg may only use  $\overline{RAS}$ -ONLY or CBR REFRESH cycles ( $\overline{WE}$  held HIGH).



### COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR