DRAM

1 MEG x 4 DRAM

QUAD CAS PARITY, FAST PAGE MODE

FEATURES

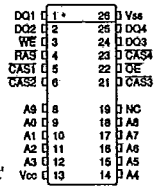
- Four independent $\overline{CAS}$ controls, allowing individual manipulation to each of the four data Input/Output ports (DQ1 through DQ4).
- Offers a single chip solution to byte level parity for 36-bit words when using 1 Meg x 4 DRAMs for memory
- Emulates write-per-bit, at design-in level, with simplified timing constraints
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles with $\overline{WE}$ as a don't care

OPTIONS — MARKING

- Timing
  - 70ns access — -7
  - 80ns access — -8
  - 100ns access — -10
- Packages
  - Plastic SOJ (300mil) — DJ
  - Plastic SOJ (350mil) — DJW
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-5, E-6)



NC = Pin is a 'no connect'

GENERAL DESCRIPTION

The MT4C4004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each $\overline{CAS}$ ($\overline{CAS1}$ through $\overline{CAS4}$) controls its corresponding data I/O port in conjunction with $\overline{OE}$ (eg. $\overline{CAS1}$ controls DQ1 I/O port, $\overline{CAS2}$ controls DQ2, $\overline{CAS3}$ controls DQ3 and $\overline{CAS4}$ controls DQ4).

The best way to view the Quad $\overline{CAS}$ function is to imagine the $\overline{CAS}$ inputs going into an AND gate to obtain an internally generated $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on a standard 1 Meg x 4 DRAM device. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$) on the Quad CAS DRAM.

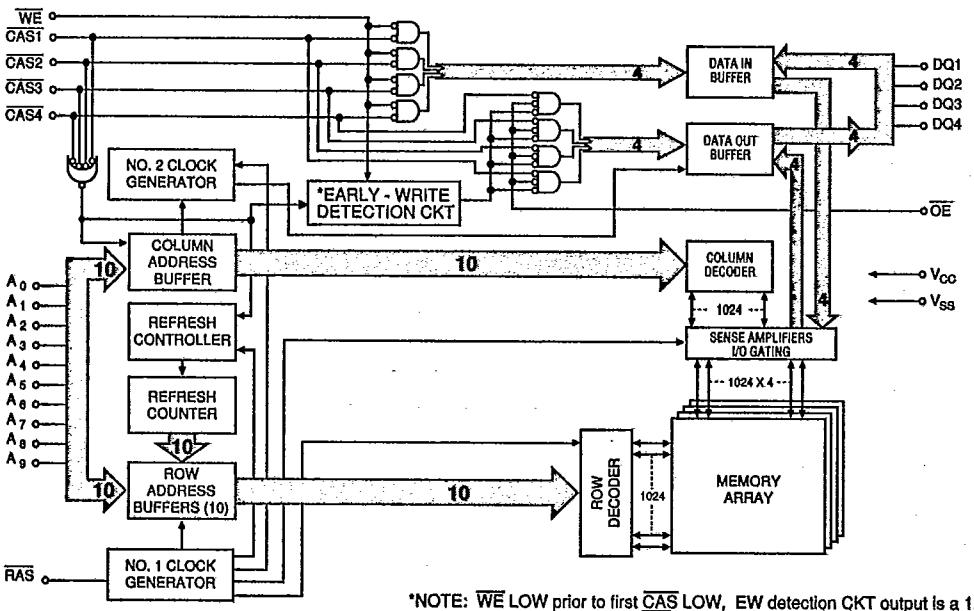
During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits, and the first $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data-in (Dx) is latched by the falling edge of $\overline{WE}$ or the first $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to the first $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output buffer, data out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding $\overline{CAS}$ occurs (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle ($\overline{OE}$ switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by the first $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and all four $\overline{CAS}$ controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic and sequential row addressing.

FUNCTIONAL BLOCK DIAGRAM
QUAD CAS



*NOTE: WE LOW prior to first CAS LOW, EW detection CKT output is a 1.
First CAS LOW while WE HIGH, EW detection CKT output is a 0,
(OE will now determine I/O).

TRUTH TABLE

Function		RAS	CASx	CASy	WE	OE	Addresses tR	Addresses tC	DQx (DQy always High-Z)
Standby		H	X	X	X	X	X	X	High-Z
READ		L	L	H	H	L	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	H	L	X	ROW	COL	Valid Data In
READ-WRITE		L	L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out
PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	H	L	X	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Valid Data In
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
	2nd Cycle	L	H→L	H	H→L	L→H	n/a	COL	Valid Data Out, Data In
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	H	L	X	ROW	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC3}	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC= ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC= ^tRC (MIN))	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC6}	100	90	80	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$1-4, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		115		ns	31
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15, 29
Output Enable	t_{OE}		20		20		25	ns	33
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	29
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	27
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	34
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	28
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16, 32
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	32
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	28
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	27
Column address hold time	t_{CAH}	15		15		20		ns	27
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	27
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 28
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

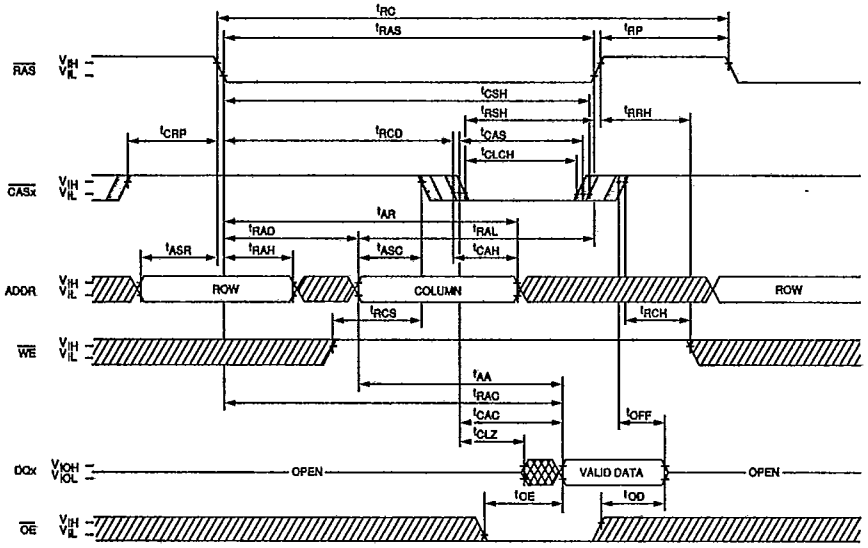
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20, 29, 38
Output disable	t_{OD}		20		20		20	ns	34, 38
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21, 27
Write command hold time	t_{WCH}	15		15		20		ns	36
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	55		60		75		ns	
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	28
Data-in setup time	t_{DS}	0		0		0		ns	22, 29
Data-in hold time	t_{DH}	15		15		20		ns	22, 29
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	t_{AWD}	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	50		55		60		ns	21, 27
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	t_{REF}		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	5, 27
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	5, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	t_{CLCH}	10		10		10		ns	30
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	t_{OEH}	20		20		20		ns	37
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN refresh cycle	t_{ORD}	0		0		0		ns	

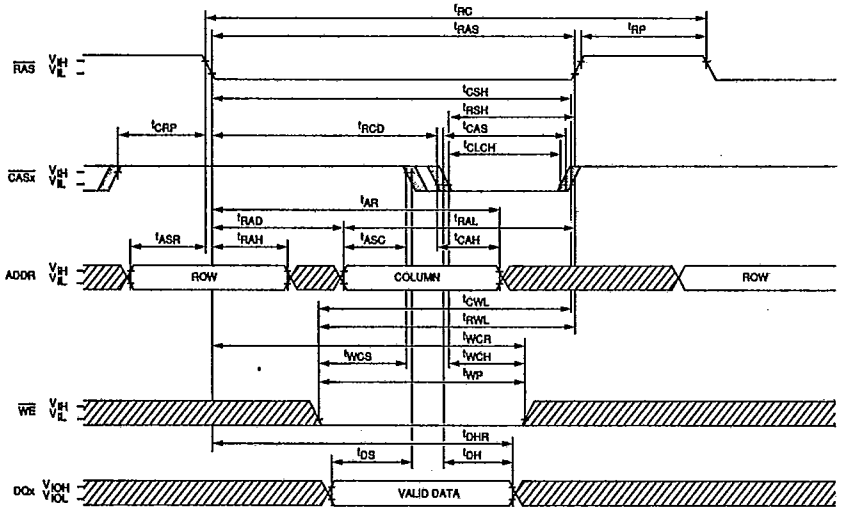
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and Vcc = 5V.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CASx}$ = V_{IH}, data output (Qx) is high impedance.
12. If $\overline{CASx}$ = V_{IL}, Qx may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If at least one $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four $\overline{CAS}$ controls must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in EARLY-WRITE and READ-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CASx}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. One to three $\overline{CAS}$ controls may be HIGH throughout any given $\overline{CAS}$ cycle, even though the timing waveforms show all $\overline{CAS}$ controls going LOW. If any one does go LOW, it must meet all the timing requirements listed or the data for that I/O buffer may be invalid. At least one of the four $\overline{CAS}$ controls must be LOW for a valid $\overline{CAS}$ cycle to occur.
26. All other inputs at Vcc -0.2V.
27. The first $\overline{CASx}$ edge to transition LOW.
28. The last $\overline{CASx}$ edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding $\overline{CASx}$ input; DQ1 by $\overline{CAS1}$, DQ2 by $\overline{CAS2}$, etc.
30. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
31. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
32. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
33. First DQx controlled by the first $\overline{CASx}$ to go LOW.
34. Last DQx controlled by the last $\overline{CASx}$ to go HIGH.
35. Each $\overline{CASx}$ must meet minimum pulse width.
36. Last $\overline{CASx}$ to go LOW.
37. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If the last $\overline{CASx}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
38. The DQs open during READ cycles once ^tOD or ^tOFF occur. If the last $\overline{CASx}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CASx}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CASx}$ remains LOW).

READ CYCLE



EARLY-WRITE CYCLE



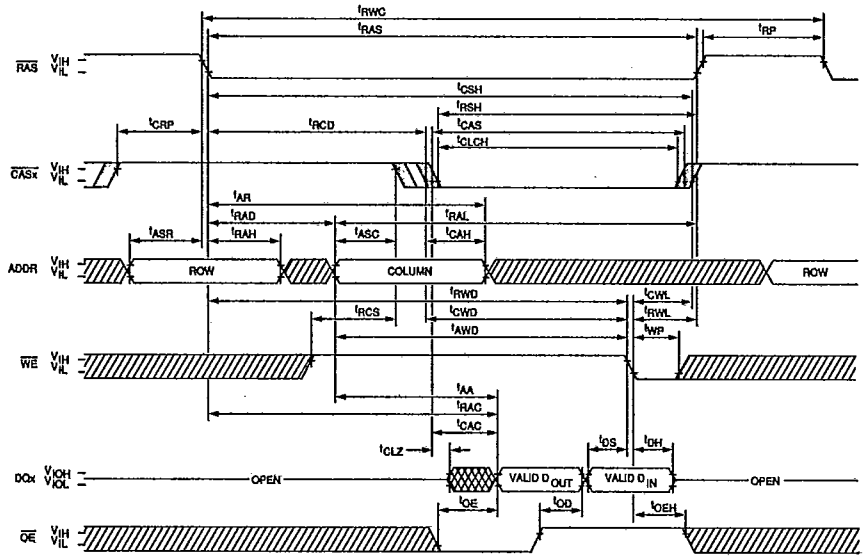
OE = DON'T CARE

DON'T CARE

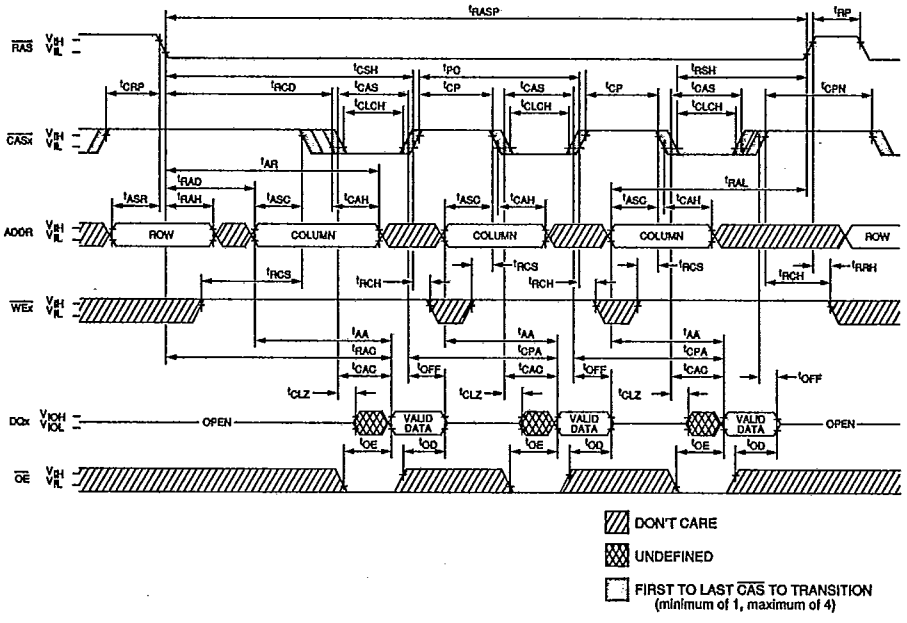
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

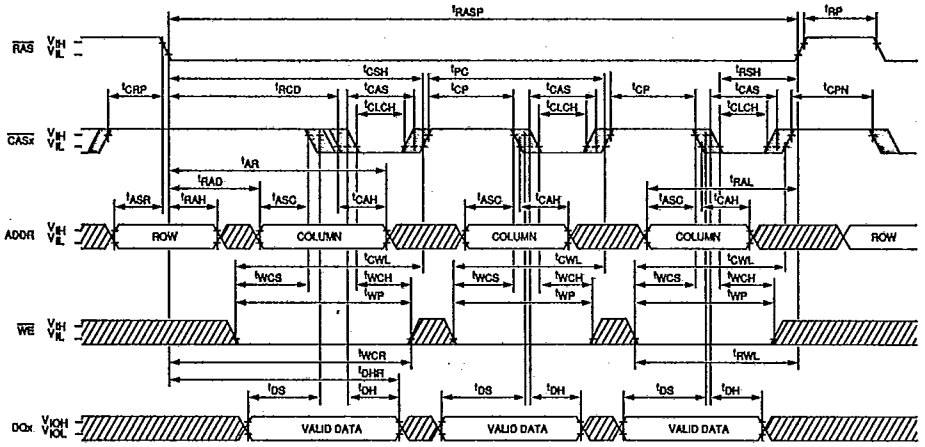
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



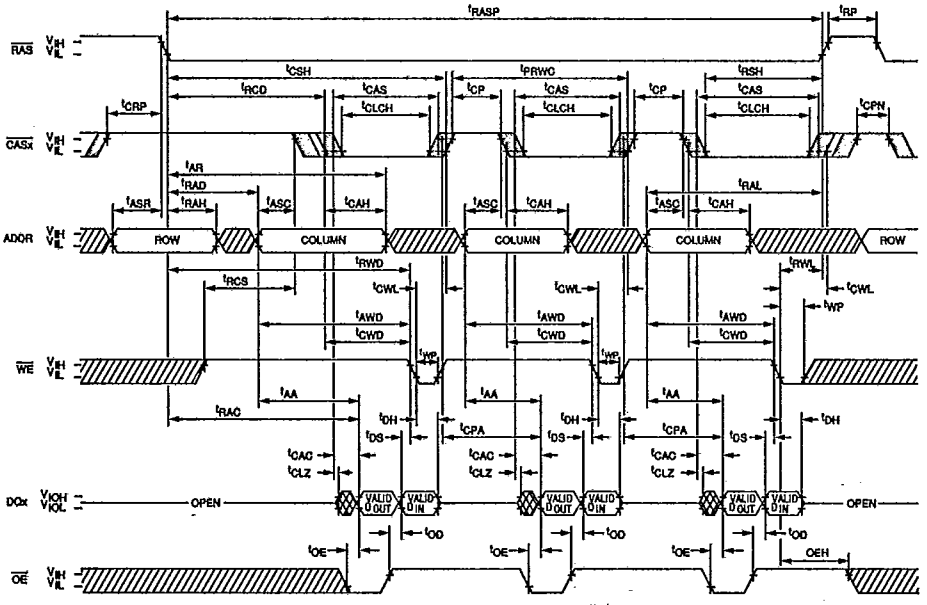
FAST-PAGE-MODE READ CYCLE



FAST PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



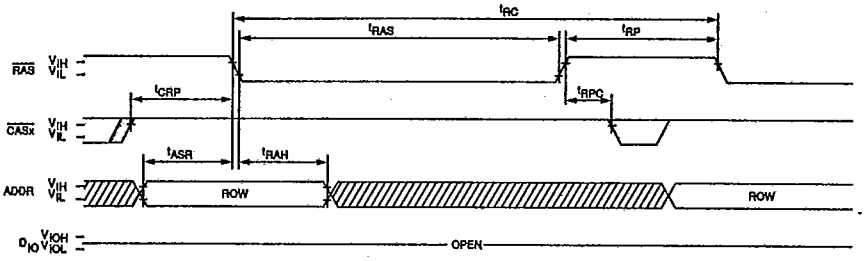
DON'T CARE

UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

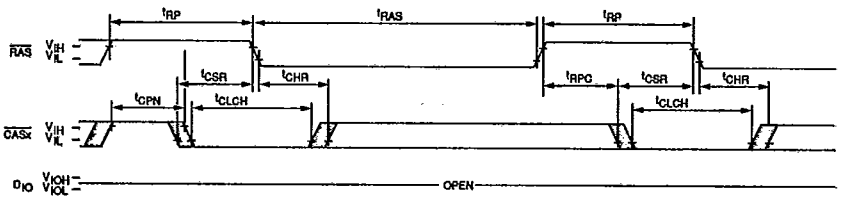
RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; WE and OE = DON'T CARE)



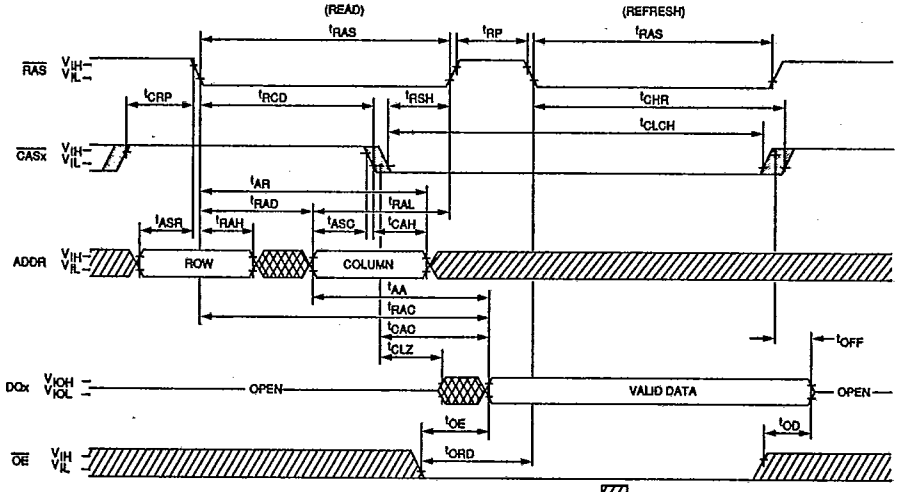
CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE

(WE = HIGH, OE = LOW) [24]

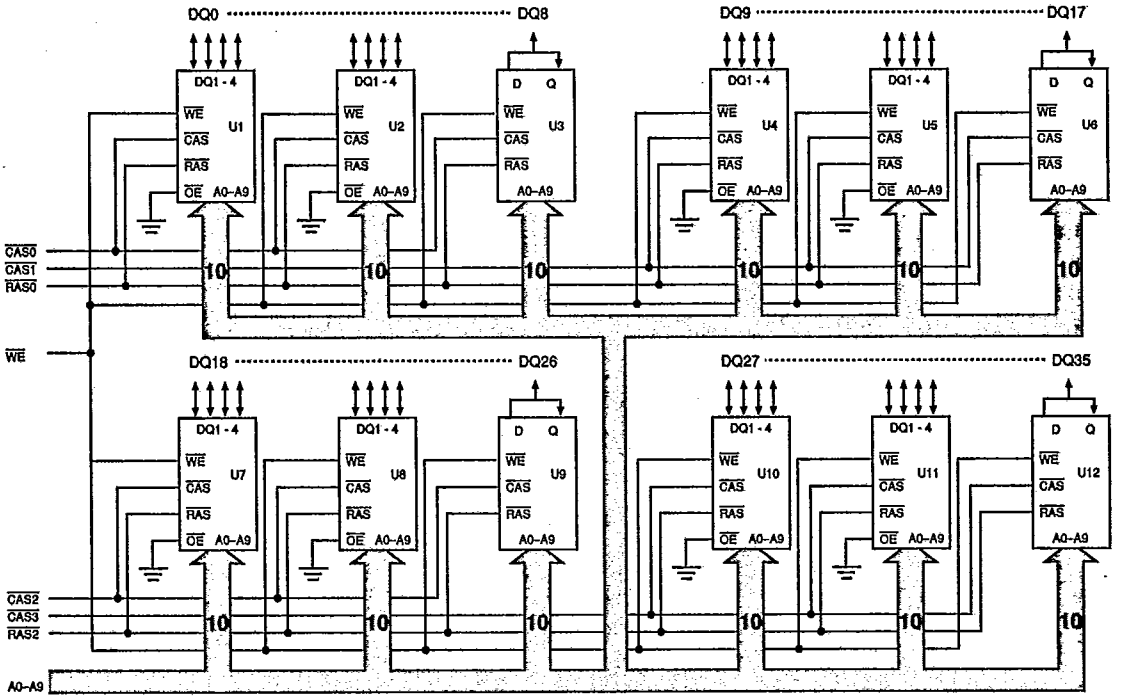


QUAD CAS MODULE UPGRADE

The MT4C4004 (Quad CAS DRAM) was developed to supersede the 1 Meg DRAMs used in the current 1 Meg and 2 Meg x 36 DRAM modules and to add leading-edge CMOS performance. The MT4C4004 is a 1 Meg x 4 CMOS FAST-PAGE-MODE DRAM with four $\overline{CAS}$ input controls. The four individual $\overline{CAS}$ inputs allow each I/O buffer (DQ) to be separately controlled, just as if there were four separate 1 Meg x 1 DRAMs. Most 1 Meg x 1 DRAMs use older CMOS technology and do not have the access speeds of the newer CMOS 4 Meg (1 Meg x 4).

The MT4C4004 will reduce chip count on a x36 module; improving reliability, reducing power consumption and lowering cost. The 1 Meg x 36 will have four 1 Meg x 1 DRAMs replaced by either one or two Quad CAS DRAMs, depending on whether $\overline{RAS0}$ and $\overline{RAS1}$ must be separate or can be connected together. The 2 Meg x 36 will have eight 1 Meg x 1 DRAMs replaced by either two or four Quad CAS DRAMs, depending on whether $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$ must be split or can be connected together.

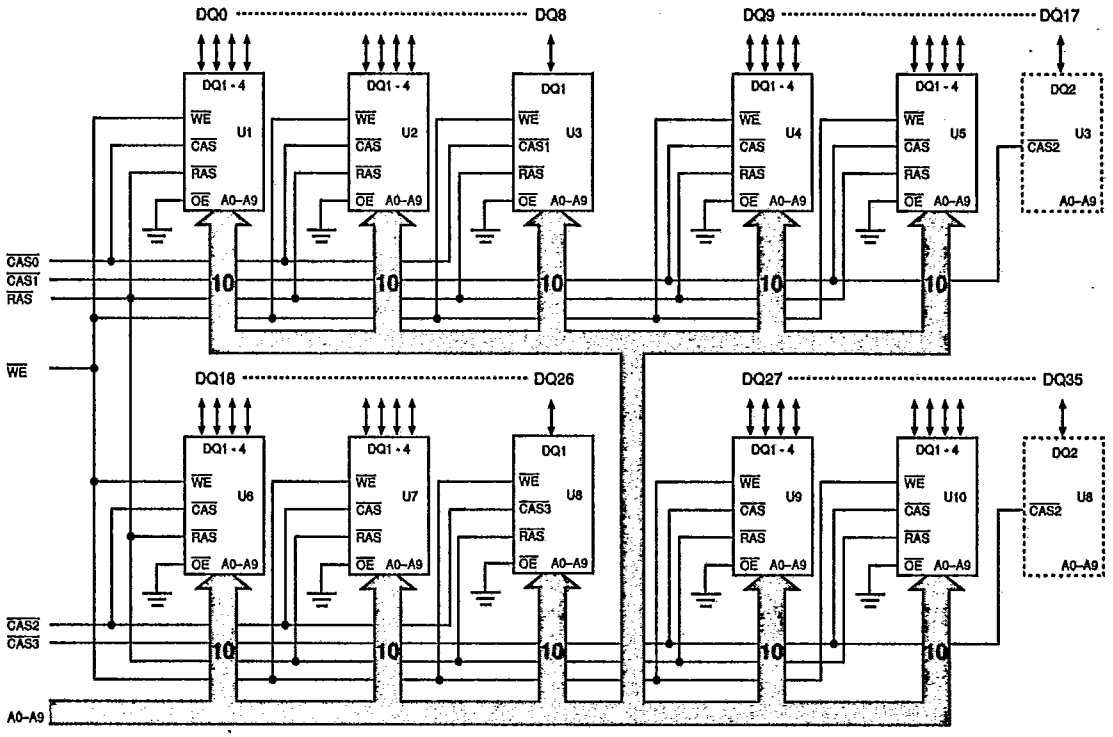
The current 1 Meg x 36 DRAM Module is shown with 256K x 1 DRAMs in Figure 1 below. Figures 2 and 3 show how the same module will be realized with the Quad CAS DRAM for both the split $\overline{RAS}$ (Figure 2) and the common $\overline{RAS}$ (Figure 3) modules.



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4256DJ
U3, U6, U9, U12 = MT1259EJ

Figure 1
1 MEG x 36 WITH 1 MEG x 1 FOR PARITY BIT

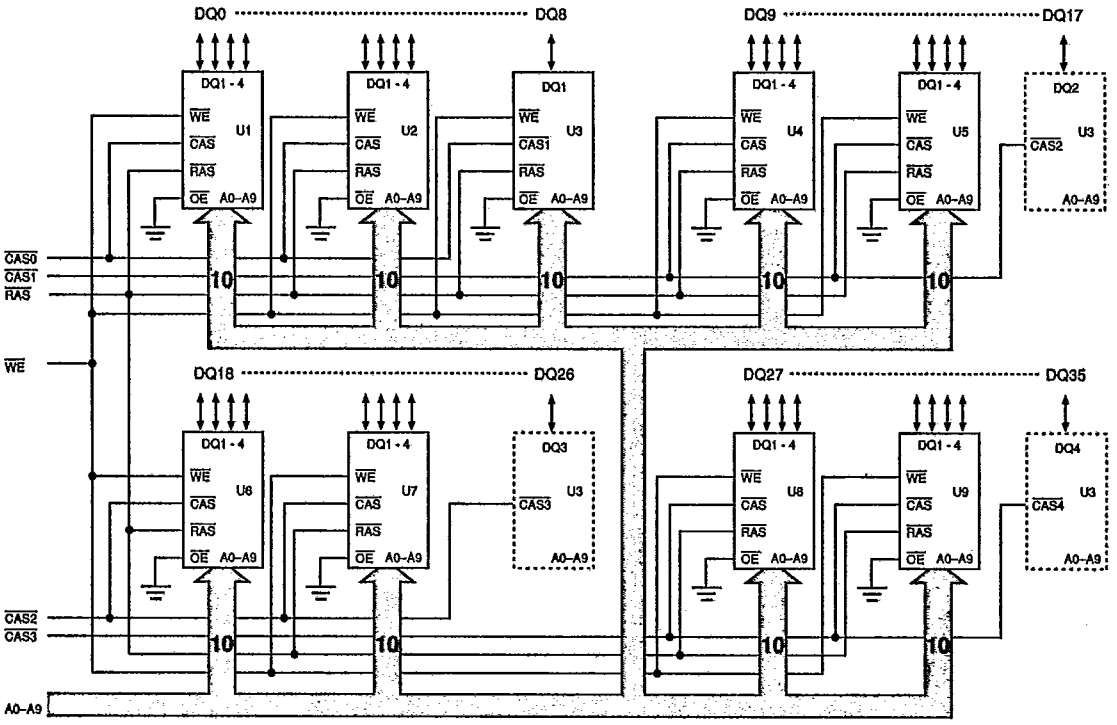
QUAD CAS ENHANCED x36 MODULES



U1, U2, U4, U5, U6, U7, U8, U9 = MT4C4256DJ
U3 = MT4C4259EJ

Figure 2
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND SPLIT $\overline{RAS}$ CONTROL

QUAD CAS ENHANCED x36 MODULES



U1, U2, U4-U9 = MT4C4256DJ
U3 = MT4C4259EJ

Figure 3
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND COMMON $\overline{RAS}$ CONTROL