CMOS **MT90737**

DS3/DS1 MUX/DEMUX (M13)

Preliminary Information

ISSUE 1 June 1995

Features

- Multiplexes/demultiplexes 28 DS1 signals to/from a DS3 signal
- Selectable M13 or C-bit parity mode
- Separate interface for C-bits
- FEBE, C or P-bit parity error insertion
- DS3 LOS, LOF, P-bit parity, C-bit parity, AIS and idle signal detection
- DS3 AIS and idle signal generation
- Access to DS3 and DS2 X-bits
- DS3 and DS1 loopbacks
- Detects DS2 LOF
- DS1 idle signal (QRS, AIS or ESF) generation
- DS1 LOS detection on transmit or receive path
- Multiplexed and non-multiplexed microprocessor bus interfaces

Applications

- Single-board M13 multiplexer
- Compact add/drop mux
- Fractional T3
- Digital Cross-connect Systems
- CSU/DSU

Ordering Information

MT90737AM 208 Pin PQFP

-40° to 85°C

Description

The MT90737 DS3/DS1 Multiplexer/Demultiplexer (M13) is designed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. The MT90737 complies with Bellcore's TR-TSY-000499, ANSI's T1.107-1988 and supplement T1.107a-1990.

The MT90737 provides a separate transmit (13 bits) and receive (14 bits) interface for C-bits while operating in the C-bit parity mode. The FEAC channel (C3) is accessed via MT90737 memory. The MT90737 uses 37 byte register locations for software control, performance counters, and alarm reporting. Both multiplexed and non-multiplexed bus types are supported by the microprocessor interface.

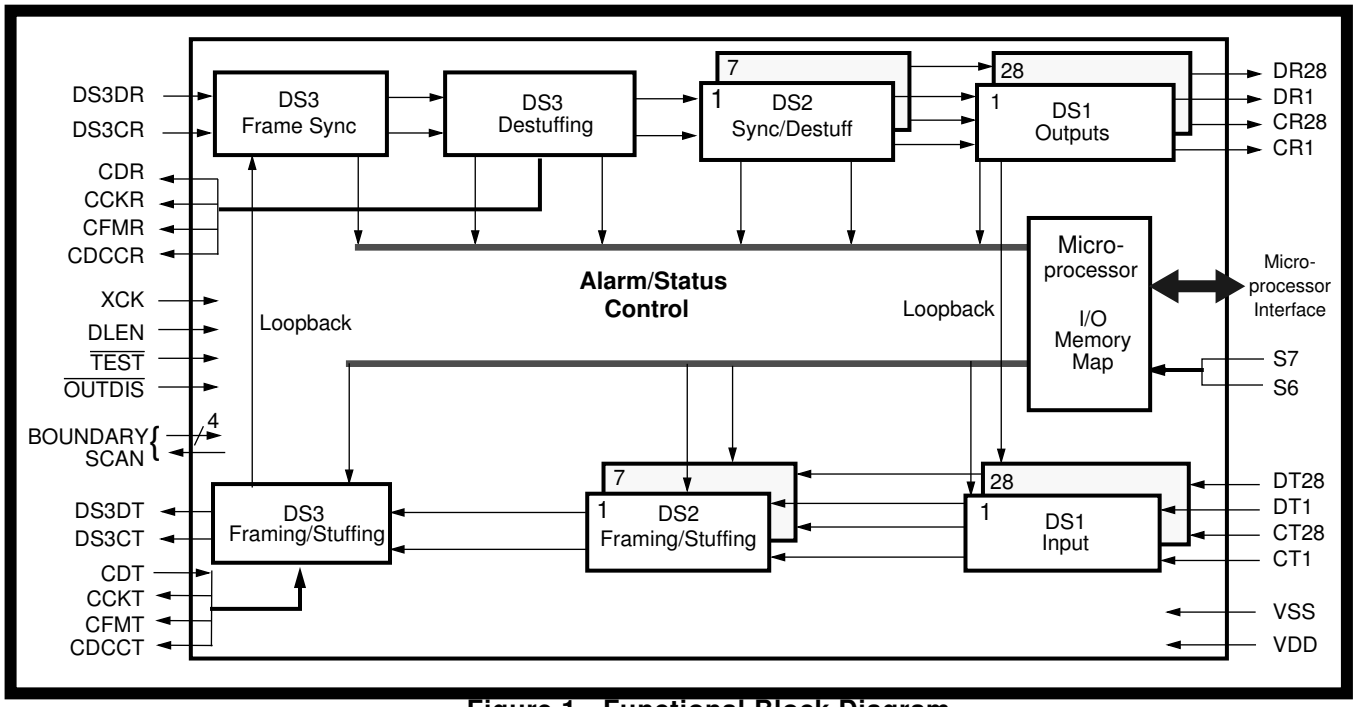


Figure 1 - Functional Block Diagram

U.S. Patent Number 5040170

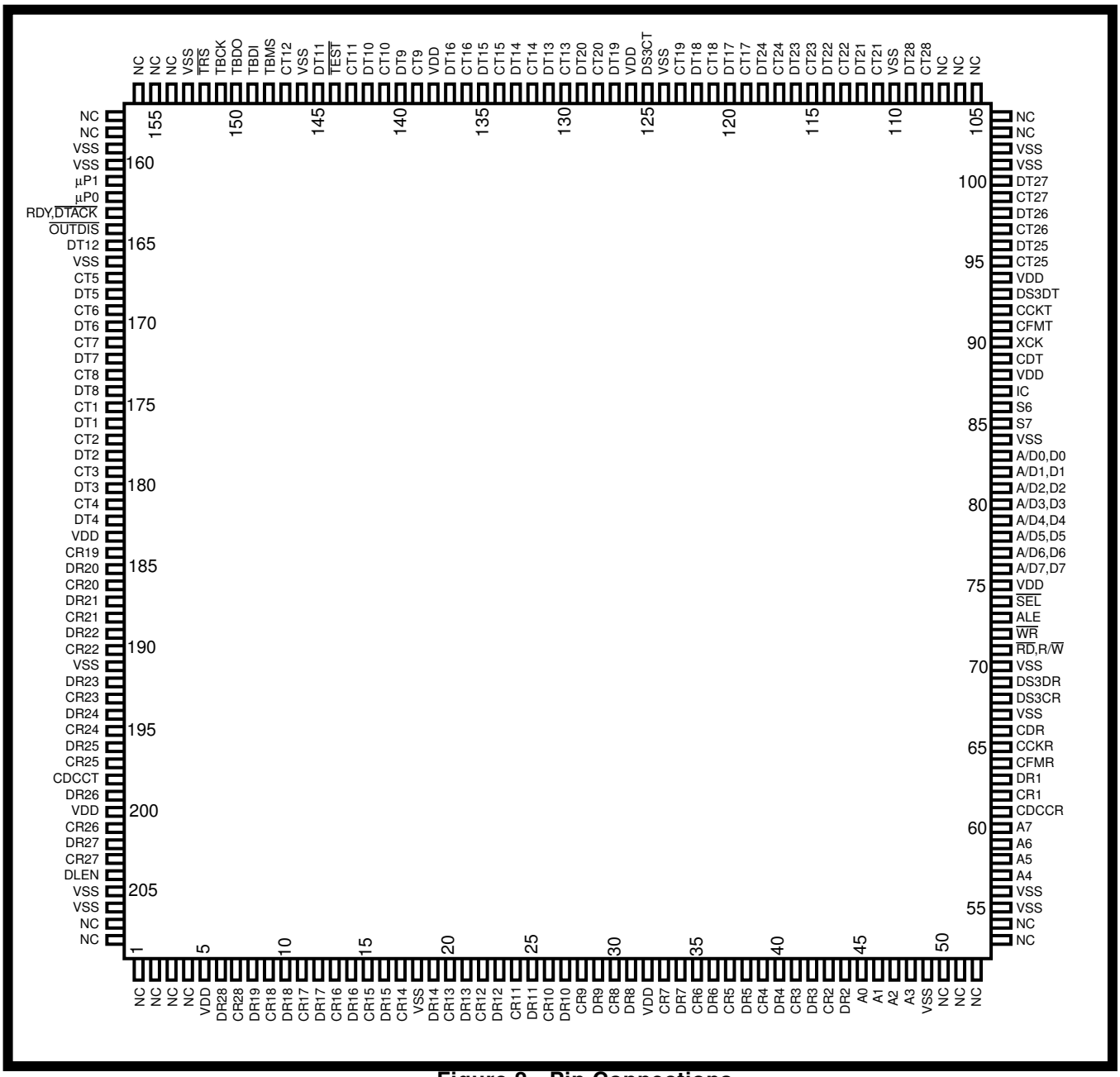


Figure 2 - Pin Connections

Pin Description

Power Supply, Ground and No Connect.

Pin #	Name	I/O/P	Description
5, 32, 75, 88, 94, 126, 138 183, 200	VDD	P	**Power Supply.** +5V±5%.
18, 49, 55, 56, 67, 70, 84,101,102, 110, 124, 146, 153, 159, 160, 166, 191, 205, 206	VSS	P	**Ground.**
1-4, 50-54, 103-107, 154-158, 207, 208	NC	--	**No Connection.** leave open.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

DS1 Receive Interfaces

Pin #	Name	I/O/P	Description
62	CR1	O	**Receive Clock Channels 1 - 28.** TTL Type III compatible. Receive data is clocked out of the MT90737 on positive transitions. The clock for the first DS1 channel corresponds to CR1, while the clock for the last DS1 channel corresponds to CR28. The DS1 clock signals are derived from the DS3 clock signal (DS3CR). During periods of DS3/DS2 out of frame or AIS, the MT90737 provides a DS1 clock signal for clocking out AIS which is derived from the XCK clock (pin 90).
43	CR2		
41	CR3		
39	CR4		
37	CR5		
35	CR6		
33	CR7		
30	CR8		
28	CR9		
26	CR10		
24	CR11		
22	CR12		
20	CR13		
17	CR14		
15	CR15		
13	CR16		
11	CR17		
9	CR18		
184	CR19		
186	CR20		
188	CR21		
190	CR22		
193	CR23		
195	CR24		
197	CR25		
201	CR26		
203	CR27		
7	CR28		

DS1 Receive Interfaces

Pin #	Name	I/O/P	Description
63	DR1	O	**Receive Data DS1 Channels 1 - 28.** TTL Type III compatible. Demultiplexed DS1 channels. The first DS1 channel corresponds to DR1, while the last DS1 channel corresponds to DR28.
44	DR2		
42	DR3		
40	DR4		
38	DR5		
36	DR6		
34	DR7		
31	DR8		
29	DR9		
27	DR10		
25	DR11		
23	DR12		
21	DR13		
19	DR14		
16	DR15		
14	DR16		
12	DR17		
10	DR18		
8	DR19		
185	DR20		
187	DR21		
189	DR22		
192	DR23		
194	DR24		
196	DR25		
199	DR26		
202	DR27		
6	DR28		

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

DS1 Transmit Interfaces

Pin #	Name	I/O/P	Description
175	CT1	I	**Transmit DS1 Clocks Channels 1 - 28.** TTL Type I compatible.Transmit data is clocked into the MT90737 on positive transitions. The clock for the first DS1 channel corresponds to CT1, while the clock for the last DS1 channel corresponds to CT28.
177	CT2		
179	CT3		
181	CT4		
167	CT5		
169	CT6		
171	CT7		
173	CT8		
139	CT9		
141	CT10		
143	CT11		
147	CT12		
130	CT13		
132	CT14		
134	CT15		
136	CT16		
	(continued next page)		

DS1 Transmit Interfaces

Pin #	Name	I/O/P	Description
119 121 123 128 111 113 115 117 95 97 99 108	CT17 CT18 CT19 CT20 CT21 CT22 CT23 CT24 CT25 CT26 CT27 CT28	I	**Transmit DS1 Clocks** (continued from previous page).
176 178 180 182 168 170 172 174 140 142 145 165 131 133 135 137 120 122 127 129 112 114 116 118 96 98 100 109	DT1 DT2 DT3 DT4 DT5 DT6 DT7 DT8 DT9 DT10 DT11 DT12 DT13 DT14 DT15 DT16 DT17 DT18 DT19 DT20 DT21 DT22 DT23 DT24 DT25 DT26 DT27 DT28	I	**Transmit Data DS1 Channels 1 - 28.** TTL Type I compatible.The first DS1 channel corresponds to DT1, while the last DS1 channel corresponds to DT28.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

DS3 Interface

Pin #	Name	I/O/P	Description
68	DS3CR	I	**DS3 Receive Clock.** CMOS compatible. A 44.736 MHz clock that is used to clock DS3 data into the MT90737. This clock is used as the time base for demultiplexing the DS3 data. When the loop timing feature is active (a one written into bit 3 (LPTIME) in 02H), or when the DS3 external transmit clock (XCK) fails, DS3CR becomes the transmit clock.
69	DS3DR	I	**DS3 Receive Data.** CMOS compatible. Receive 44.736 Mbit/s data is clocked into the MT90737 on positive transitions of the receive clock (DS3CR).
125	DS3CT	O	**DS3 Transmit Clock.** TTL Type IV compatible. A 44.736 MHz clock which is derived from the external transmit clock input signal (XCK). It is used to clock DS3 data from the MT90737.
93	DS3DT	O	**DS3 Transmit Data.** TTL Type IV compatible. Transmit C-bit parity or M13 formatted DS3 data is clocked out of the MT90737 on positive transitions of the transmit clock (DS3CT).

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Microprocessor Interface

Pin #	Name	I/O/P	Description
60-57 48-45	A(7-4) A(3-0)	I	**Address Bus (Intel/Motorola).** TTL Type II compatible. These are active high address inputs that are used by the microprocessor for accessing the MT90737 registers for a read/write operation. A7 is the most significant bit. These signals are ignored when the multiplexed interface is selected.
76-83	A/D (7-0) D(7-0)	I/O	**Address/Data Bus (Multiplexed), Data Bus (Intel/Motorola).** TTL Type IV compatible. For a multiplexed interface, these bi-directional leads constitute address/data buses for accessing the MT90737 registers. For either the Intel or Motorola interface, these bi-directional leads are used for transferring data. The most significant bit is A/D7 or D7.
74	$\overline{SEL}$	I	**Select.** TTL Type I compatible. A low enables data transfers between the microprocessor and the MT90737 registers during a read/write bus cycle.
71	$\overline{RD}$ R/$\overline{W}$	I	**Read (Intel/Multiplexed) or Read/Write (Motorola).** TTL Type I compatible. Intel/Multiplexed - An active low signal generated by the microprocessor for reading the MT90737 register locations. Motorola - An active high signal generated by the microprocessor for reading the MT90737 register locations. An active low signal is used to write to the MT90737 register locations.
73	ALE	I	**Address Latch Enable (Multiplexed).** TTL Type I compatible. An active high enable signal generated by the microprocessor. The falling transition is used to store an address during a read/write bus cycle.
72	$\overline{WR}$	I	**Write (Intel/Multiplexed).** TTL Type I compatible. An active low signal generated by the Intel/Multiplexed microprocessor for writing to the MT90737 register locations. Not used for the Motorola microprocessor interface.
163	RDY $\overline{DTACK}$	O	**Ready (Intel) or Data Transfer Acknowledge (Motorola Mode).** TTL Type IV compatible. Intel - The MT90737 is always Ready. Connection to an Intel Microprocessor is optional. If connected, a pull-up resistor is required. Motorola - During a read cycle, a low signal indicates the information on the data bus is valid. During a write cycle, a low signal acknowledges the acceptance of data. A pull-up resistor is required for this pin.

Microprocessor Interface

Pin #	Name	I/O/P	Description
162 161	µP0 µP1	I	**Microprocessor Interface Type Select.** TTL Type II compatible. The type of microprocessor interface selected is given in the table below: µP1 / µP0 / Interface: 0 / 0 / Intel Compatible; 0 / 1 / Motorola Compatible; 1 / 0 / Multiplexed; 1 / 1 / Not Used The multiplexed interface consists of eight bi-directional address/data leads, select, address latch enable, read, and write. The Intel compatible interface (80X86 family) consists of eight address leads, eight bi-directional data leads, select, read, write, and ready. The Motorola compatible interface (680X0 family) consists of eight address leads, eight bi-directional data leads, select, read/write, and data transfer acknowledge.
85, 86	S(7-6)	I	**Address Straps.** TTL Type II compatible. When the Intel, Motorola, or Multiplexed microprocessor interfaces are selected by µP0 and µP1, the two address straps, S7 and S6, allow the MT90737 to be partitioned as a segment of memory. The straps define the address offset of the device. The address register is partitioned as shown below. The data register pointed to by the 6 LSBs is only accessed if the 2 MSBs match the address straps. Bit 7 6 — MT90737 Address — Register Address
87	IC	-	**Internal Connection.** Keep open.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Receive C-Bit Interface

Pin #	Name	I/O/P	Description
65	CCKR	O	**Receive C-Bit Clock.** TTL Type IV compatible. A gapped clock signal provided for clocking out the selected receive C-bit data. Data (CDR) is clocked out on positive transitions.
66	CDR	O	**Receive C-Bit Data.** TTL Type IV compatible. The following C-bits are provided at this interface. C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21.
64	CFMR	O	**Receive C-Bit Framing Pulse.** TTL Type IV compatible. This positive framing pulse occurs prior to the C2 bit.
61	CDCCR	O	**Receive Data Link Indication.** TTL Type IV compatible. A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The receive C-bit clock (CCKR) may be AND'ed with this signal to provide a gapped data link clock for loading the three C-bits from the C-bit data (CDR) into external circuitry. CDCCR is enabled by placing a high on DLEN pin.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Transmit C-Bit Interface

Pin #	Name	I/O/P	Description
92	CCKT	O	**Transmit C-Bit Clock.** TTL Type IV compatible. A gapped clock signal provided for clocking in selected transmit C-bit data (CDT). Data is clocked into the MT90737 on positive transitions.
89	CDT	I	**Transmit C-Bit Data.** TTL Type I compatible. The transmit gapped clock (CCKT) provided for clocking in the following C-bits: C2, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. An unused C-bit should be transmitted as a one.
91	CFMT	O	**Transmit C-Bit Framing Pulse.** TTL Type IV compatible. This positive framing pulse occurs prior to the C2 bit.
198	CDCCT	O	**Transmit Data Link Indication.** TTL Type IV compatible. A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The transmit C-bit clock (CCKT) may be AND'ed with this signal to provide a gapped data link clock signal. CDCCT is enabled by placing a high on DLEN pin.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Control Bits

Pin #	Name	I/O/P	Description
164	$\overline{\text{OUTDIS}}$	I	**Outputs Disable.** TTL Type II compatible. A low causes all MT90737 outputs and bi-directional signal leads to be set to a high impedance state for test purposes except the CDCCR and CDCCT pins. The CDCCR and CDCCT outputs are controlled by DLEN pin. $\overline{\text{OUTDIS}}$ is provided with an internal pull-up resistor.
204	DLEN	I	**Data Link Enable.** TTL Type II compatible. Normally left open. A high enables the transmit and receive data link indication signals, CDCCT and CDCCR. The data link indication signals identify the location of the three data link C-bits (C13, C14, and C15). A low puts CDCCR and CDCCT into high impedance state.
144	$\overline{\text{TEST}}$	O	**Test Pin.** Leave open.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

External Clock

Pin #	Name	I/O/P	Description
90	XCK	I	**External Transmit Clock.** CMOS compatible. An external clock having a frequency of 44.736 MHz ±20 ppm is required to meet DSX-3 cross-connect requirements. The clock duty cycle should be 50 ±5%. The transmit clock is also used to operate the microprocessor interface. The MT90737 monitors this clock for transitions. When a clock failure is detected, the MT90737 automatically switches to the receive clock (DS3CR) for multiplexer and microprocessor operation. Receive loop timing (a one written to bit 3, LPTIME, in 02H) also causes the receive clock to become the transmit clock.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Boundary Scan Pins

Pin #	Name	I/O/P	Description
148	TBMS	I	**Test Boundary Mode Select.** TTL Type II compatible. The signal present on this lead is clocked in by the positive transitions of TBCK to control test operations.
149	TBDI	I	**Test Boundary Data Input.** TTL Type II compatible. Serial data input clocked in by positive transitions of TBCK as boundary scan test messages.
150	TBDO	O	**Test Boundary Data Output.** TTL Type IV compatible. Serial data output whose information is clocked out on negative transitions of TBCK. A pull-up resistor is required for this tri-stating pin.
151	TBCK	I	**Test Boundary Scan Clock.** TTL Type II compatible.The input clock for boundary scan testing.
152	$\overline{\text{TRS}}$	I	**Test Boundary Scan Reset.** TTL Type II compatible. When a low signal is applied to this pin, the MT90737 Test Access Port (TAP) controller resets and the boundary scan is disabled. The TAP is also reset upon power-up or by holding the TBMS signal lead high for at least five rising clock transitions of TBCK. When the boundary scan feature is not used, $\overline{\text{TRS}}$ must be held low.

Note: I = Input; O = Output; P = Power. See DC Characteristics section for CMOS and TTL Type definitions.

Functional Description

The MT90737 (M13) multiplexes and demultiplexes 28 DS1 signals to and from a DS3 signal in either M13 or C-bit parity mode. In the C-bit parity mode, the MT90737 provides a separate transmit (13 bits) and receives (14 bits) interface for C-bits. The Far End Alarm and Control (FEAC) channel (C3) is accessed via internal memory. The MT90737 has 37 byte registers for software control, performance counters, and alarm reporting. The microprocessor interface is selectable via two external hardware straps. Interface options are Multiplexed and Non-Multiplexed bus types (such as Intel 80X86 and Motorola 680X0 families).

The MT90737 supports Bellcore's TR-TSY-000499, ANSI's T1.107-1988 and supplement T1.107a-1990. Figure 1 shows a functional block diagram of the MT90737.

Multiplex (Transmit)

In the transmit direction, DS1 transmit data (DTn) is clocked into the MT90737 on positive transitions of the clock input (CTn) for each of the 28 DS1 channels. A DS1 Input Block, which consists of a FIFO and supporting logic, is provided for each DS1 channel. Under software control, the MT90737 can invert the transmit data signals, or the clock signals for all 28 DS1 channels. The data inversion feature provides compatibility with certain T1 line interface devices, while the clock inversion feature allows back-to-back M13 operation.

The DS1 Input Block is also used to insert one of three available idle patterns from a common generator into a DS1 bit stream, under software control. The selection of the idle pattern is common to all 28 DS1 channels. The idle patterns are: a Quasi-Random Sequence (QRS), an Extended Super Frame DS1 (ESF) format with all ones in channels one through 24, and an AIS format (unframed all ones).

Each DS1 signal is bit-multiplexed into the respective DS2 frame, with the stuff bits inserted based on the fill level of an internal FIFO. When the level of the FIFO drops below half full, a stuff bit is inserted into the DS1 bit stream in the DS2 signal. The DS2 signal is formed by combining four DS1 signals. In each DS2 frame there are 287 data bit positions per DS1 channel, one stuff bit per DS1 channel and 24 overhead bits for a total of 1176 bits. The overhead bits are used for framing, X-bit channel and stuff control.

The DS3 signal is partitioned into M-frames of 4760 bits each. The M-frames are divided into seven M-subframes having 680 bits each. Each M-subframe is further divided into eight blocks of 85 bits each. Each block uses 84 bits for payload and one bit for frame overhead. There are 56 overhead bits in each M-frame. the M-frame alignment uses three bits, the M-subframe alignment (F-bits) uses 28 bits, 21 bits are defined as C-bits, two bits are assigned for parity, and two bits are assigned for the X-bit channel.

The DS3 frame is constructed and timed according to the operating mode, i.e., C-bit parity mode or M13 mode.

C-Bit Parity Mode

In the C-bit parity mode, all seven of the DS2 stuff bits are fixed as stuff, resulting in 7 pseudo DS2 frames of 671 bits per DS2 frame in each DS3 frame, for a DS2 rate of 6.3062723 Mbit/s. Since stuffing always occurs, the 21 C-bits are assigned for other functions, as shown in Figure 2. A C-bit interface is provided for transmitting 13 C-bits (C2, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, C21). The external transmit C-bit interface consists of a serial data input (CDT), an output clock (CCKT), a data link indicator pulse (CDCCT), and an output framing pulse (CFMT). The data link indicator pulse identifies the location of the three data link bits, C13, C14, and C15. In addition, a control bit (C3CLKI) is provided in the memory map (register 19H) which enables the MT90737 to generate an extra clock cycle in CCKT during the C3 bit time.

Of the eight remaining C-bits, C1 is used as an identification channel; C3 is defined as a Far End Alarm and Control (FEAC) bit; C7, C8, and C9 (CP-bits) are used for C-bit parity; and the remaining three bits, C10, C11, and C12, are used to transmit a Far End Block Error (FEBE) indication. C1 should be set to 1 under C-bit parity mode. The FEAC channel carries alarm or status information from the far-end terminal to the near-end terminal, and is also used to initiate DS3 and DS1 loopbacks at the far-end terminal from the near-end terminal. The CP-bits are used to carry DS3-path parity information for end-to-end parity checking. Since the CP-bits pass through the network unchanged (except in the case of an AIS or CP-bit errors), the DS3 receiver can determine if an error has occurred in an M-frame by computing the contents of the given M-frame and comparing this parity value with the parity received in the CP-bits in the following M-frame. If a received C-bit parity error or framing error is detected, the FEBE bits shall be returned to the transmitting terminal to indicate the error occurrence. Thus, the overall performance of the full-duplex DS3 path, under C-bit parity mode, can be determined at either end or at any place along the path with the FEAC and FEBE signals.

C1	C2*	C3**	C1 = C-bit parity mode C2 = Reserved C3 = Far End Alarm & Control (FEAC)
C4*	C5*	C6*	Not defined, set to one
C7	C8	C9	C-Parity bits (CP-bits)
C10	C11	C12	Far End Block Error (FEBE)
C13*	C14*	C15*	Maintenance data link (28 Kbit/s)
C16*	C17*	C18*	Not defined, set to one
C19*	C20*	C21*	Not defined, set to one

*These bits are provided at the C-bit interface in the C-bit mode
** Always provided at the receive C-bit interface in the C-bit mode

Figure 2 - C-Bit Assignments In C-bit Parity Format

M13 Mode

In the M13 mode, fixed DS2 to DS3 stuffing is used for M23 multiplexing at a rate of seven stuffs per every 18 DS3 stuff opportunities. This yields a DS2 frequency of +2.6 ppm above the desired frequency of 6.312 Mbit/s. Adding this to the tolerance of the DS3 clock signal, ±20 ppm, the frequency is still within the ±32 ppm allowed for a DS2 signal.

Other functions, which are common to the C-bit parity and M13 mode, provided by the MT90737 are as follows. Under software control, the MT90737 can generate DS3 idle and AIS signals, and loop back the transmitted DS3 signal to the receiver for test purposes. The MT90737 also provides DS1 loopback capability, and transmit clock failure protection.

Demultiplex (Receive)

In the receive direction, DS3 data (DS3DR) is clocked into the MT90737 on positive transitions of the DS3 input clock (DS3CR). The DS3 Frame Sync Block searches for and locks to the DS3 frame. The receive DS3 signal is monitored for out of frame, loss of signal, DS3 AIS, DS3 idle signal, P-bit parity, the state of the X-bits, and loss of clock. The DS3 AIS detection mechanism is software selectable, with a choice of six different patterns. These range from full compliance to T1.107/107a to unframed all ones AIS detection. Control bits are also provided in memory which allows all, some of, or none of the DS3 alarms to cause the insertion of AIS into the receive DS1 channels.

In the C-bit parity mode, the C-bits are allocated for network performance. The MT90737 performs Far End Alarm and Control (FEAC) detection, C-bit parity error detection, and Far End Block Error (FEBE) detection. FEAC loopback requests and alarm/status information is provided in the memory map. A receive C-bit interface is provided for extraction of 14 C-bits (C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21). The receive C-bit interface consists of a serial data output (CDR), an output clock signal (CCKR), a framing pulse (CFMR), and a data link indicator pulse (CDCCR). The data link indicator pulse identifies the location of the data link C-bits, C13, C14, and C15.

In the M13 mode, destuffing from DS3 to DS2 is performed based on the states of the C-bits in the DS3 subframes. If two or three of the C-bits in a subframe are ones, the associated stuff bit is interpreted as being a stuff bit and is removed from the data stream and discarded.

The MT90737 synchronizes and extracts the 28 DS1 channels from the seven DS2 channels. Each of the DS2 channels is monitored for out of frame. The MT90737 may generate AIS in each of the DS1 signal tributaries corresponding to the DS2 channel(s) that lost frame, depending on the DS1 AIS alarm insertion control bits. DS2 to DS1 destuffing is based on the states of the three C-bits in each DS2 subframe. If two or three of the C-bits in one of the DS2 subframes are ones, the stuff bit for that subframe is discarded. In the M13 mode, the DS2 C-bits or stuffing bits are also used for DS1 remote loopback requests. The MT90737 provides control bits in the memory map for selecting the remote loopback detection mechanism. The destuffing operation is still active during loopback request and operation. In addition to DS2 synchronization, destuffing, and remote loopback detection, the MT90737 also extracts the X-bits from seven DS2 frames.

An option is provided that allows the received or transmitted DS1 channels to be monitored for loss of signal. Receive data for each of the DS1 channels (DRn) is clocked out of the MT90737 on positive transitions of the associated clock signal (CRn). In addition, the

MT90737 provides a stable DS1 clock signal for the data signals received during AIS periods.

Register Bit Map

The MT90737 memory map consists of control bits, alarms (non-latched and latched), and counters accessed by a microprocessor read/write cycle. The unused bit positions (shown below shaded) in a register must be masked by software to avoid reading incorrect data.

Address (Hex)	Mode*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	R	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	XR2	XR1
01	R/W			T3AIS	T3IDL	FEBE	PBITE	CBITE	XT
02	R/W	IDLB	IDLA	TEST1	3LBK	LPTIME	INVCK	1INV	MODE
03	R	CBIT1	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
04	R	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
05	R	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
06	R	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
07	R/W	EXEC	CON/DIS	LBSEL	D22	D21	D20	D11	D10
08	R	LBALL	LB25	LB21	LB17	LB13	LB9	LB5	LB1
09	R	LBDS3	LB26	LB22	LB18	LB14	LB10	LB6	LB2
0A	R		LB27	LB23	LB19	LB15	LB11	LB7	LB3
0B	R		LB28	LB24	LB20	LB16	LB12	LB8	LB4
0C	R		LOS25	LOS21	LOS17	LOS13	LOS9	LOS5	LOS1
0D	R		LOS26	LOS22	LOS18	LOS14	LOS10	LOS6	LOS2
0E	R		LOS27	LOS23	LOS19	LOS15	LOS11	LOS7	LOS3
0F	R		LOS28	LOS24	LOS20	LOS16	LOS12	LOS8	LOS4
10	R/W		IDL25	IDL21	IDL17	IDL13	IDL9	IDL5	IDL1
11	R/W		IDL26	IDL22	IDL18	IDL14	IDL10	IDL6	IDL2
12	R/W		IDL27	IDL23	IDL19	IDL15	IDL11	IDL7	IDL3
13	R/W		IDL28	IDL24	IDL20	IDL16	IDL12	IDL8	IDL4
14	R		R2X7	R2X6	R2X5	R2X4	R2X3	R2X2	R2X1
15	R/W		T2X7	T2X6	T2X5	T2X4	T2X3	T2X2	T2X1
16	R(L)	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	$\overline{XR2}$	$\overline{XR1}$
17	R(L)	CERROR	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
18		TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
19	R/W	C3CLKI	TEST	TEST	TEST	TEST	TEST	TEST	TEST
1A		TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
1B	R	FME7	FME6	FME5	FME4	FME3	FME2	FME1	FME0
1C	R/W	EXEC	CONT/10	TFEAC6	TFEAC5	TFEAC4	TFEAC3	TFEAC2	TFEAC1
1D	R	FIDL	NEW	RFEAC6	RFEAC5	RFEAC4	RFEAC3	RFEAC2	RFEAC1
1E	R/W	EXEC	CON/DIS		LLB22	LLB21	LLB20	LLB11	LLB10
1F**	R/W	Initialization Register							
20	R/W	1TRIST	1LOSSEL	1TAIS1	1TAIS0	1LBV3	1LBV2	1LBV1	1LBV0
21	R/W				R3AIS2	R3AIS1	R3AIS0	T3AIS1	T3AIS0
22	R	C1BZ7	C1BZ6	C1BZ5	C1BZ4	C1BZ3	C1BZ2	C1BZ1	C1BZ0
23	R	ME7	ME6	ME5	ME4	ME3	ME2	ME1	ME0
24	R(L)	AISX=1	AISC=0	TEST	TEST	TEST	TEST		SEF

*Read/write (R/W); Read only (R); Read only - latched register R(L).
**To initialize the MT90737, writing F0H followed by 00H to this location resets the entire device.

Register Bit Map Definitions

Addr	Bit	Symbol	Description
00	7	R3LOS	**Receive DS3 Loss of Signal.** A receive LOS alarm occurs (R3LOS is set to 1) when the incoming DS3 data (DS3DR) is stuck low for more than 1022 clock cycles (DS3CR). Recovery occurs (R3LOS is reset to 0) when two or more ones are detected in the incoming data bit stream. This bit position is unlatched.
	6	R3OOF	**Receive DS3 Out of Frame.** A receive OOF alarm occurs (R3OOF is set to 1) when three out of 16 F-bits are in error in a sliding window of 16 bits, or one or more M-bits are in error in two consecutive frames. Recovery occurs (R3OOF is reset to 0) when the F-bits pattern of 1001 and the M-bits of 010 are detected for two consecutive frames. Recovery takes approximately 0.95 milliseconds, worst case. This bit position is unlatched. An OOF also inhibits the performance counters (04H, 05H, 06H, 1BH, 22H, and 23H).
	5	R3AIS	**Receive AIS Alarm Indication Signal.** The MT90737 can detect one of six possible DS3 AIS's including the ANSI's standard AIS pattern. An 1 in R3AIS indicates a receive AIS has been detected. The pattern of AIS is selected by the states written to the three R3AISn bits in register 21H. R3AIS bit position is unlatched. When the MT90737 is configured to detect one of the framed AIS signals, the R3OOF (bit 6 of this register) should be examined to ensure that the MT90737 is detecting DS3 frame.
	4	R3IDL	**Receive DS3 Idle Pattern Signal.** A DS3 idle pattern signal has the valid M-bit, F-bit, and P-bit channels. The information bits are a 1100 sequence that starts with 11 after each M-bit, F-bit, X-bit, P-bit, and C-bit channels. The C-bits (C7, C8, and C9) in M-subframe 3 are set to zero. A valid received DS3 idle signal is detected when the MT90737 detects zeros for C7, C8, and C9 in subframe 3 and the 1100 sequence. The 1100 pattern sequence is searched on a per DS3 frame basis. The MT90737 can tolerate up to and including 5 errored 4 bit groups of the 1100 pattern per DS3 frame and still recognize the 1100 pattern as valid. If the MT90737 detects 6 or more errored 4 bit groups of the 1100 pattern per DS3 frame the MT90737 will exit the R3IDL state. This bit position is unlatched. A DS3 idle signal as defined in ANSI T1.107a-1990 is being received by the MT90737 device if this bit (R3IDL), bit 1 (XR2) and bit 0 (XR1) of this register are all set to 1.
	3	R3CKF	**Receive DS3 Clock Failure.** A receive DS3 clock failure alarm occurs (R3CKF is set to 1) when the receive clock (DS3CR) is stuck high or low for 30-100 DS3 clock periods. The demultiplexer does not function when the receive clock is lost. Recovery occurs on the first clock transition. This bit position is unlatched.
	2	T3CKF	**Transmit DS3 Clock Failure.** A transmit DS3 clock failure alarm occurs (T3CKF is set to 1) when the transmit input clock (XCK) is stuck high or low for 30-100 DS3 clock periods. A failure causes the receive clock to become the transmit clock. This permits the MT90737 microprocessor interface and multiplexer to function. Recovery occurs when the first clock transition is detected.
	1	XR2	**Receive DS3 X-bit Number 2.** This bit position indicates the receive state of X2. This bit position is updated each frame.
	0	XR1	**Receive DS3 X-bit Number 1.** This bit position indicates the receive state of X1. This bit position is updated each frame.

Addr	Bit	Symbol	Description
01	7,6	-	**Not Used.**
	5	T3AIS	**Transmit DS3 Alarm Indication Signal.** A one causes the MT90737 to transmit a DS3 AIS. The type of AIS sent is determined by the states written into bit 1 (T3AIS1) and bit 0 (T3AIS0) in register 21H. To terminate DS3 AIS transmission T3AIS needs to be reset to zero.
	4	T3IDL	**Transmit DS3 Idle Signal.** To transmit a DS3 idle signal, a one must be written to T3IDL (bit 4) and XT (bit 0) of this register (01H), in addition, bit 0 (T3AIS0) and bit 1 (T3AIS1) of register 21H must be set to zero.
	3	FEBE	**Transmit Far End Block Error.** A one causes the MT90737 to transmit a single FEBE error indication (C10, C11, and C12 equal to 0) in the next DS3 frame. To send an additional FEBE indication, the microprocessor must first write a zero before writing another one to this bit.
	2	PBITE	**Transmit P-Bit Parity Error.** A one causes the MT90737 to transmit a single P-bit parity error in the next DS3 frame. The P-bit error is transmitted by inverting the value of the two calculated bits. To send an additional error, the microprocessor must first write a zero before writing another one to this bit.
	1	CBITE	**Transmit C-Bit Parity Error.** A one causes the MT90737 to transmit a single C-bit parity error in the next available DS3 frame when the MT90737 is operating in the C-bit parity mode. The C-bit error is introduced by inverting the calculated C-bit parity bits in subframe 3 (C7, C8, and C9). To send an additional error, the microprocessor must first write a zero before writing another one to this bit.
	0	XT	**Transmit X-Bits.** The X-bits may be used to transmit a yellow alarm or may be used as a low speed signaling channel. A one or zero causes the MT90737 to transmit a one or zero for both X1 and X2. Not: Set to 1 when transmitting DS3 idle signal (see T3IDL in this register 01H).

<table>
<tr><th>Addr</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="8">02</td><td>7
6</td><td>IDLB
IDLA</td><td>DS1 Idle Code Selection. Three types of DS1 idle codes are provided according to the table given below. A selected idle code is common to all DS1 channels selected. One or more transmitted DS1 channels can be selected by writing a one in IDLn register locations 10, 11, 12, or 13 Hex, provided register 1E Hex has not selected these DS1 channels for loopback.
<table>
<tr><th>IDLB</th><th>IDLA</th><th>DS1 Idle Code Selected</th></tr>
<tr><td>0</td><td>0</td><td>Quasi-Random Signal (2^{20} - 1 QRS) including zero suppression.</td></tr>
<tr><td>1</td><td>0</td><td>Framed Extended Super Frame (ESF) signal format which consists of a Framing Pattern Sequence of 001011 pattern, CRC-6 pattern, and ones in the 64kbit/s channels 1 through 24.</td></tr>
<tr><td>X</td><td>1</td><td>Unframed all ones signal (AIS).</td></tr>
</table></td></tr>
<tr><td>5</td><td>TEST1</td><td>Reserved for Testing Purposes. A zero must be written into this bit position for normal operation.</td></tr>
<tr><td>4</td><td>3LBK</td><td>DS3 Line Loopback. A one disables the DS3 receive input and causes the DS3 transmit output to be looped back as receive data. Transmit data is provided at the output (DS3DT). A zero allows MT90737 to be in normal operation.</td></tr>
<tr><td>3</td><td>LPTIME</td><td>Receive Loop Timing. A one disables the transmit clock input (XCK), and causes the DS3 receive clock to become the DS3 transmit clock. If the DS3 receive clock fails in this mode, the MT90737 switches over to the transmit clock, and the demultiplexer becomes inoperative, however, the multiplexer and microprocessor interface continue to function.</td></tr>
<tr><td>2</td><td>INVCK</td><td>Invert DS1 Transmit Clocks. A one causes all transmit DS1 clock inputs (CTn) to be inverted. This is provided for back-to-back M13 operation.</td></tr>
<tr><td>1</td><td>1INV</td><td>Invert DS1 Transmit Data. A one causes the transmit data inputs for all DS1 channels (DTn) to be inverted.</td></tr>
<tr><td>0</td><td>MODE</td><td>Operating Mode. A one enables the MT90737 to operate in the M13 mode as specified in Bellcore TR-TSY-000009, and the ANSI T1.107-1988 standard. A zero enables the MT90737 to operate in the C-bit parity mode as specified in the ANSI T1.107a-1990, supplement to ANSI T1.107-1988.</td></tr>
<tr><td rowspan="2">03</td><td>7</td><td>CBIT1</td><td>C-bit Number 1. This bit is updated each frame with the state of the received C1. The C1 bit is used to identify the DS3 application according to the table given below.
<table>
<tr><th>C1 Value</th><th>Application</th></tr>
<tr><td>Random</td><td>M13 format</td></tr>
<tr><td>All 1s</td><td>C-bit parity format</td></tr>
</table>
In addition, the number of C1 bits equal to zero is counted by the C1 Bit Zero Counter (C1BZn) in 22 Hex.</td></tr>
<tr><td>6-0</td><td>DS2OOFn
(n=7-1)</td><td>DS2 Out of Frame Alarm Indication. A one in bits 6-0 corresponds to an out of frame alarm for the respective DS2 channel (7-1). A DS2 OOF occurs when two out of four consecutive DS2 framing bits are in error. A DS2 OOF for a DS2 channel causes AIS to be inserted into its four DS1 channels. Recovery is based on searching for the correct DS2 framing pattern (0101...). Once the framing pattern is found, one more frame is used to acquire alignment. Recovery takes approximately 6.8 milliseconds, worst case average.</td></tr>
</table>

Addr	Bit	Symbol	Description
04	7-0	FBn (n=7-0)	**FEBE Performance Counter/DS3 F&M Bit Error Counter.** This performance counter counts the number of FEBEs received since the last read cycle in the C-bit parity mode. A FEBE indication occurs when C10, C11, or C12 is received equal to zero in a DS3 frame. The counter is protected from overflow by stopping at the maximum count of 255 until read. The counter is protected during the period of a microprocessor read cycle and when the MT90737 updates the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the counter update. The counter is inhibited during DS3 loss of signal or out of frame times, and is cleared on a microprocessor read cycle. In the M13 mode, this saturating counter counts the number of DS3 F&M bits that have been received in error since the last read cycle.
05	7-0	CPn (n=7-0)	**C-Bit Parity Performance/Number of Frames Counter.** In the C-bit parity mode, this counter counts the number of C-bit parity errors received since the last read cycle. The counter is protected from overflow by stopping at the maximum count of 255 until read. The counter is protected during the period of a microprocessor read cycle and when the MT90737 updates the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the counter update. The counter is inhibited during DS3 loss of signal or out of frame times, and is cleared on a microprocessor read cycle. In the M13 mode, this saturating counter counts the number of DS3 frames since the last read cycle.
06	7-0	PPn (n=7-0)	**P-Bit Parity Performance Counter.** This counter counts the number of P-bit parity errors received since the last read cycle. This performance count is valid in either operating mode. The counter is protected from overflow by stopping at the maximum count of 255 until read. The counter is protected during the period of a microprocessor read cycle and when the MT90737 updates the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterward, the counter increments. Only the indication of one error count is held during the microprocessor read and the counter update. The counter is inhibited during DS3 loss of signal or out of frame times, and is cleared on a microprocessor read cycle.

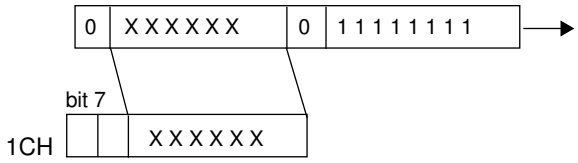
Addr	Bit	Symbol	Description
07	7 6 5 4 3 2 1 0	EXEC CON/DIS LBSEL D22 D21 D20 D11 D10	**Remote Loopback.** The bits in this register are used to send a DS1 remote loopback request in the M13 mode, or a DS3/DS1 remote loopback request in the C-bit parity mode. Bit 7 (EXEC) executes the command. In the M13 mode, a one in this bit ascertains the remote loopback request and a zero removes a remote loopback request. In the C-bit parity mode, a one written to this bit sends a remote loopback connect or disconnect command and once the command is transmitted, bit 7 (EXEC) is automatically reset to zero (see below Remote Loopback in C-bit parity mode). Bit 6 (CON/DIS) sends the command to connect or disconnect the loopback selected. This bit is not used in the M13 mode and effective only in the C-bit parity mode. Bit 5 (LBSEL) selects either the M13 mode (LBSEL=0) or C-bit parity mode (LBSEL=1). The C or stuff bit inversion mechanism selected by the four 1LBV bits in location 20H, is used for remote loopback in the M13 mode. In the C-Parity mode, the MT90737 automatically translates date written in this register to the FEAC (C3) code word which is used to send DS1 and DS3 remote loopback requests. Bits 4-0 select the DS1 channel to be looped back. Bits 4 (D22), 3 (D21), and 2 (D20) select the DS2 frame (1-7). Bits 1 (D11) and 0 (D10) select one of four DS1 channels. Remote Loopback in C-bit parity mode: In the C-bit parity mode, the MT90737 translates the channel to be looped back as written in bits 4-0 into the FEAC code word. To send a loopback request, the MT90737 sends ten repetitions of the FEAC line activator code sequence (0 000111 0 11111111) followed immediately by ten repetitions of the loopback code word (0 xxxxxx 0 11111111). At the end of this sequence (20 code words or 320 DS3 frames), completion is indicated by bit 7 (EXEC) resetting to zero. To deactivate a loopback in the C-bit parity mode, the MT90737 sends ten repetitions of the deactivate code followed immediately by ten repetitions of the channel selected. Only one loopback request can be sent at a time. The codes for sending and deactivating an M13, or a C-bit parity remote loopback request are shown below:

Bits	7	6	5	4	3	2	1	0
Channel	EXEC	CON/DIS	LBSEL	D22	D21	D20	D11	D10
All	1	X	X	0	0	0	0	0
Channel 1	1	X	X	0	0	1	0	0
Channel 2	1	X	X	0	0	1	0	1
- - - - - - - - - -	- - - - - - -	- - - - - - - -	- - - - - -	- - - - -	- - - - -	- - - - -	- - - - - -	- - - - - -
Channel 28	1	X	X	1	1	1	1	1
DS3	1	X	1	0	0	0	1	0

Addr	Bit	Symbol	Description
08	7 6 5 4 3 2 1 0	LBALL LB25 LB21 LB17 LB13 LB9 LB5 LB1	**Receive Loopback Requests.** Bit 7, LBALL (all DS1 channels), and bits 6-0 (LBn) indicate the loopback request detected. For the M13 mode, a loopback request is received when any of the conditions (C-bit or stuff bit inversions) are detected five or more times in succession. The remote loopback type is determined by the states written to the 1LBVn bits in register location 20H. A remote loopback request is cancelled when the normal state of the bit (C or stuff bit) is received five or more times in succession. In the C-bit parity mode, a remote loopback request is received by detecting the FEAC connect word five times in succession, followed by five consecutive receptions of the DS1 channel number word. A remote loopback request is cleared upon the reception of five consecutive disconnect words followed by five consecutive reception of the DS1 channel number word. Note: It is possible to have multiple loopback set. Once a loopback request is received or taken down in registers 08H-0BH, a microprocessor must write the appropriate code to register 1EH to correspondingly set up or take down the loopback in the appropriate DS1 channel. The loopback requests in registers 08H-0BH are valid only when the MT90737 has DS3 frame and the corresponding DS2 channels are in frame, and when the MT90737 is not receiving a R3AIS or R3IDL alarm (e.g., if the MT90737 has DS3 frame and only DS2 channel 2 is in frame, then only the loopback requests for DS1 channels 5-8 are valid).
09	7 6 5 4 3 2 1 0	LBDS3 LB26 LB22 LB18 LB14 LB10 LB6 LB2	**Receive Loopback Requests.** Bits 7 (LBDS3) and 6-0 (LBn) indicate loopback requests sent by the distant end for either a DS3 signal or for the DS1 channels indicated. For complete explanation, see 08H.
0A	7	-	**Not Used.**
	6 5 4 3 2 1 0	LB27 LB23 LB19 LB15 LB11 LB7 LB3	**Receive Loopback Requests.** Bits 6-0 (LBn) indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.
0B	7	-	**Not Used.**
	6 5 4 3 2 1 0	LB28 LB24 LB20 LB16 LB12 LB8 LB4	**Receive Loopback Requests.** Bits 6-0 (LBn) indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.

Addr	Bit	Symbol	Description
0C	7	-	**Not Used.**
	6 5 4 3 2 1 0	LOS25 LOS21 LOS17 LOS13 LOS9 LOS5 LOS1	**Loss of Signal, DS1 Channel n.** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state of bit 6 in 20H.
0D	7	-	**Not Used.**
	6 5 4 3 2 1 0	LOS26 LOS22 LOS18 LOS14 LOS10 LOS6 LOS2	**Loss of Signal, DS1 Channel n.** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state of bit 6 in 20H.
0E	7	-	**Not Used.**
	6 5 4 3 2 1 0	LOS27 LOS23 LOS19 LOS15 LOS11 LOS7 LOS3	**Loss of Signal, DS1 Channel n.** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state of bit 6 in 20H.
0F	7	-	**Not Used.**
	6 5 4 3 2 1 0	LOS28 LOS24 LOS20 LOS16 LOS12 LOS8 LOS4	**Loss of Signal, DS1 Channel n.** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state of bit 6 in 20H.
10	7	-	**Not Used.**
	6 5 4 3 2 1 0	IDL25 IDL21 IDL17 IDL13 IDL9 IDL5 IDL1	**Internal DS1 Idle Channel/Loopback.** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a local DS1 loopback. When register 1EH is written with 00H, and a DS1 channel in this register location is written with a one, the MT90737 generates and transmits a DS1 idle pattern determined by the idle code selection bits (IDLB and IDLA in location 02H) for that channel. When a DS1 channel is selected by register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead.
11	7	-	**Not Used.**
	6 5 4 3 2 1 0	IDL26 IDL22 IDL18 IDL14 IDL10 IDL6 IDL2	**Internal DS1 Idle Channel/Loopback.** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a DS1 loopback. When register 1EH is written with 00H, and a DS1 channel in this register location is written with a one, the MT90737 generates and transmits a DS1 idle pattern determined by the idle code selection bits (IDLB and IDLA in location 02H) for that channel. When a DS1 channel is selected by register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead.

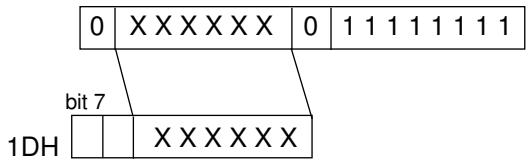
Addr	Bit	Symbol	Description
12	7	-	**Not Used.**
	6 5 4 3 2 1 0	IDL27 IDL23 IDL19 IDL15 IDL11 IDL7 IDL3	**Internal DS1 Idle Channel/Loopback.** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a DS1 loopback. When register 1EH is written with 00H, and a DS1 channel in this register location is written with a one, the MT90737 generates and transmits a DS1 idle pattern determined by the idle code selection bits (IDLB and IDLA in location 02H) for that channel. When a DS1 channel is selected by register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead.
13	7	-	**Not Used.**
	6 5 4 3 2 1 0	IDL28 IDL24 IDL20 IDL16 IDL12 IDL8 IDL4	**Internal DS1 Idle Channel/Loopback.** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a DS1 loopback. When register 1EH is written with 00H, and a DS1 channel in this register location is written with a one, the MT90737 generates and transmits a DS1 idle pattern determined by the idle code selection bits (IDLB and IDLA in location 02H) for that channel. When a DS1 channel is selected by register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead.
14	7	-	**Not Used.**
	6-0	R2Xn (n=7-1)	**Receive DS2 X-Bits.** The bits in this location indicate the state of the seven received DS2 channel X-bits.
15	7	-	**Not Used.**
	6-0	T2Xn (n=7-1)	**Transmit DS2 X-bits.** The bits written in this register are used to transmit the state of the seven DS2 channel X-bits. An X-bit OFF state is normally a one.
16	7 6 5 4 3 2 1 0	R3LOS R3OOF R3AIS R3IDL T3CKF R3CKF $\overline{XR2}$ $\overline{XR1}$	**Latched Receive Alarm/Status.** The bits in this register location are the same alarm/status bits listed in register location 00H, except that the corresponding bit latches on with an alarm. The $\overline{XR2}$ and $\overline{XR1}$ are the inverse of the two X-bits received, and latch when the received X bits are equal to zero. A microprocessor read cycle clears an alarm condition. If an alarm state or status condition remains true (a one) even after microprocessor Read, the corresponding bit relatches.
17	7 6-0	CERROR DS2OOFn (n=7-1)	**Latched C-bit Status/DS2 Out Of Frame Bits.** The bits in this register location are the same bits listed in register location 03H, except that the corresponding bit latches on with an alarm. For example, CERROR latches to a one on the first time C1 is 0. A microprocessor read cycle clears a set bit. If a DS2 OOF remains true (a one) even after microprocessor Read, the corresponding bit relatches.
18	7-0	TEST	**Test Register.** Used for testing.
19	7	C3CLKI	**C-Bit Parity C3 Clock Inhibit.** A zero enables the MT90737 to generate an extra clock pulse in the CCKT clock signal for clocking the C3 bit out to external logic. A one disables the generation of the C3 clock pulse.
	6-0	TEST	**Test Bits.** Used for testing.
1A	7-0	TEST	**Test Register.** Used for testing.
1B	7-0	FMEn (n=7-0)	**DS3 F-bits and M-bits in Error Counter.** An 8-bit saturating counter that counts the number of DS3 F-bits and DS3 M-bits that are in error since the last read cycle. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared on a microprocessor read cycle.

Addr	Bit	Symbol	Description
1C	7 6 5-0	EXEC CONT/10 TFEACn (n=6-1)	**Transmit FEAC Word.** Bit 7 (EXEC) initiates the FEAC transmission (EXEC=1) and also indicates when the transmission is completed (EXEC=0). Bit 6 (CONT/10) controls the duration of the FEAC transmission (1 = continuous, 0 = 10 times). Bits 5-0 (TFEACn) constitute the variable (XXXXXX) field in the FEAC word. A FEAC word is written in the field in the same order of transmission as shown below: **16-Bit FEAC Word**  FEAC Word/Microprocessor Write Relationship The MT90737 formats and generates the other ones and zeros that comprise the FEAC word. A minimum length (send FEAC word 10 times) message is sent using the following sequence: - Write 1 0 X X X X X X (X's=6-bit FEAC word) - MT90737 sends 16-bit FEAC word 10 times - MT90737 indicates completion by resetting bit 7 (0 0 X X X X X X) A continuous FEAC word is sent using the following sequence: - Write 1 1 X X X X X X (X's=6-bit FEAC word) - MT90737 sends 16-bit FEAC word continuously - Write 1 0 X X X X X X (X's=6-bit FEAC word) - MT90737 indicates completion by resetting bit 7 (0 0 X X X X X X)

<table>
<tr><th>Addr</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1D</td><td>7
6
5-0</td><td>FIDL
NEW
RFEACn
(n=6-1)</td><td>
Receive Single FEAC Word.
Bit 7 (FIDL) is the FEAC idle channel indication. It clears whenever a zero C3 bit is received framing the six-bit variable word. Bit 7 cannot be reset by a microprocessor read cycle.

Bit 6 (NEW) indicates when a new FEAC word has been detected. It clears when the register is read.

Bits 5-0 (RFEACn) constitute the variable (XXXXXX) field in the FEAC word. A FEAC word is read in the field in the same order of being received as shown below:

16-Bit FEAC Word


The following table lists possible FEAC combinations.
<table>
<tr><th>FIDL</th><th>NEW</th><th>Status</th></tr>
<tr><td>1</td><td>0</td><td>FEAC channel idle - No message received since last read cycle</td></tr>
<tr><td>0</td><td>1</td><td>New message received - FEAC channel busy</td></tr>
<tr><td>1</td><td>1</td><td>New message received - FEAC channel idle</td></tr>
</table>
Note: There is no buffering for the received FEAC message. The latest, validated FEAC message is provided and bit 6 (NEW) is set to one even if the previous message is not read.
</td></tr>
<tr><td>1E</td><td>7
6
4
3
2
1
0</td><td>EXEC
CON/DIS
LLB22
LLB21
LLB20
LLB11
LLB10</td><td>
DS1 Local Loopback.
Bit 7 (EXEC) initiates the loopback. This bit is reset upon completion of the command.

Bit 6 (CON/DIS) connects (CON/DIS= 1) or disconnects (CON/DIS=0) the specified loopback.

Bits 4 through 2 (LLB2n) selects one of seven DS2s.

Bits 1 and 0 (LLB1n) selects the DS1 within the DS2 signal.

The following table lists the commands for generating local loopback.
<table>
<tr><th>Bits
Channel</th><th>7
EXEC</th><th>6
CON/DIS</th><th>5
---</th><th>4
D22</th><th>3
D21</th><th>2
D20</th><th>1
D11</th><th>0
D10</th></tr>
<tr><td>All</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Clear All</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Clear All Confirmed</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Channel 1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Channel 2</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>----------</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Channel 28</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Clear Channel 28</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Clear Channel 28 Confirmed</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Addr</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1F</td><td>7-0</td><td>Initialization Register</td><td>Initialization Register. This register location is used to reset and initialize the MT90737. After power becomes stable, a F0 Hex followed by a 00 Hex must be written into this location to reset the internal counters.</td></tr>
<tr><td>20</td><td>7</td><td>1TRIST</td><td>Tri-State DS1 Receive Channels. A one causes all 28 receive DS1 data (DRn) and clock (CRn) output leads to a high impedance state. A zero is for normal operation.</td></tr>
<tr><td></td><td>6</td><td>1LOSSEL</td><td>DS1 Loss of Signal Selection. A zero selects the receive DS1 channels for loss of signal detection. A one selects the transmit DS1 channels for loss of signal detection. The DS1 loss of signals (LOSn) are reported in register locations 0C through 0FH.</td></tr>
<tr><td></td><td>5
4</td><td>1TAIS1
1TAIS0</td><td>DS1 AIS Insertion Selection. The two bits control the insertion of AIS (unframed all ones) into the 28 DS1 channels on certain DS3 alarm conditions, that are defined in register location 00H. The following table lists the settings for having various alarm conditions for causing AIS:
<table>
<tr><th>1TAIS1</th><th>1TAIS0</th><th>Received DS3 Alarm Conditions</th></tr>
<tr><td>0</td><td>0</td><td>R3OOF, R3AIS, R3LOS, R3CKF</td></tr>
<tr><td>0</td><td>1</td><td>R3OOF, R3AIS, R3CKF</td></tr>
<tr><td>1</td><td>0</td><td>R3LOS</td></tr>
<tr><td>1</td><td>1</td><td>No AIS insertions</td></tr>
</table>
The XCK clock (pin 90) is used as the time base for generating the DS1 AIS clocks.</td></tr>
<tr><td></td><td>3
2
1
0</td><td>1LBV3
1LBV2
1LBV1
1LBV0</td><td>M13 Remote Loopback Options. The following table indicates the various ways the MT90737 can transmit and receive a DS1 remote loopback request in the M13 operating mode by inverting C-bits or the stuff bit. The specified condition is transmitted for the duration of the loopback:
<table>
<tr><th>1LBV3</th><th>1LBV2</th><th>1LBV1</th><th>1LBV0</th><th>Loopback Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Third C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Second C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>First C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Undefined - Do not use</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Third C-bit & stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Second C-bit & stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>First C-bit & stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Stuff bit inverted</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Stuff bit = 0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Stuff bit = 1</td></tr>
<tr><td>1</td><td>X</td><td>1</td><td>X</td><td>Undefined - Do not use</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td>Undefined - Do not use</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Addr</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>21</td><td>7,6,5</td><td>-</td><td>Not used.</td></tr>
<tr><td></td><td>4
3
2</td><td>R3AIS2
R3AIS1
R3AIS0</td><td>Receive DS3 AIS Selection. A DS3 AIS may be detected in one of six ways. The following table selects the DS3 AIS detection mechanism for providing a R3AIS alarm:
<table>
<tr><th>R3AIS2</th><th>R3AIS1</th><th>R3AIS0</th><th>Receive DS3 AIS Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Framed 1010 pattern
C-bits = 0
X-bits disregarded</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Framed 1010 pattern
C-bits = 0
X-bits = 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Framed 1010 pattern
C-bits disregarded
X-bits disregarded</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Framed 1111 pattern
C-bits disregarded
X-bits disregarded</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Unframed 1010 pattern</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Unframed all ones pattern</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>Undefined - Do not use</td></tr>
</table>
The C-Bits = 0 & X bits = 1 conditions are detected as explained for bits 6 & 7 of Address 24H.
R3AIS2-0 set to 000_2, 001_2, & 010_2 respectively:
The framed 1010 pattern detection consists of looking for the 1010 pattern on a per DS3 subframe basis and monitoring for errors in four bit groups of the 1010 pattern. The 1010 pattern is accepted as valid if the MT90737 receives 4 or less errored four bit groups of the 1010 pattern per DS3 subframe and the 1010 pattern starts with a 1 after each DS3 overhead bit.
R3AIS2-0 set to 011_2:
The framed 1111 pattern detection consists of looking for the 1111 pattern on a per DS3 subframe basis and monitoring for errors in four bit groups of the 1111 pattern. The 1111 pattern is accepted as valid if the MT90737 receives 4 or less errored four bit groups of the 1111 pattern per DS3 subframe.
R3AIS2-0 set to 100_2:
For the unframed 1010 pattern detection the MT90737 looks for 1010 pattern and declares R3AIS if it receives 2 or less errored four bit groups of the 1010 pattern per DS3 subframe. The M90737 will exit the R3AIS state if it receives 5 or more errored four bit groups of the 1010 pattern per DS3 subframe. If 3 or 4 four bit groups of the 1010 pattern are errored per DS3 subframe the M90737 will exit and reenter the R3AIS state.
R3AIS2-0 set to 101_2:
The unframed 1111 pattern detection consists of looking for the 1111 pattern and monitoring for errors in 4 bit groups of the 1111 pattern. The 1111 pattern is accepted as valid if the MT90737 receives four or less errored four bit groups of the 1111 pattern out of a total of 168 four bit groups.</td></tr>
</table>

<table>
<tr><th>Addr</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>21</td><td>1
0</td><td>T3AIS1
T3AIS0</td><td>Transmit DS3 AIS Selection. A DS3 AIS may be generated in one of following four patterns. The table below selects the DS3 AIS generation mechanism:

<u>T3AIS1</u> <u>T3AIS0</u> <u>Transmit DS3 AIS Selection</u>
0 0 ANSI defined AIS generation
Note. A one must be written to bit 0 of register 01H to set the transmitted DS3 X-bits to 1.
0 1 Framed all ones & C-bits set to 1
1 0 Unframed 1010 pattern
1 1 Unframed all ones pattern
Note: Set these bits to 0 when transmitting DS3 idle (see T3IDL in register 01H).</td></tr>
<tr><td>22</td><td>7-0</td><td>C1BZn
(n=7-0)</td><td>C1 Bit Zero Counter. An 8-bit saturating counter that counts the number of C1 bits equal to zero in both the C-bit parity mode and M13 mode. In the M13 mode the contents of this counter should be disregarded. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared on a microprocessor read cycle.</td></tr>
<tr><td>23</td><td>7-0</td><td>MEn
(n=7-0)</td><td>DS3 M-bits in Error Counter. An 8-bit saturating counter that counts the number of M-bits that are in error since the last read cycle. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared on a microprocessor read cycle.</td></tr>
<tr><td>24</td><td>7</td><td>AISX=1</td><td>DS3 AIS Detection. This bit provides a filtered indication of the receive DS3 X-bits equal to one. Two counters are used to implement this filter, a mod 16 counter CXE1 which counts the receive DS3 X-bit pairs=1, and a mod 4 counter CXE0 which counts the receive DS3 X-bit pairs=0. When either counter matures, both counters are reset. The AISX=1 bit is set to one when the CXE1 counter matures. This bit is used for determining if the X-bits=1 condition is met when R3AIS2=0, R3AIS1=0, and R3AIS0=1 in register 21H (ANSI DS3 defined AIS detection). This is a latched bit, and clears on a microprocessor read cycle. This bit will relatch if the condition that causes this bit to latch is still present.</td></tr>
<tr><td></td><td>6</td><td>AISC=0</td><td>DS3 AIS Detection. This bit provides a filtered indication of the receive DS3 C-bits equal to zero. This bit will be set if the MT90737 receives 7 contiguous DS3 frames with 30 or less DS3 C-Bits set to 1. This bit is used for determining if the C Bits = 0 condition is met when R3AIS2 = 0 & R3AIS1 = 0 & R3AIS0 = X, where X means don’t care. This is a latched bit, and clears on a microprocessor read cycle. This bit will relatch if the condition that causes this bit to latch is still present.</td></tr>
<tr><td></td><td>5</td><td>TEST</td><td>Test Bit.</td></tr>
<tr><td></td><td>4</td><td>TEST</td><td>Test Bit.</td></tr>
<tr><td></td><td>3</td><td>TEST</td><td>Test Bit.</td></tr>
<tr><td></td><td>2</td><td>TEST</td><td>Test Bit.</td></tr>
<tr><td></td><td>1</td><td>-</td><td>Not Used.</td></tr>
<tr><td></td><td>0</td><td>SEF</td><td>Severely Errored Frame Indication. A one indicates a severely errored frame has been detected. An SEF is defined as 3 out of 16 F-bits are in error in a sliding window of 16 bits. This is a latched bit, and clears on a microprocessor read cycle. This bit will relatch if the condition that causes this bit to latch is still present.</td></tr>
</table>

Initialization Sequence

The following table lists the sequence that should be followed for initializing the MT90737.

Location	Code (Hex)	Comments
1F (R/W)	F0	Resets internal counters and FIFOs.
1F (R/W)	00	Presets internal counters and FIFOs.

System Considerations

Careful attention must be paid to power supply decoupling, device layout, and printed circuit board traces. The MT90737 has separate +5 volt supply pins which provide internal circuit isolation. All V_{DD} pins must be tied together to a single +5 volt power supply in order to avoid excessive substrate currents. Mitel recommends that good quality, high frequency, low lead inductance 0.1 microfarad ceramic capacitors be used for decoupling and that they be connected in close proximity to the supply input pins on the device. If low frequency noise is present on the +5 volt supply lead, Mitel recommends that a 10 microfarad 6.3 volt tantalum capacitor be connected between +5 volts and ground.

A multilayer board that has separate planes for ground and power should be used. Because of the data rate at which the MT90737 operates, it is important that connections between devices be as short as possible. This is especially true for the DS3 receive and transmit interface connections between the MT90737 and a line interface device. In addition, the clock and data traces should be the same length.

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any I/O pin	V_{IN}	-0.3	V_{DD} + 0.3	V
3	Storage Temperature	T_{ST}	-55	150	°C

* Exceeding those values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Supply Current	I_{DD}			100	mA	
3	Operating Temperature	T_{OP}	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

DC Electrical Characteristics For CMOS - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	3.15			V	4.75V ≤V_{DD} ≤ 5.25V
2	Input Low Voltage	V_{IL}			1.65	V	4.75V ≤V_{DD} ≤ 5.25V
3	Input Leakage Current	I_{IL}			10	µA	V_{DD} = 5.25V
4	Input Capacitance	C_{IN}		3.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

DC Electrical Characteristics For TTL Type I - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	4.75V ≤V_{DD}≤ 5.25V
2	Input Low Voltage	V_{IL}			0.8	V	4.75V ≤V_{DD}≤ 5.25V
3	Input Leakage Current	I_{IL}			10	µA	V_{DD} = 5.25V
4	Input Capacitance	C_{IN}		5.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

DC Electrical Characteristics For TTL Type II - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	4.75V ≤V_{DD}≤ 5.25V
2	Input Low Voltage	V_{IL}			0.8	V	4.75V ≤V_{DD}≤ 5.25V
3	Input Leakage Current	I_{IL}		0.5	1.4	mA	V_{DD} = 5.25V; Input = 0V
4	Input Capacitance	C_{IN}		5.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: Input has a 9K (nominal) internal pull-up resistor.

DC Electrical Characteristics For TTL Type III - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75V; I_{OH} = -1.0mA
2	Output Low Voltage	V_{OL}			0.4	V	V_{DD} = 4.75V; I_{OL} = 2.0mA
3	Output Low Current	I_{OL}			2.0	mA	
4	Output High Current	I_{OH}			-1.0	mA	
5	Rise Time	t_{RISE}	5.0	11.0	20.0	ns	C_{LOAD} = 15 pF
6	Fall Time	t_{FALL}	2.0	4.0	8.0	ns	C_{LOAD} = 15 pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

DC Electrical Characteristics For TTL Type IV - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	4.75V $\leq V_{DD} \leq$ 5.25V
2	Input Low Voltage	V_{IL}			0.8	V	4.75V $\leq V_{DD} \leq$ 5.25V
3	Input leakage current	I_{IL}			10	µA	V_{DD} = 5.25V
4	Input capacitance	C_{IN}		5.5		pF	
5	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75V; I_{OH} = -4.0mA
6	Output Low Voltage	V_{OL}			0.4	V	V_{DD} = 4.75V; I_{OL} = 8.0mA
7	Output Low Current	I_{OL}			8.0	mA	
8	Output High Current	I_{OH}			-4.0	mA	
9	Rise Time	t_{RISE}	2.4	4.9	7.0	ns	C_{LOAD} = 25 pF
10	Fall Time	t_{FALL}	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

Timing Characteristics

Detailed timing diagrams for the MT90737 are illustrated in Figures 4 through 15, with values of the timing intervals following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ as applicable.

DS3 Receive Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DS3CR clock period	t_{CYC}	20.0	22.35		ns	
2	DS3CR duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%	
3	DS3DR set-up time for DS3CR↑	t_{SU}	-1.0			ns	
4	DS3DR hold time after DS3CR↑	t_H	6.0			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

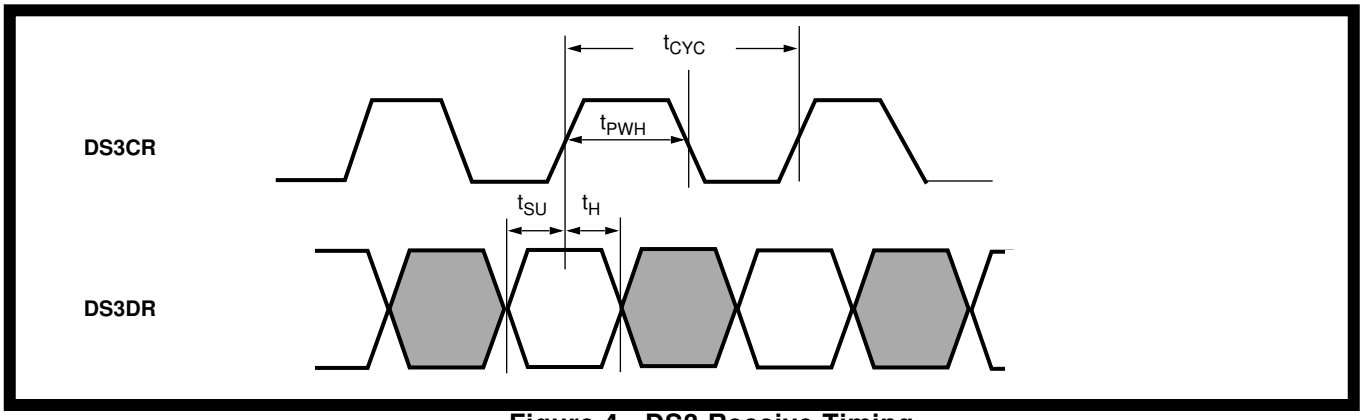


Figure 4 - DS3 Receive Timing

DS3 Transmit Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DS3CT clock period	t_{CYC}	20.0	22.35		ns	
2	DS3CT duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%	
3	DS3DT output delay after DS3CT↑	t_{OD}	4.0		8.0	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

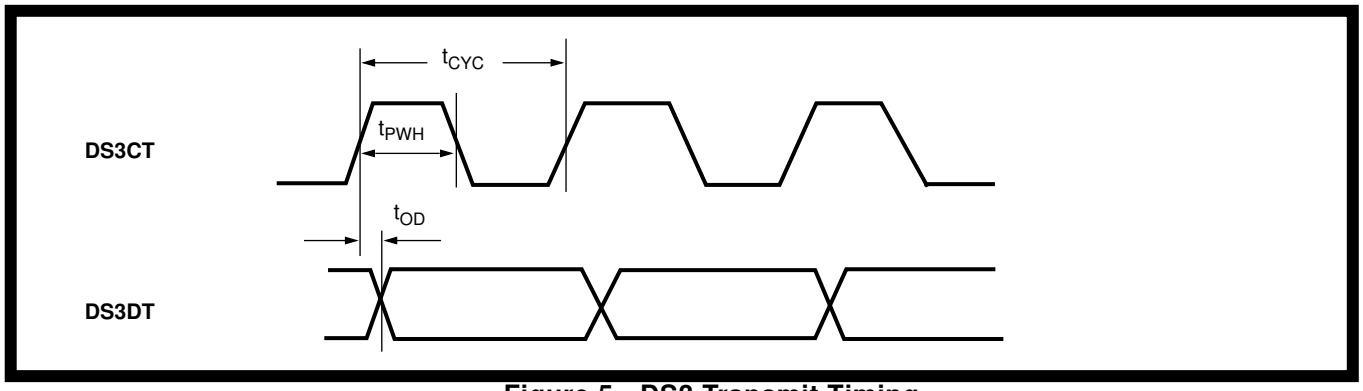


Figure 5 - DS3 Transmit Timing

DS1 Receive Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CR clock period	t_{CYC}	585		1300	ns	
2	CR high time	t_{PWH}	262		970	ns	
3	CR low time	t_{PWL}	262		356		
4	DR output delay after CR↑	t_{OD}	-12		10	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

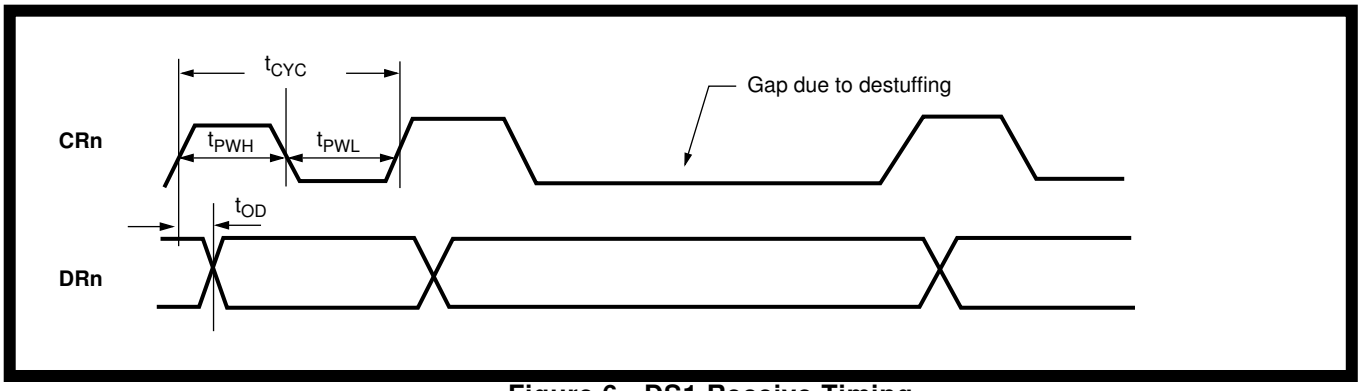


Figure 6 - DS1 Receive Timing

DS1 Transmit Timing*

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CT clock period	t_{CYC}	583	648	712.8	ns	
2	CT high time	t_{PWH}	262	324	356	ns	
3	CT low time	t_{PWL}	262	324	356	ns	
4	CT duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%	
5	DT set-up time to CT↑	t_{SU}	4			ns	
6	DT hold time after CT↑	t_H	6			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: Each DS1 input can be asynchronous with respect to another DS1 channel.

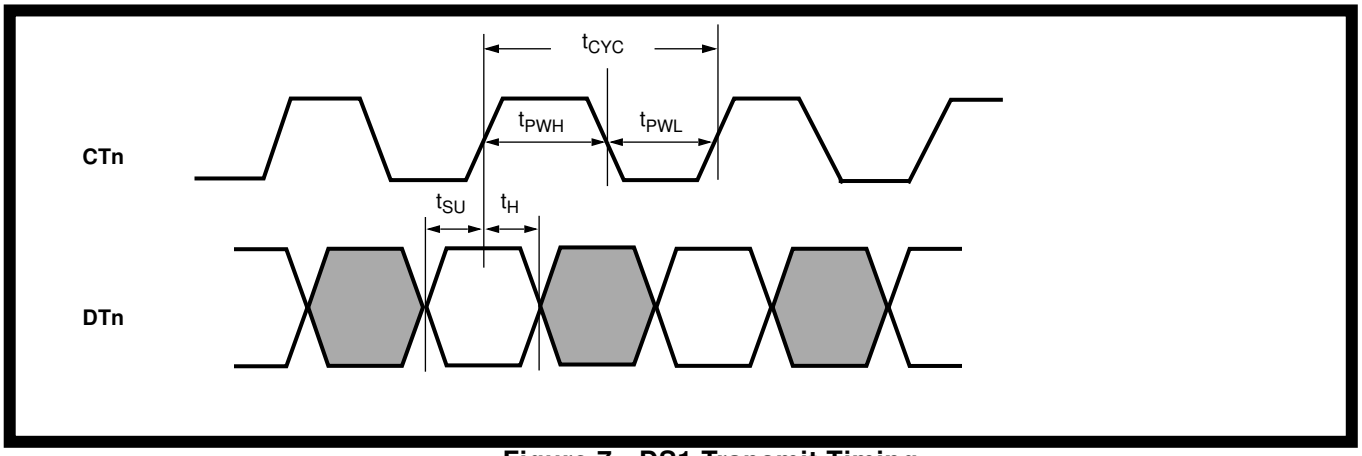


Figure 7 - DS1 Transmit Timing

C-Bit Receive Interface Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CCKR clock period	t_{CYC}		3800		ns	
2	CCKR output delay after CFMR↑	$t_{OD}^{(1)}$		3800		ns	
3	CDR output delay after CCKR↑	$t_{OD}^{(2)}$	0	13	20	ns	
4	CCKR↑ delay after CDCCR↑	$t_{D}^{(1)}$		1900		ns	
5	CDCCR↓ delay after CCKR↓	$t_{D}^{(2)}$		1900		ns	
6	CFMR pulse width (high)	t_{PW}		1900		ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

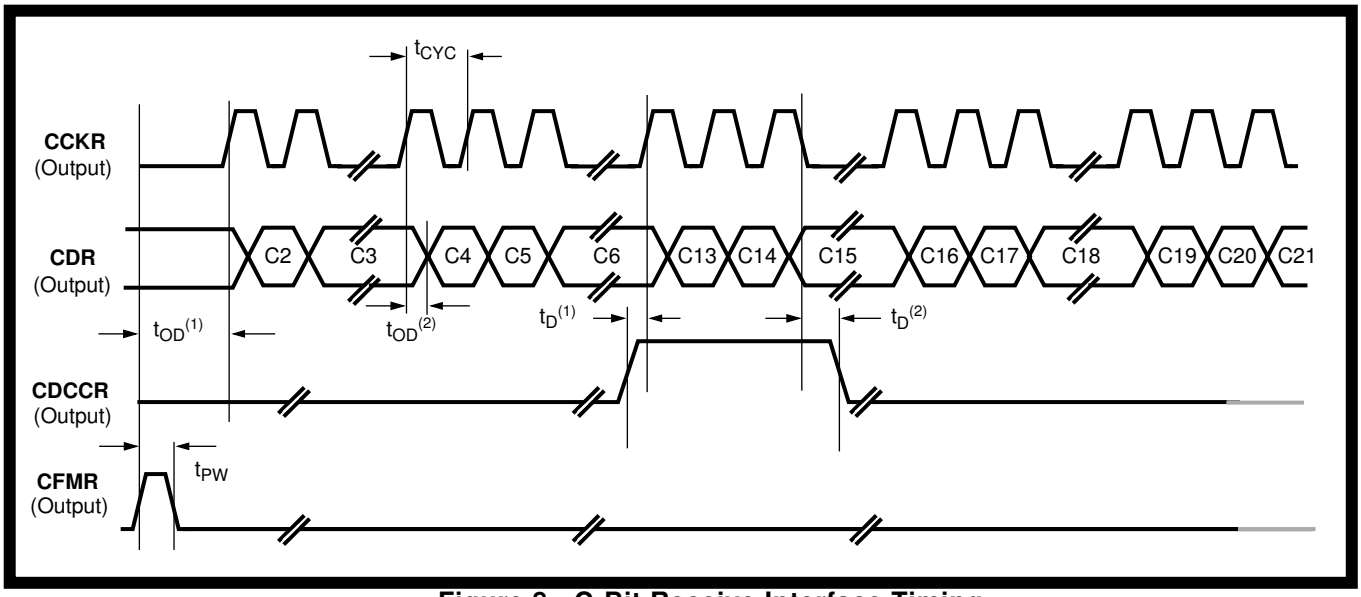


Figure 8 - C-Bit Receive Interface Timing

C-Bit Transmit Interface Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CCKT clock period	t_{CYC}		3800		ns	
2	CDT set-up time to CCKT↑	t_{SU}	20			ns	
3	CDT hold time after CCKT↑	t_H	40			ns	
4	CCKT output delay after CFMT↑	t_{OD}		3800		ns	
5	CCKT↑ delay after CDCCT↑	$t_D^{(1)}$		1900		ns	
6	CDCCT↓ delay after CCKT↓	$t_D^{(2)}$		1900		ns	
7	CFMT pulse width	t_{PW}		1900		ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

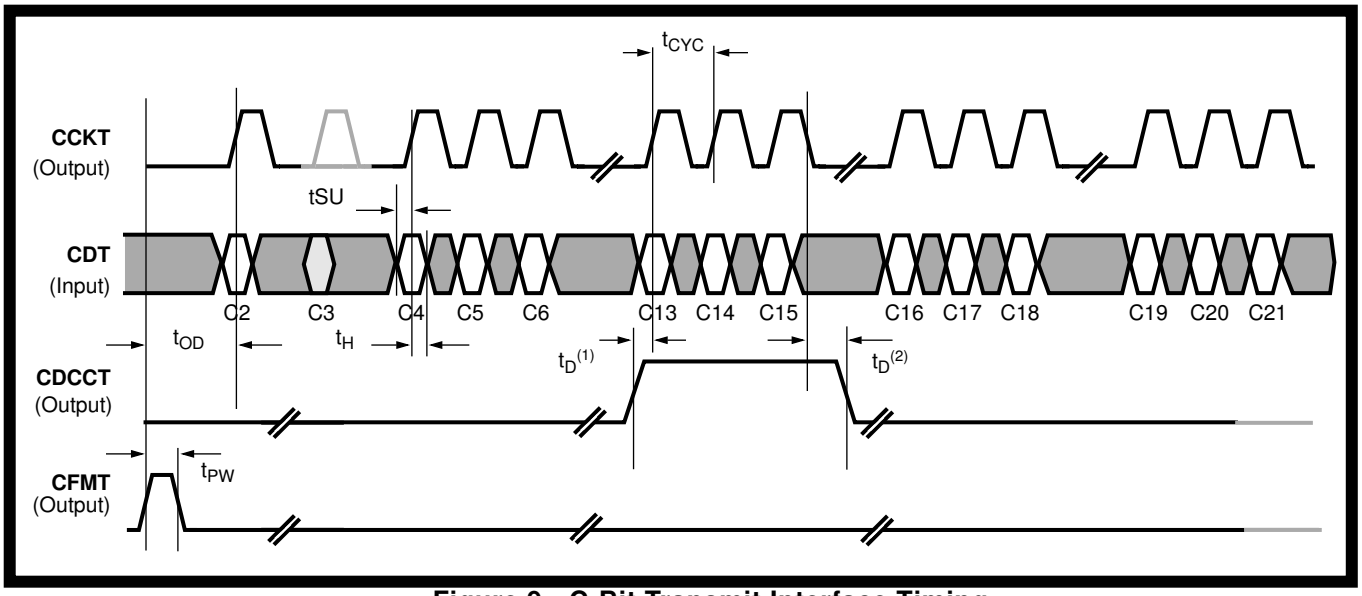


Figure 9 - C-Bit Transmit Interface Timing

Note 1: A C-bit must be transmitted as a one when not needed.
Note 2: Following normal power-up procedures, bit 7 in register 19H will be set to "0" and the extra clock pulse for the C3 bit in the CCKT clock will be present. If bit 7 is then set to "1," the extra C3 bit clock pulse will not be present.

Microprocessor Read Cycle - Multiplexed Interface*

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW}^{(1)}$	95			ns	
2	ALE wait after $\overline{RD}$ ↑	$t_{W}^{(1)}$	20			ns	
3	Addr set-up time to ALE ↓	t_{SU}	30			ns	
4	Addr hold time after ALE ↓	$t_{H}^{(1)}$	25			ns	
5	Addr hold time after $\overline{RD}$ ↓	$t_{H}^{(2)}$			20	ns	
6	Data output delay (to tristate) after $\overline{RD}$ ↑	$t_{OD}^{(1)}$	10		50	ns	
7	Data valid delay after $\overline{RD}$ ↓	$t_{OD}^{(2)}$			150	ns	
8	$\overline{SEL}$↓ delay after ALE↓	$t_{OD}^{(3)}$			80	ns	
9	$\overline{RD}$ pulse width	$t_{PW}^{(2)}$	180			ns	
10	$\overline{RD}$ wait after ALE ↓	$t_{W}^{(2)}$	25			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

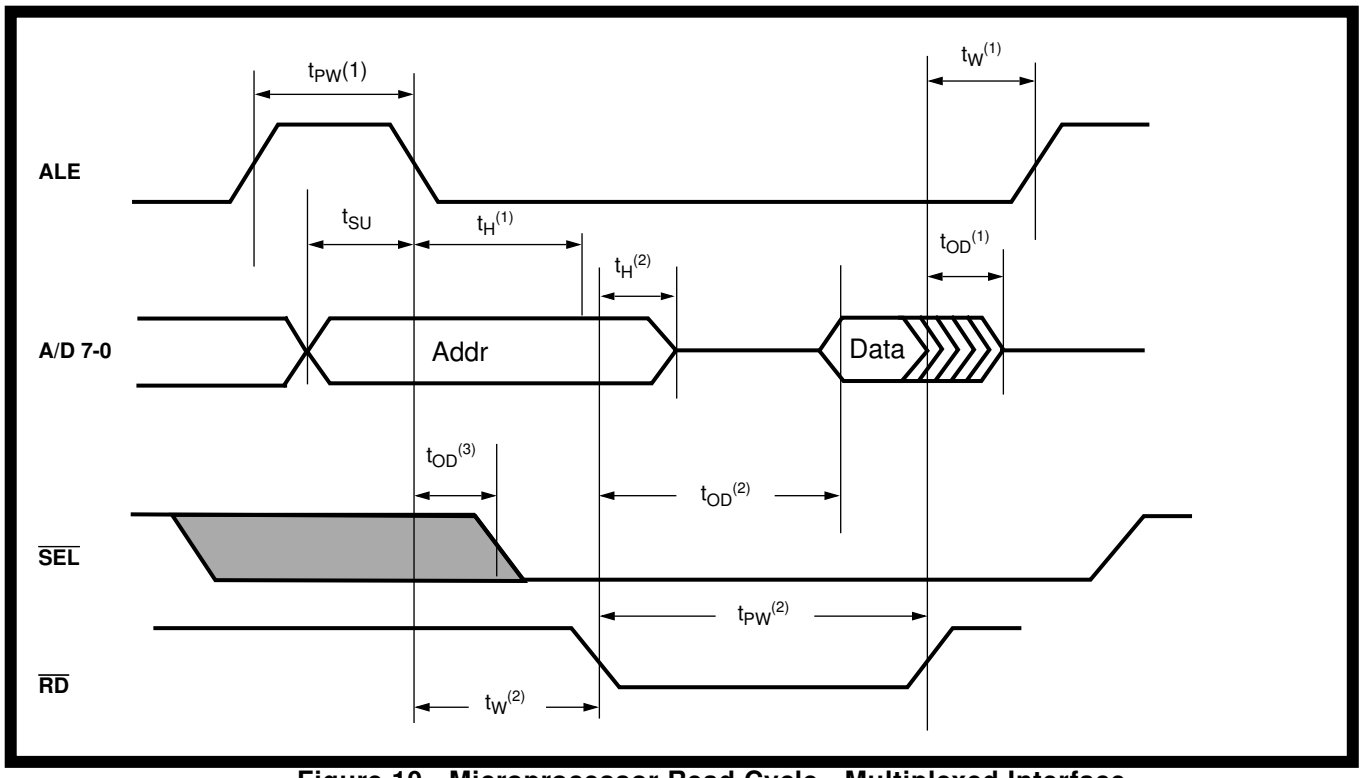


Figure 10 - Microprocessor Read Cycle - Multiplexed Interface

Microprocessor Write Cycle - Multiplexed Interface*

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW}^{(1)}$	95			ns	
2	ALE wait after $\overline{WR}$ ↑	$t_W^{(1)}$	20			ns	
3	Addr set-up time to ALE ↓	t_{SU}	30			ns	
4	Addr hold time after ALE ↓	$t_H^{(1)}$	25			ns	
5	Data hold time after $\overline{WR}$ ↑	$t_H^{(2)}$	20			ns	
6	$\overline{SEL}$ output delay after ALE↓	t_{OD}			80	ns	
7	$\overline{WR}$ pulse width	$t_{PW}^{(2)}$	200			ns	
8	$\overline{WR}$ wait after ALE ↓	$t_W^{(2)}$	25			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

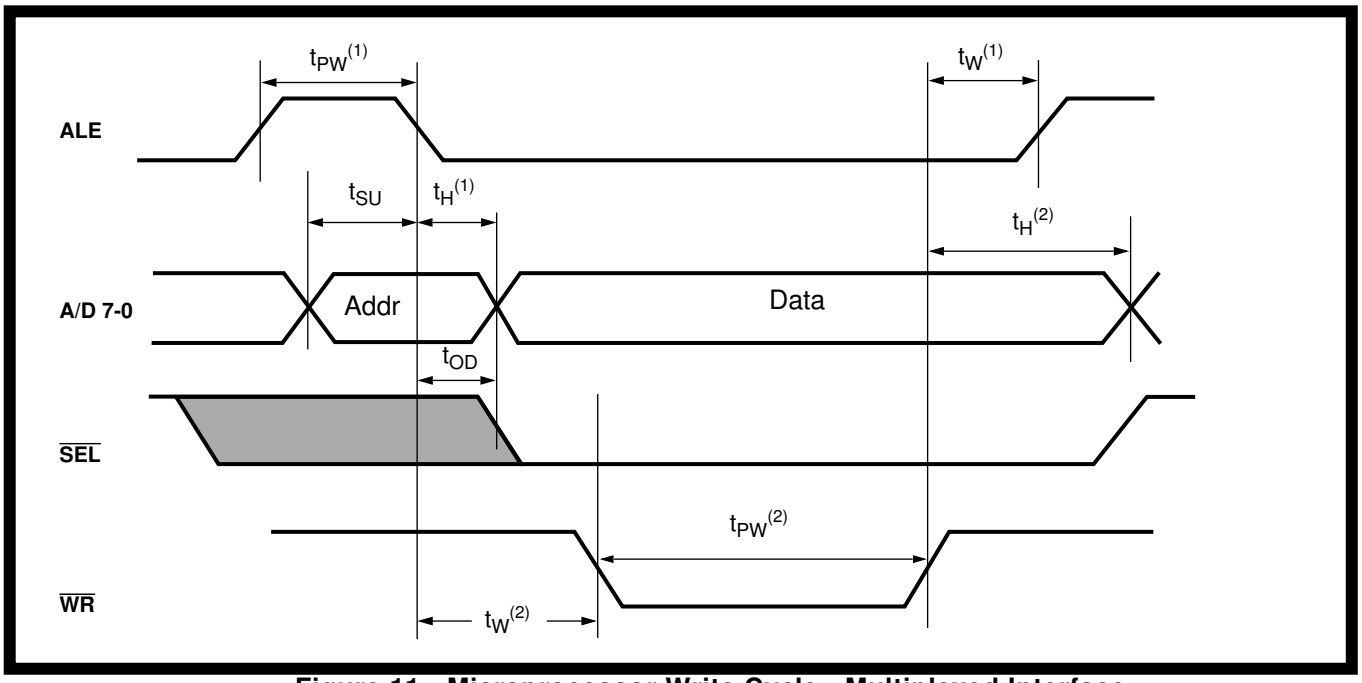


Figure 11 - Microprocessor Write Cycle - Multiplexed Interface

Microprocessor Read Cycle - Intel Interface*

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ADR hold time after $\overline{RD}\uparrow$	$t_H^{(1)}$	0			ns	
2	ADR set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(1)}$	20			ns	
3	DATA valid delay after $\overline{RD}\downarrow$	t_D			60	ns	
4	DATA float time after $\overline{RD}\uparrow$	t_F			80	ns	
5	$\overline{RD}$ pulse width	t_{PW}	80			ns	
6	$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU}^{(2)}$	10			ns	
7	$\overline{SEL}\uparrow$ hold time after $\overline{RD}\uparrow$	$t_H^{(2)}$	0			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

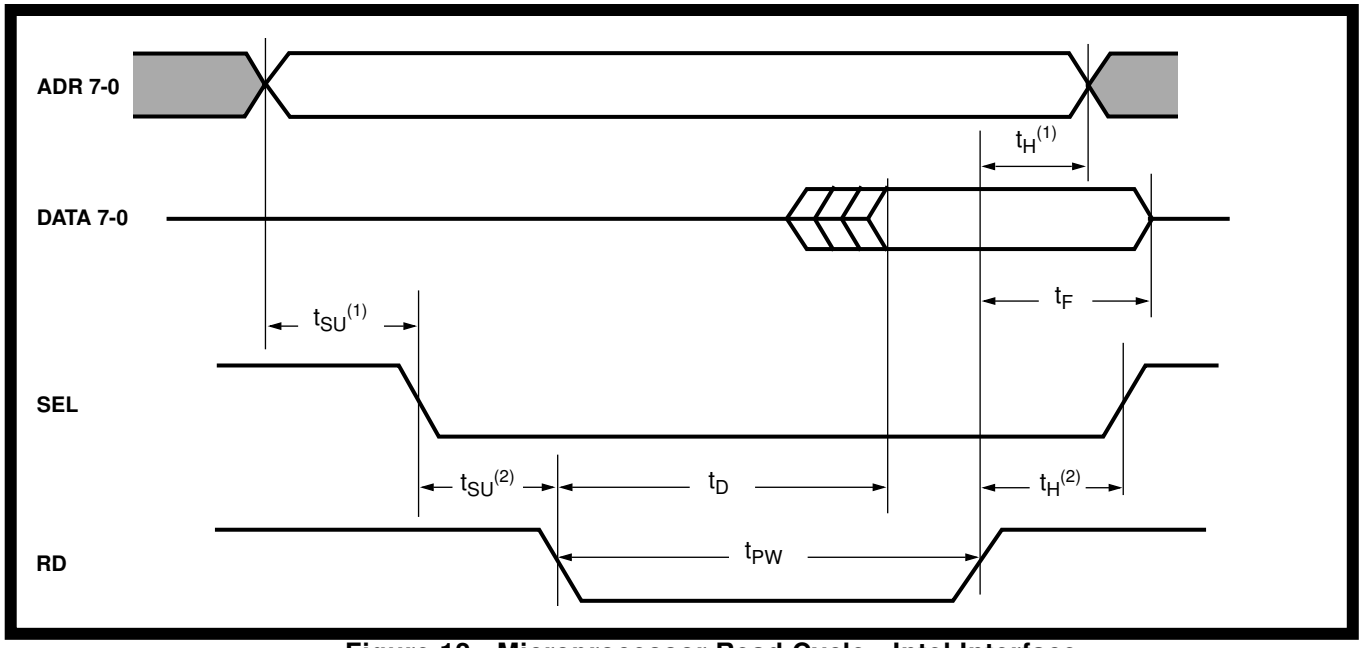


Figure 12 - Microprocessor Read Cycle - Intel Interface

Microprocessor Write Cycle - Intel Interface

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ADR hold time after $\overline{WR}\uparrow$	$t_H^{(1)}$	0			ns	
2	ADR set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(1)}$	20			ns	
3	DATA valid set-up time to $\overline{WR}\uparrow$	$t_{SU}^{(2)}$	20			ns	
4	DATA hold time after $\overline{WR}\uparrow$	$t_H^{(2)}$	5			ns	
5	$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU}^{(3)}$	10			ns	
6	$\overline{WR}$ pulse width	t_{PW}	80			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

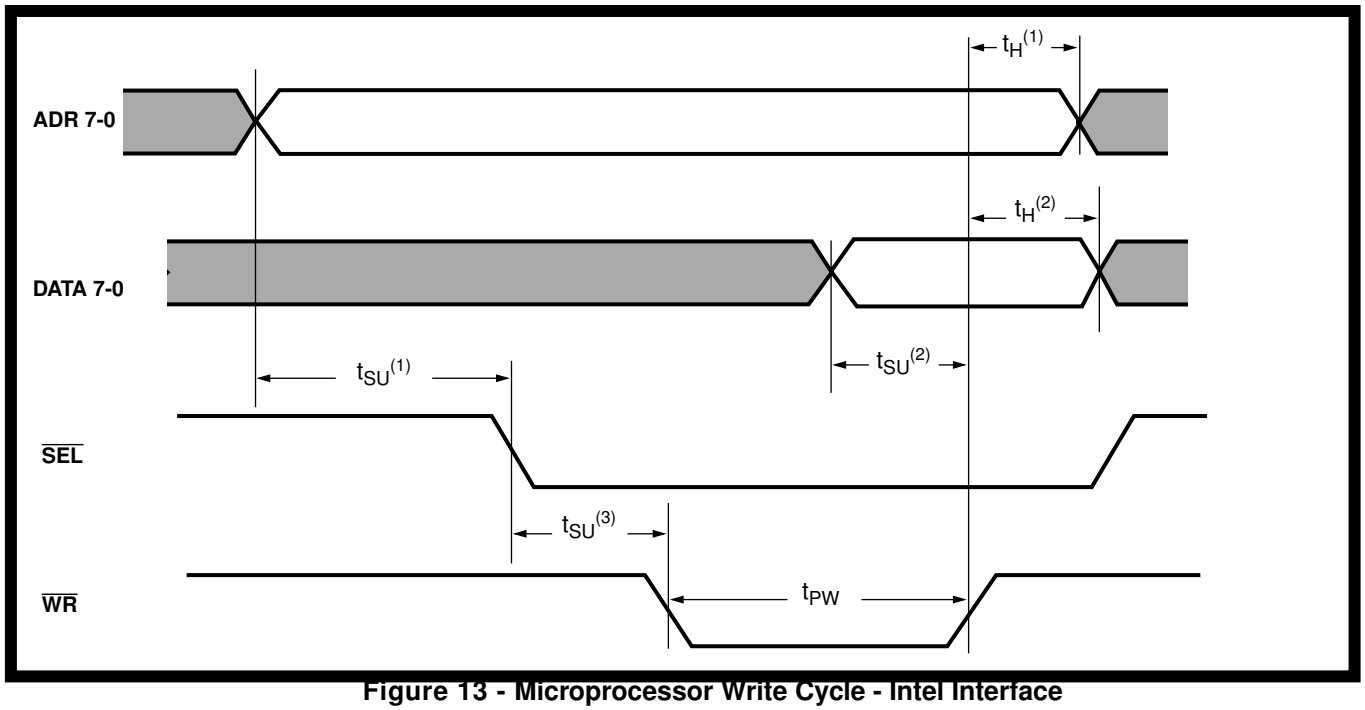


Figure 13 - Microprocessor Write Cycle - Intel Interface

Microprocessor Read Cycle - Motorola Interface

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ADR hold time after $\overline{SEL}\uparrow$	$t_H^{(1)}$	0			ns	
2	ADR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(1)}$	20			ns	
3	DATA valid delay after $\overline{DTACK}\downarrow$	$t_D^{(1)}$		16		ns	
4	DATA hold time after $\overline{SEL}\uparrow$	$t_H^{(2)}$			25	ns	
5	$\overline{SEL}$ pulse width	$t_{PW}^{(3)}$	60			ns	
6	RD/$\overline{WR}\uparrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(2)}$	20			ns	
7	RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_H^{(3)}$	0			ns	
8	$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_D^{(2)}$			5	ns	
9	$\overline{DTACK}$ pulse width	$t_{PW}^{(2)}$	0		4	µs	
10	$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			3	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
† The $\overline{DTACK}$ signal lead is tristated when $\overline{SEL}$ is high.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

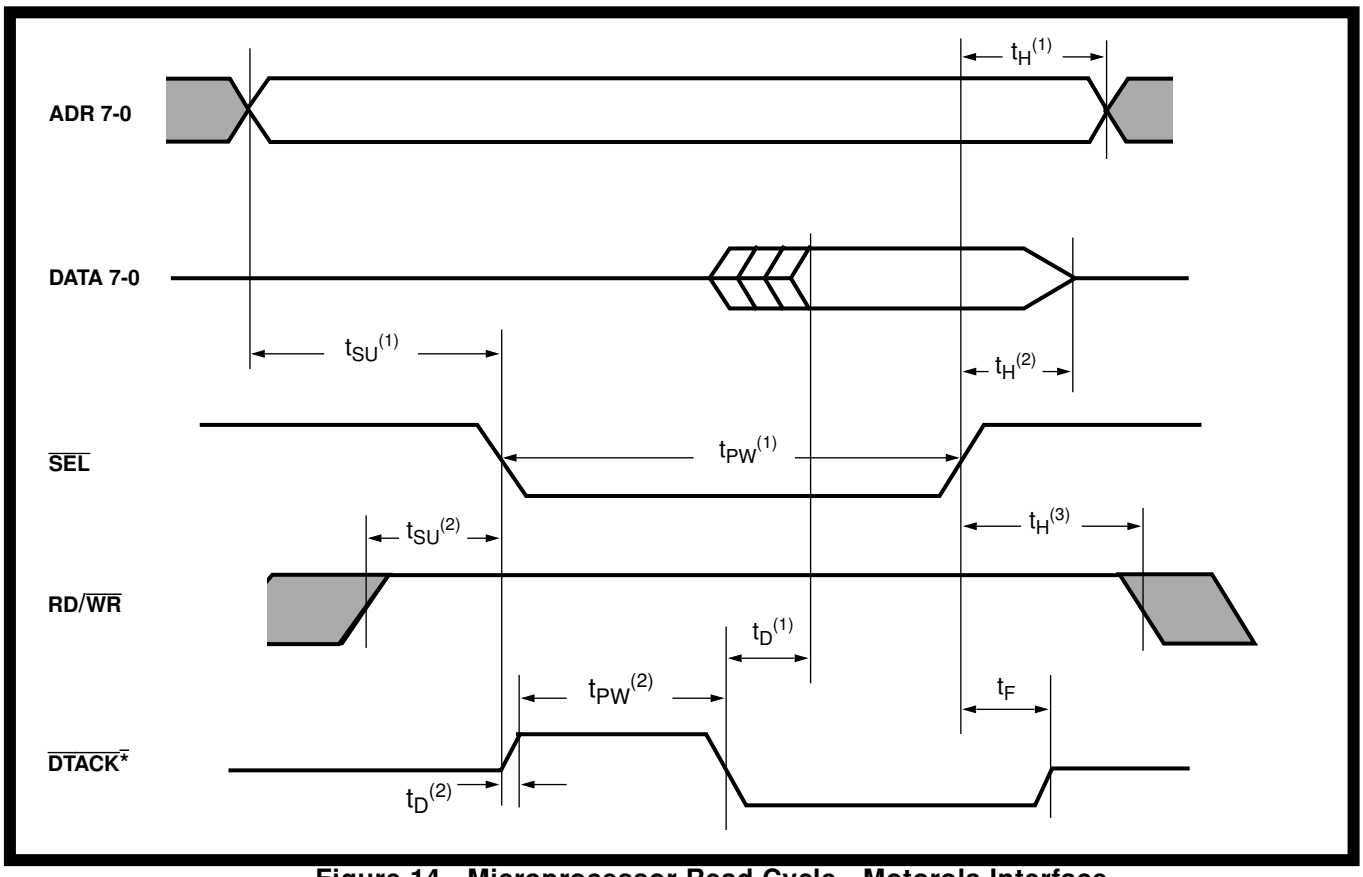


Figure 14 - Microprocessor Read Cycle - Motorola Interface

Microprocessor Write Cycle - Motorola Interface

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ADR hold time after $\overline{SEL}\uparrow$	$t_H^{(1)}$	0			ns	
2	ADR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(1)}$	20			ns	
3	DATA valid set-up time to $\overline{SEL}\uparrow$	$t_{SU}^{(2)}$	10			ns	
4	DATA hold time after $\overline{SEL}\uparrow$	$t_H^{(2)}$	5			ns	
5	$\overline{SEL}$ pulse width	$t_{PW}^{(1)}$	60			ns	
6	RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU}^{(3)}$	20			ns	
7	RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_H^{(3)}$	0			ns	
8	$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D		25		ns	
9	$\overline{DTACK}$ pulse width	$t_{PW}^{(2)}$	20			ns	
10	$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
† The $\overline{DTACK}$ signal lead is tristated when $\overline{SEL}$ is high.
* Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

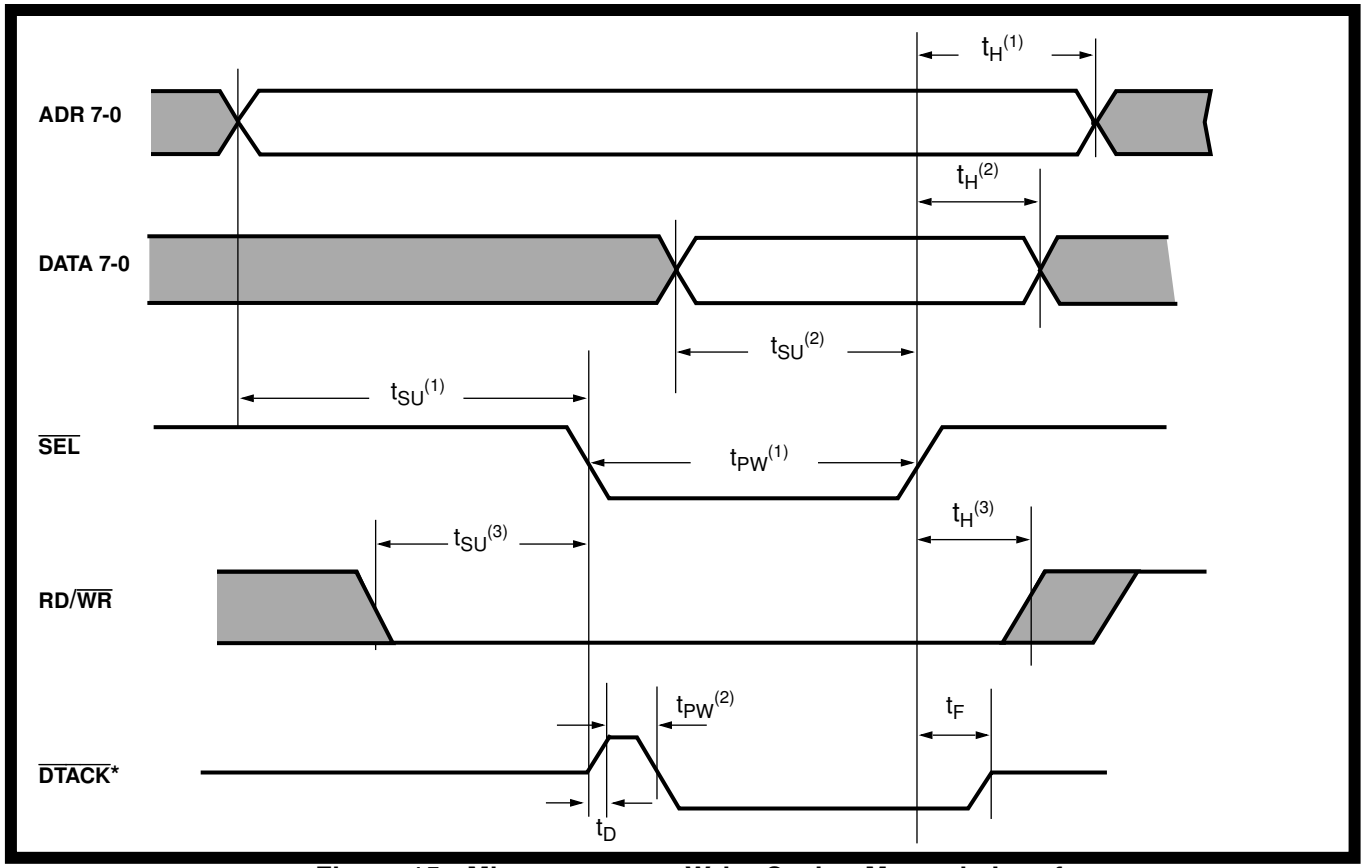


Figure 15 - Microprocessor Write Cycle - Motorola Interface

Packaging

The MT90737 device is packaged in a 208-pin plastic quad flat pack suitable for surface mounting. All dimensions shown are in millimeters and are nominal unless otherwise noted.

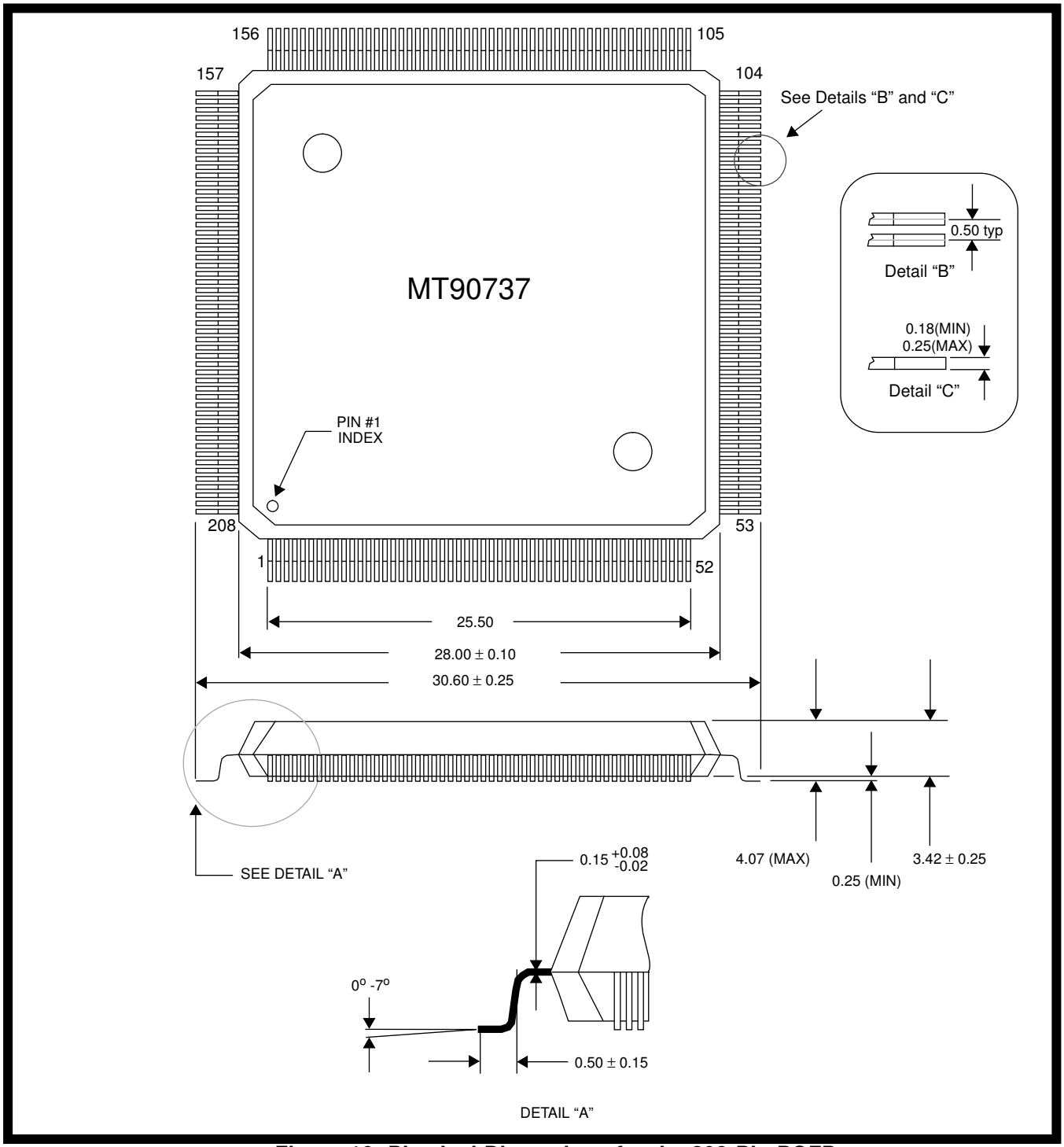


Figure 16- Physical Dimensions for the 208-Pin PQFP

Notes: