

XGA Flat Panel Controller

FEATURES

General

- Auto configuration of sampling clock frequency, phase, H/V center, as well as white balance.
- Auto detection of present or non-present or over range sync signals and their polarities.
- Composite sync separation and odd/even field detection of interlaced video.
- No external memory required.
- On-chip output PLL provide clock frequency fine-tune (inverse, duty cycle and delay).
- Selection of serial 2-wire I²C or 3-wire serial or 8-bit direct host interface to 8-bit MCU.
- 3.3V supplier, 5V I/O tolerance in 208-pin PQFP package.

Input Processor

- Single RGB (24-bit) or Dual RGB (48-bit) input rates up to 100MHz.
- Support both non-interlaced and interlaced RGB graphic input signals.
- YUV 4:2:2 or YUV 4:1:1 (CCIR601) interlaced video input.
- Glue-less connection to Philips SAA711x digital video decoder.
- Built-in YUV to RGB color space converter.
- Compliant with digital LVDS/PanelLink TMDS input interface.
- PC input resolution up to XGA 1024x768 @85Hz.

Video Processor

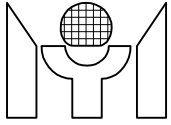
- Independent programmable Horizontal and Vertical scaling up ratios from 1 to 32
- Flexible de-interlacing unit for digital YUV video input data.
- Zoom to full screen resolution of de-interlaced YUV video data stream.
- Built-in programmable gain control for white balance alignments.
- Built-in programmable 8-bit gamma correction table.
- Built-in programmable temporal color dithering.
- Built-in programmable interpolation look-up table.
- Support smooth panning under viewing window change.

Output Processor

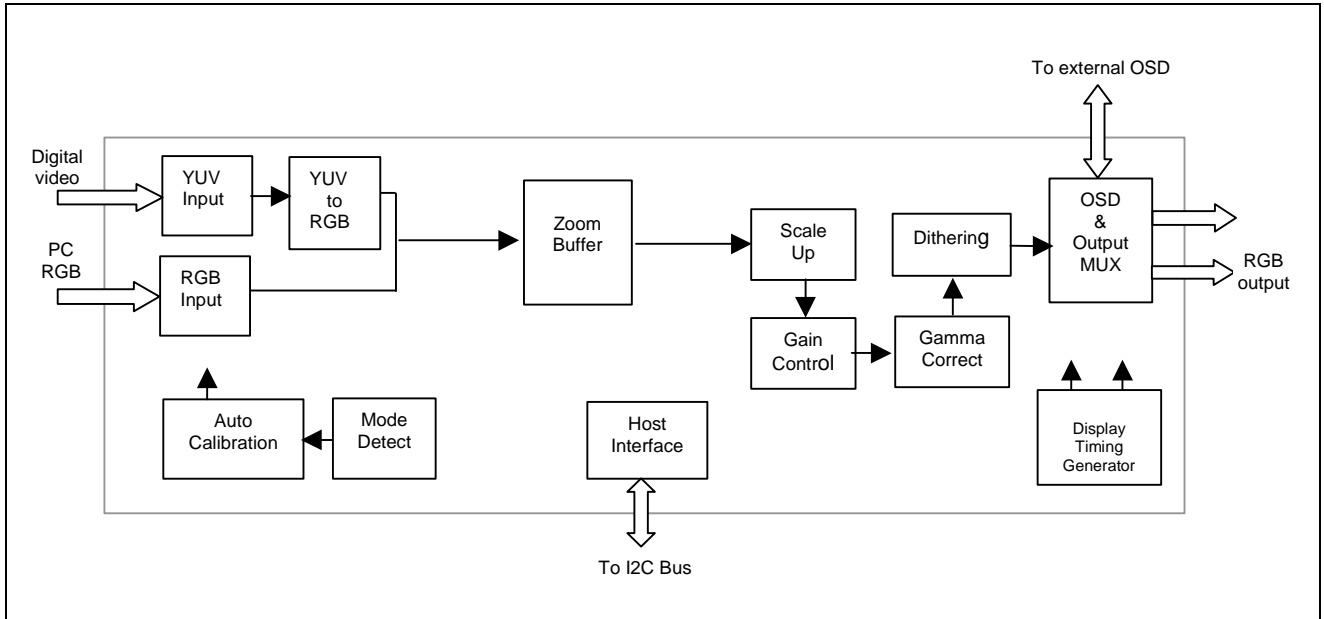
- Single pixel (18/24-bit) or Dual pixel (36/48-bit) per clock digital RGB output.
- Built-in output timing generator with programmable clock and H/V sync.
- Support VGA/SVGA/XGA display resolution.
- Overlay input interface with external OSD controller.
- Double scan capability for interlaced input.

GENERAL DESCRIPTION

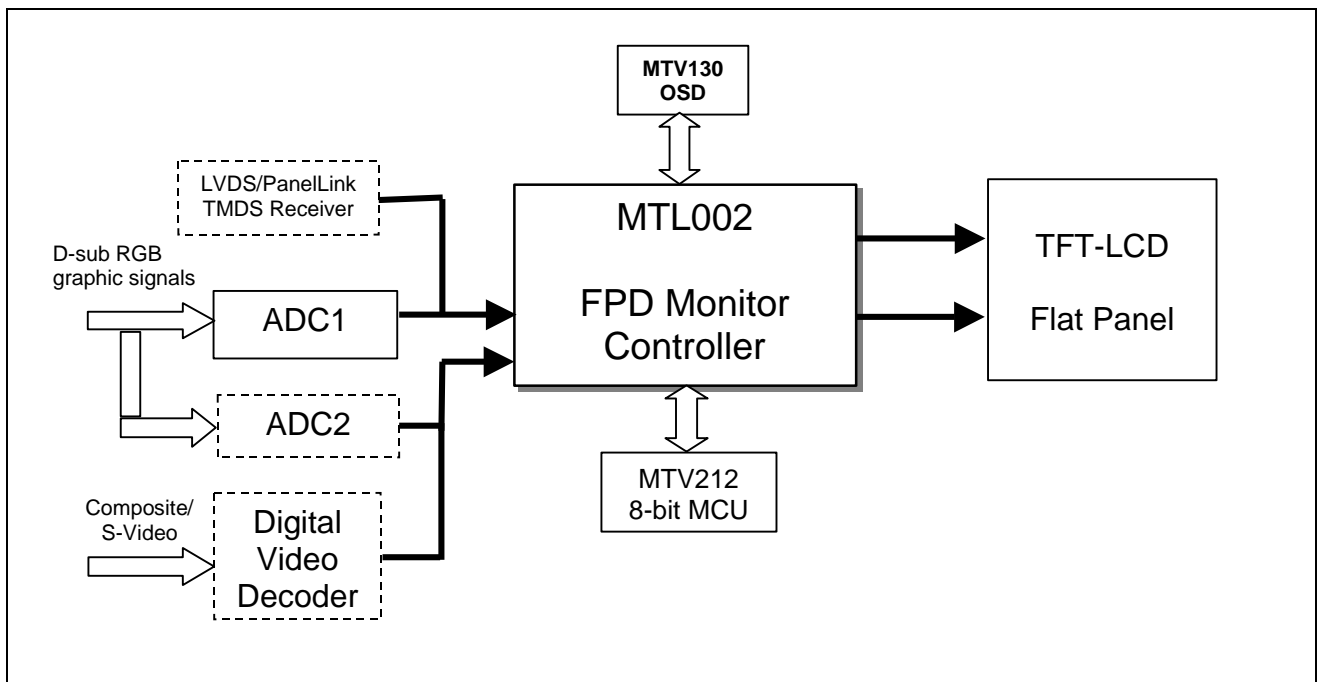
The MTL002 Flat Panel Display (FPD) Controller is an input format converter for TFT-LCD Monitor or LCD TV application which accepts 15-pin D-sub RGB graphic signals (through ADC), YUV signals from digital video decoder or digital RGB graphic signals from PanelLink TMDS receiver. It includes a RGB/YUV input processor, video scaling up processor, OSD input interface and output display processor in 208-pin PQFP.



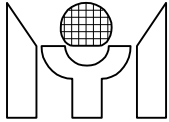
BLOCK DIAGRAM



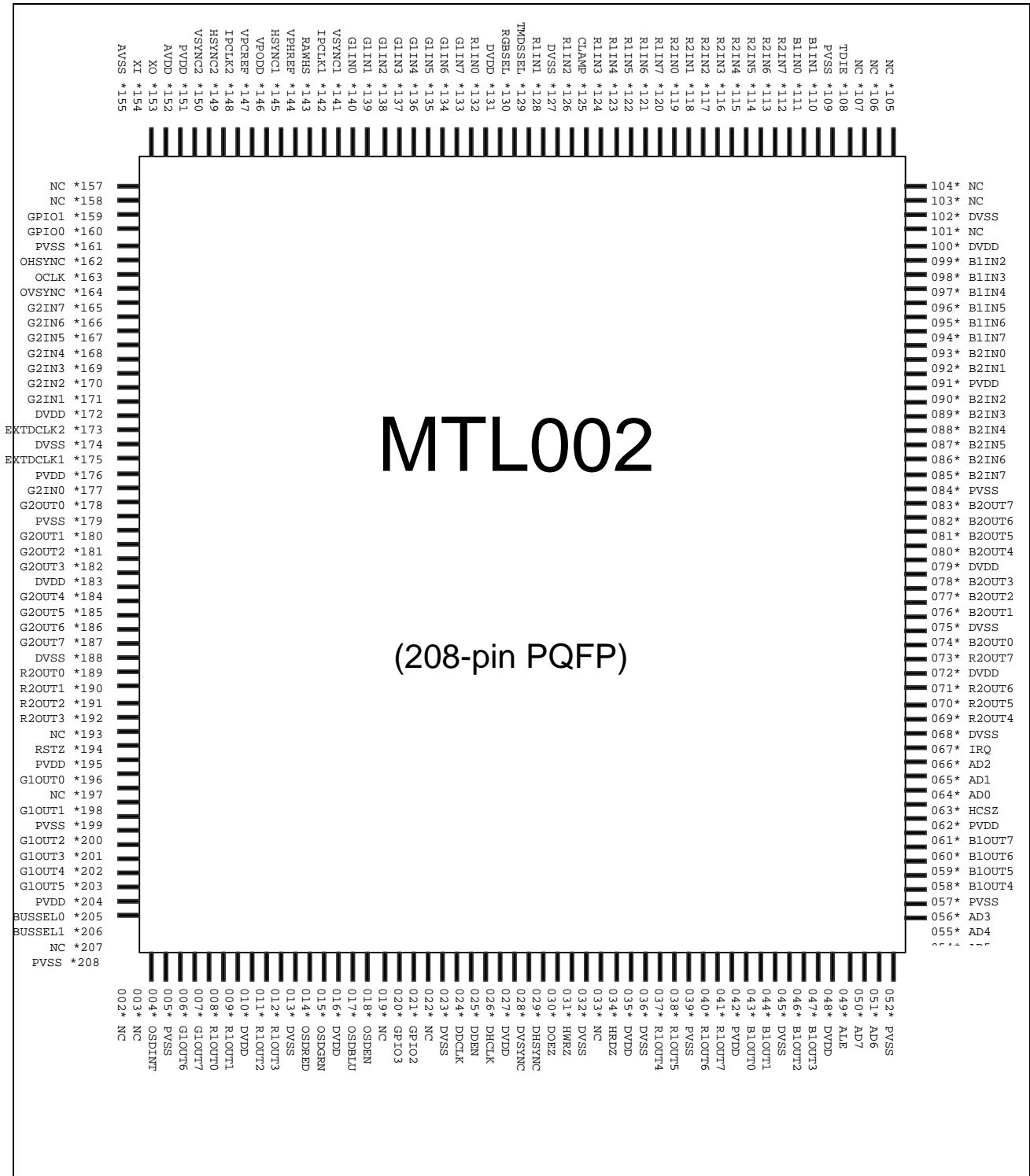
APPLICATIONS

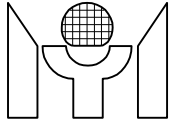


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1. PIN CONNECTION





2. PIN DESCRIPTION

ADC1 Input Interface (RGB or TMDS Input Data)

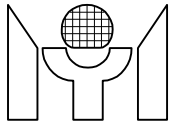
Name	Type	Pin#	Description
IPCLK1	I	142	Input pixel clock 1
VSYNC1	I	141	Input Vertical sync 1
HSYNC1/CS1	I	145	Input Horizontal or Composite sync 1
R1IN[7:0]	I	120-124, 126,128, 132	Red channel or TMDS input data (Single/Dual ADC)
G1IN[7:0]	I	133-140	Green channel or TMDS input data (Single/Dual ADC)
B1IN[7:0]	I	94-99, 110-111	Blue channel or TMDS input data (Single/Dual ADC)
RAWHS/SOG	I	143	Input source HSYNC or Input Sync On Green
TDIE	I	108	TMDS digital input enable
RGBSEL	O	130	Input select. 1:RGB input, 0:YUV input
TMDSSSEL	O	129	TMDS input select, active high
CLAMP	O	125	Clamp pulse output for ADC

ADC2 Input Interface (YUV or RGB or TMDS Input Data)

Name	Type	Pin#	Description
IPCLK2	I	148	Input pixel clock 2
VSYNC2	I	150	Input Vertical sync 2
HSYNC2/CS2	I	149	Input Horizontal or Composite sync 2
R2IN[7:0]/YIN[7:0]	I	112-119	Red or Y channel or TMDS input data (Single/Dual ADC)
G2IN[7:0]	I	165-171, 177	Green channel or TMDS input data (Single/Dual ADC)
B2IN[7:0]/UVIN[7:0]	I	85-90, 92-93	Blue or UV channel or TMDS input data (Single/Dual ADC)
VPHREF	I	144	Input Video Horizontal reference signal
VPCREF	I	147	Input Video clock enable
VPODD	I	146	Input Video ODD/EVEN field signal

Display Output Interface

Name	Type	Pin#	Description
DDEN	O	25	Display data output enable
DVSYNC	O	28	Display Vertical sync output
DHSYNC	O	29	Display Horizontal sync output
DDCLK	O	24	Display output clock
DHCLK	O	26	Display half rate output clock
DOE#	I	30	Display port output enable, "1" will tri_state all Display port output signals
R1OUT[7:0]	O	41-40 38-37, 12-11,9-8	Red output even data , bit[7:2] for 6-bit panel
G1OUT[7:0]	O	7-6, 203-200, 198,196	Green output even data , bit[7:2] for 6-bit panel
B1OUT[7:0]	O	61-58,47, 46,44,43	Blue output even data , bit[7:2] for 6-bit panel
R2OUT[7:0]	O	73,71-69, 192-189	Red output odd data , bit[7:2] for 6-bit panel
G2OUT[7:0]	O	187-184, 182-180, 178	Green output odd data , bit[7:2] for 6-bit panel



B2OUT[7:0]	O	83-80, 78-76,74	Blue output odd data , bit[7:2] for 6-bit panel
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Host Interface

Name	Type	Pin#	Description
RST#	I	194	System reset input, active low.
AD[7:0]	I/O	50-51, 54-56, 66-64	The address and data bus of 8-bit direct interface or 2-wire I ² C / 3-wire series bus Bit 2: SDAO, 3-wire serial bus data out Bit 1: SDA, serial bus data / 3-wire serial bus data in Bit 0: SCK, serial bus clock
HWR#	I	31	Host write strobe, active low
HRD#	I	34	Host read strobe, active low
ALE	I	49	Host address latch enable for 8-bit direct bus
HCS#	I	63	Host chip select
BUSSEL[1:0]	I	206,205	Bus mode selection. 0x: 3-wire bus, 10: I ² C bus, 11: 8-bit direct bus
IRQ	O	67	Interrupt request output

OSD Interface

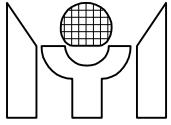
Name	Type	Pin#	Description
OCLK	O	163	Clock for external OSD
OVSYNC	O	164	Vertical sync for external OSD
OHSYNC	O	162	Horizontal sync for external OSD
OSDRED	I	14	OSD red input
OSDGRN	I	15	OSD green input
OSDBLU	I	17	OSD blue input
OSDINT	I	4	OSD intensity input
OSDEN	I	18	OSD overlay enable

Other Interface

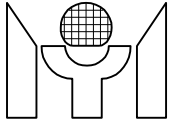
Name	Type	Pin#	Description
XI	I	154	Oscillator frequency input
XO	O	153	Oscillator frequency output
EXTDCLK1	I	175	External display clock input 1
EXTDCLK2	I	173	External display clock input 2
GPIO[3:0]	I/O	20-21, 159-160	General purpose I/O or Bit 1: ADVS, Vertical sync for A/D converter Bit 0: ADHS, Horizontal sync for A/D converter Default: Input direction
NC	-	1-3, 19, 22, 33, 53, 101, 103-107, 156-158, 193, 197, 207	No connection

3.3V Power and Ground

Name	Pin#	Description
DVDD	10, 16, 27, 35, 48, 72, 79, 100, 131, 172, 183	Digital power 3.3V
DVSS	13, 23, 32, 36, 45, 68, 75, 102, 127, 174, 188	Digital ground
PVDD	42, 62, 91, 151, 176, 195, 204	Pad power 3.3V
PVSS	5, 39, 52, 57, 84, 109, 161, 179, 199, 208	Pad ground



AVDD	152	Analog power 3.3V
AVSS	155	Analog ground



3. FUNCTIONAL DESCRIPTION

3.1 Input Processor

General Description

The function of Input Interface is to provide the interface between MTL002 and external input devices. It can process non-interlaced and interlaced RGB graphic input, YUV video input, and digital RGB input compliant with digital LVDS/PanelLink TMDS interface. It also contains the built-in YUV to RGB color space converter.

3.1.1 RGB Input Format

The RGB input port works in two modes: Single Pixel mode (24 bits) and Double Pixel mode (48 bits). For Single Pixel mode, either ports R/G/B1IN[7:0] or R/G/B2IN[7:0] selected by Reg.16h/D0 can be chosen to be internally sampled. For the Double Pixel mode, besides ports R/G/B1IN[7:0], ports R/G/B2IN[7:0] are also needed. The R/G/B1IN ports are sampled at the rising edge of the RGB input clock, and the R/G/B2IN ports are sampled at the falling edge.

3.1.2 TMDS Input Format

The Digital RGB input port works just in the same way as Sec 3.1.1 except that pin "Digital Input Enable DIEN" is needed.

With a flexible single or double pixel input interface, the supported format is up to true color, including 18 bit/pixel or 24 bit/pixel in 1 or 2 pixels/clock mode.

3.1.3 YUV Input Format

The YUV input port supports interlaced video data from the most common video decoder ICs like SAA711x. The 16 bit data bus is shared with ports R2IN[7:0] and B2IN[7:0]. The 16 bit data is sampled at the rising edge of the shared video clock VPCLK when the shared data enable HREF is active. The formats supported are YUV4:1:1 and YUV4:2:2 with CCIR601 standard.

3.1.4 Input HSYNC Path

In addition to the pins HSYNC1/2, MTL002 provides another pin RAWHS to support the Sync Processor. In general, the synchronous HSYNC input for HSYNC1 or HSYNC2 generated by an ADC may have a very narrow pulse width and a different polarity comparing to the original HSYNC provided by the source. The RAWHS input provides the path of original HSYNC connection to MTL002, thus making Sync Processor in MTL002 working properly.

3.1.5 YUV to RGB Converter

Is used to convert YCbCr format into RGB format. The basic equations are as follows:

$$\begin{aligned}R &= Y + 1.371(Cr - 128) \\G &= Y - 0.698(Cr - 128) - 0.336(Cb - 128) \\B &= Y + 1.732(Cb - 128)\end{aligned}$$

3.1.6 De-interlace mode

For the interlace input, MTL002 features several de-interlacing algorithms for processing interlaced video data depending on the type of input images.

Å **Toggle Mode**

In this mode, only one field is displayed at the time. First field and second field are toggling displayed. The missing lines are calculated by duplicating the neighboring lines. This mode gives good quality for moving pictures.

Å **Spatial Mode**

In this mode, two fields are toggling displayed just like the Toggle mode. The missing lines are calculated by interpolating the neighboring lines. This mode has a generally good quality for still and moving pictures.



3.1.7 Sync Processor

The V/H SYNC processing block performs the functions of Composite signal separation/insertion, SYNC inputs presence check, frequency counting, polarity detection and control. It contains a de-glitch circuit to filter out any pulse shorter than one OSC period which is treated as noise among V/H SYNC pulses.

̂ V/H SYNC Frequency Counter

MTL002 can measure VSYNC/HSYNC frequency counted in proper clock and save the information in the register. Users can read the figure and calculate VSYNC/HSYNC frequency as following formulas:

$$f_{\text{vsync}} = f_{\text{osc}} / N_{\text{vsync}} \quad F \ 1/256$$

$$f_{\text{hsync}} = f_{\text{osc}} / N_{\text{hsync}} \quad F \ 8$$

,Where f_{vsync} : VSYNC frequency
 f_{hsync} : HSYNC frequency
 f_{osc} : oscillator clock with 14.31818 MHz
 N_{vsync} : counted number of VSYNC
 N_{hsync} : counted number of HSYNC

̂ V/H SYNC Presence Check

This function checks the input VSYNC, where Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz and the input HSYNC, where Hpre flag is set when HSYNC is over 10Khz or cleared when HSYNC is under 10Hz.

̂ V/H Polarity Detect

This function detects the input VSYNC/HSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted.

̂ Composite SYNC separation/insertion

MTL002 continuously monitors the input HSYNC. If the input VSYNC can be extracted from it, a CVpre flag is set. MTL002 can insert HSYNC pulse during Composite VSYNC's active time and the insertion frequency can adapt to the original HSYNC's.

3.1.8 Auto Tune

Auto Tune function consists of Auto Position which automatically centering the screen and Auto Calibration which contains Phase Calibration, Histogram, Min/Max Value, and Pixel Grab that are described in the following paragraphs. With such auto adjustment support it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured. Firmware can adjust input image registers automatically by reading Auto Tune's registers in single or burst mode.

̂ Auto Position

MTL002 provides Horizontal/Vertical back porch and active region values. Users can use these values to set input sample registers to aid in centering the screen automatically.

̂ Phase Calibration

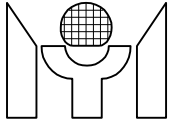
MTL002 provides Auto Calibration registers to measure the quality of current ADC's phase and frequency. The biggest Auto Calibration registers value means the right value of ADC's phase and frequency. MTL002 has two kinds of algorithms to calculate Auto Calibration's value. One is traditional Difference method, another is MYSON's proprietary method. The latter one is recommended for a better performance.

̂ Histogram

Histogram is the total number of input pixels below/above one threshold value for individual R, G, B colors. This advanced function helps Firmware to analyze ADC performance. Usually Firmware can use the information to measure ADC's noise margin, adjust its offset and gain, or even aid in the mode detection.

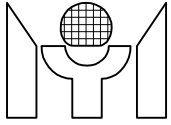
̂ Min/Max Value

Min/Max value is the minimum or maximum pixel value within the specified input active image region for each RGB channel. This information is usually used to adjust ADC's offset and gain.



À **Pixel Grab**

Pixel Grab means user can grab a single input pixel at any one point. The position of the point can be programmed by the user. This is another traditional method to measure ADC's phase and frequency.

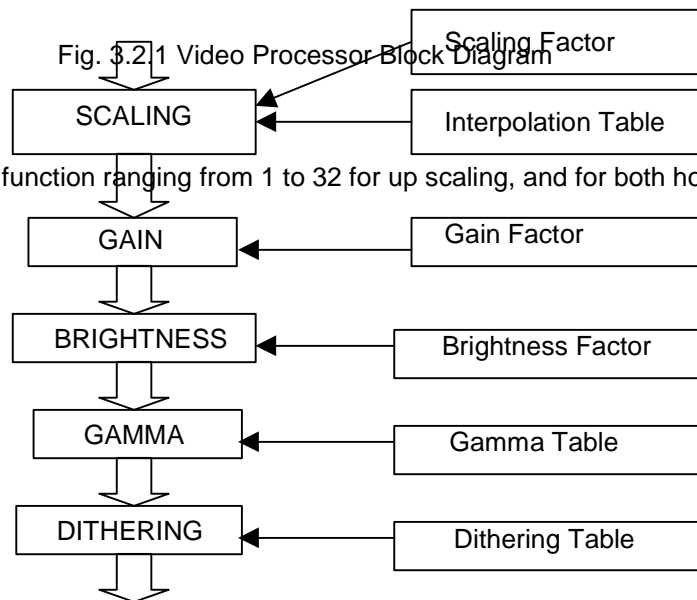


3.2 Video Processor

General Description

MTL002 possesses a powerful and programmable video processor by providing the following functions: Scaling Up, Gain Control, Brightness Control, Gamma Correction, and Dithering Control.

The block diagram of Video Processor is as follows:



3.2.1 Scaling

MTL002 provides scaling function ranging from 1 to 32 for up scaling, and for both horizontal and vertical

processing. For scaling up, both horizontal and vertical processing, MTL002 provides four methods:

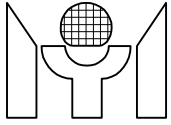
- ⌘ **Pass Mode:** Image will be passed through without taking scaling factor into account.
- ⌘ **Duplicate Mode:** Image will be scaled up based on the scaling factor. Every point of output image comes from the input. In this method, the output image will have a good contrast but the picture could be non-uniformed.
- ⌘ **Bilinear Mode:** Image will be scaled up based on the scaling factor. Every point of output image data will be filtered by bilinear filter. In this method, the output image will have a good scaling quality but the picture could be blurred.
- ⌘ **Interpolation Table Mode:** Image will be scaled up based on the scaling factor. The user-defined filter will filter every point of output image data. In this mode, every output point is calculated based on the 3 input points.

Input pixels:



Output pixels:





,where $Y_i = A_i * I_{k-1} + B_i * I_k + C_i * I_{k+1}$ and A, B, C are the scaling factors from interpolation table

Fig. 3.2.2 Scaling filter

3.2.2 Gain/Brightness Control

MTL002 provides Gain and Brightness control to adjust the contrast and brightness of output color by programming the gain and brightness coefficients. This adjustment is applied to RGB colors individually. Auto-white balance can be achieved by using this function.

3.2.3 Gamma Correction

Gamma Correction is used to compensate the non-linearity of LCD display panel. MTL002 contains an 8-bit Gamma table to fix this phenomenon.

3.2.4 Color Dithering

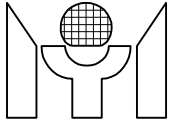
MTL002 supports true color (8 bits per color) or high color (6 bits per color) display. In the latter case, users can turn on dithering function to avoid artificial contour due to truncation. The dithering function works in two modes:

- ⌘ **Static dithering:** Dithering coefficient is fixed.
- ⌘ **Temporal dithering:** Dithering coefficient is time dependent.

3.3 Output Processor

General Description

Output processor provides the interface for both LCD panel and OSD controller. The output frame rate must be equal to the input frame rate and output display time must be equal to input display time since there is no frame buffer present.



3.3.1 Display Timing Generation

Because of no frame buffer, output displaying timing is locked by input timing and output frame rate is equal to input frame rate. Users must program output timing and lock position to make sure that line buffer will not overflow or underflow. MTL002 can automatically calculate Display Horizontal Total count to make the output timing calculation easier. MTL002 also provides line buffer overflow/underflow status for calibrating lock position.

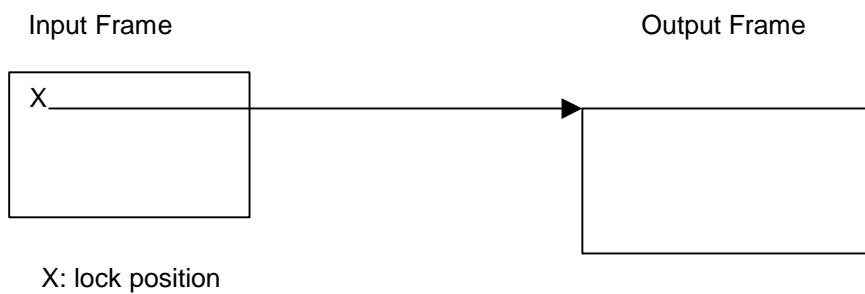


Fig. 3.2.2 Display Timing modes

3.3.2 OSD Overlay

MTL002 allows the integration of overlay data with the scaled output pixel stream. It provides a fully compatible OSD interface. Individual OSD clock, OSD HSYNC and OSD VSYNC are sent to external OSD device. MTL002 receives OSD Enable, OSD Red, OSD Green, OSD Blue, and OSD Intensity from external OSD device.

3.3.3 RGB Output Format

MTL002 output interface consists of two pixel ports, each containing Red, Green, and Blue color information with a resolution of 6/8 bits per color. These two ports are PORT1 and PORT2 respectively. The control signals for the output port are display horizontal sync signal (DHSYNC), display vertical sync signal (DVSYNC) and display data enable signal (DDEN).

All the signals mentioned above are synchronous to the output clock. The output timing relative to the active edge of the output clock is programmable.

There are two RGB output formats:

Ā Single Pixel Mode

Is designed to support TFT panels with single pixel input. Only PORT1 is active. The frequency of DCLK is equal to internal display clock.

Ā Dual Pixel Mode

Is designed to support TFT panels with dual pixel input. PORT1 and PORT2 are used. The first pixel is at PORT1, with the second at PORT2.

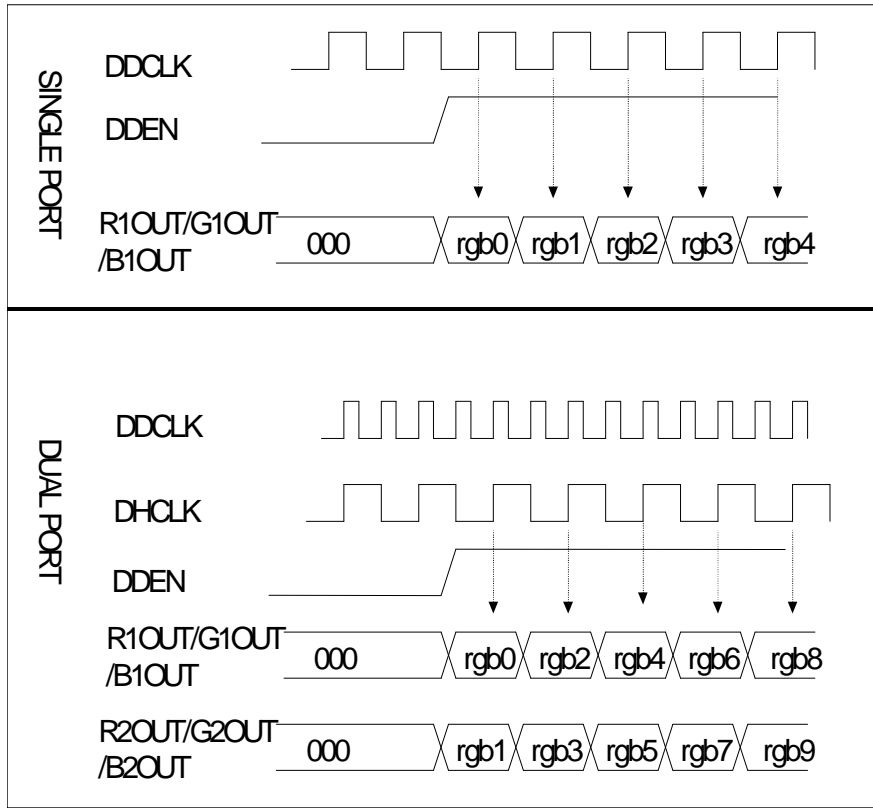
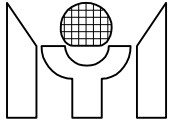
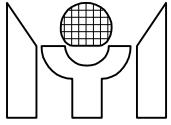


Fig. 3.2.3 Display Data Timing

3.5 Host Interface



General Description

The main function of Host Interface is to provide the interface between MTL002 and external CPU by 2-wire I²C Bus or 3-wire series Bus or 8-bit Direct Bus selected by the input pins BUSSEL[1:0]. It can generate all the I/O decoded control timing to control all the registers in MTL002. The other function is Screen Write, which allows users to clear frame buffer, and display output as well.

3.5.1 I²C Serial Bus

The I²C serial interface use 2 wires, SCK (clock) and SDA(data I/O). The SCK is used as the sampling clock and SDA is a bi-directional signal for data. The communication must be started with a valid START condition, concluded with STOP condition and acknowledged with ACK condition by receiver.

The I²C bus device address of MTL002 is 0111010x.

AD[0] SCK, serial bus clock.
AD[1] SDA, bi-directional serial bus data.

The START condition means a HIGH to LOW transition of SDA when SCK is high, the STOP condition means a LOW to HIGH transition of SDA when SCK is high. And data of SDA only changes when SCK is low. Ref. Fig.3.5.1.

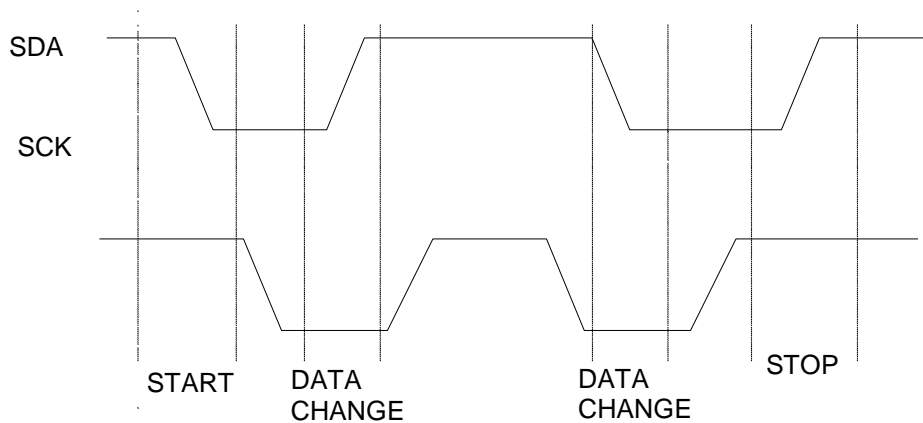


Fig. 3.5.1 START, STOP ,and DATA definition

The I²C interface supports Random Write, Sequential Write, Current Address Read, Random Read and Sequential Read operations.

\bar{A} Random Write

For Random Write operation, it contains the slave address with R/W bit set to 0 and the word address which is comprised of eight bits that provides the access to any one of the 256 bytes in the selected memory range. Upon receipt of the word address, MTL002 responds with an Acknowledge and waits for the next eight bits of data again, responding with an Acknowledge, and then the master generates a stop condition. Ref. Fig.3.5.2.

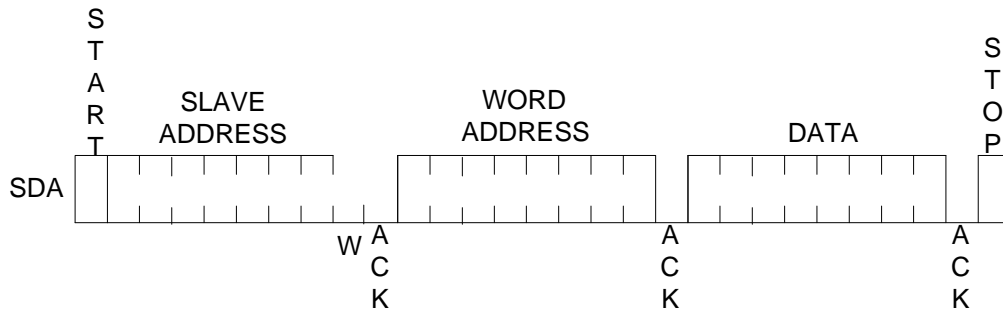
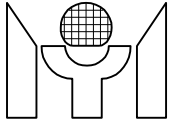


Fig. 3.5.2 Random Write

Sequential Write

The initial step of Sequential Write is the same as Random Write, after the receipt of each word data, MTL002 will respond with an Acknowledge and then internal address counter will increment by one for next data write. If the master stops writing data, it will generate stop condition. Ref. Fig. 3.5.3.

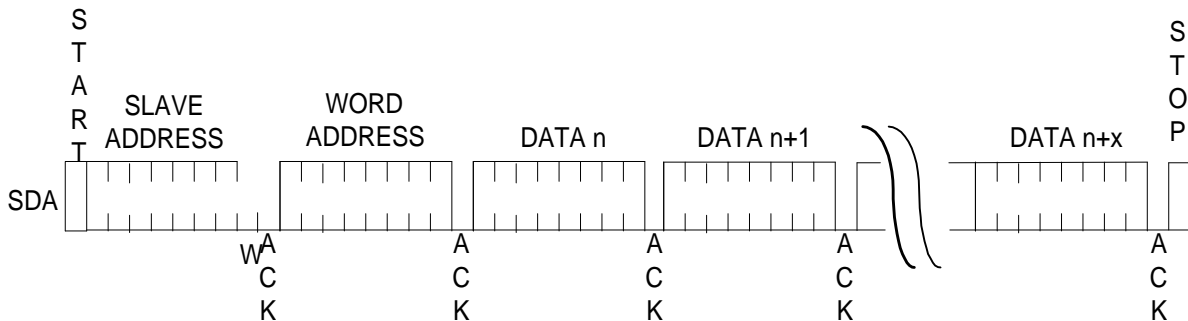


Fig. 3.5.3 Sequential Write

Current Address Read

MTL002 contains an address counter which maintains the last access address incremented by one. If the last access address is n, the read data should access from address n+1. Upon receipt of the slave address with R/W bit set to 1, MTL002 generates an Acknowledge and transmits the eight bits data. After receiving data the master will generate a stop condition instead of an Acknowledge. Ref. Fig. 3.5.4.

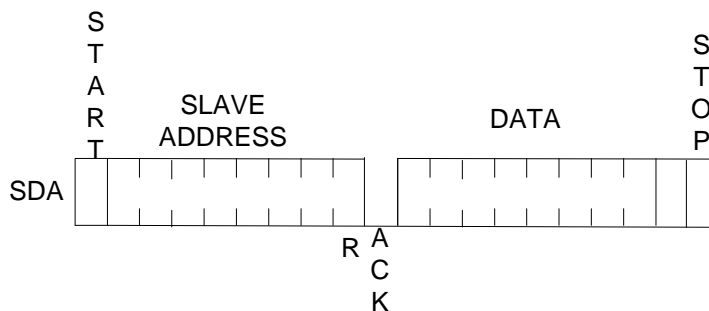


Fig. 3.5.4 Current Address Read



Random Read

The operation of Random Read allows access to any address. Before the reading data operation, it must issue a "dummy write" operation — the master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master generating a start condition again and slave address with R/W bit is set to 1. MTL002 then transmits the 8 bits of data. Upon the completion of receiving data, the master will generate a stop condition instead of an Acknowledge. Ref. Fig 3.5.5.

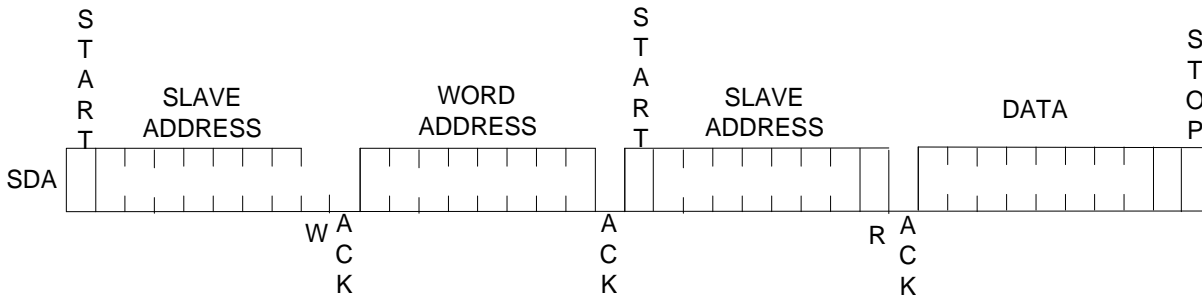


Fig. 3.5.5 Random Read

Sequential Read

The initial step can be as either Current Address Read or Random Read. The first read data is transmitted in the same manner as for other read methods. However, the master generates an Acknowledge indicating it requires more data to read. MTL002 continues to output data for each Acknowledge received. The output data is sequential and the internal address counter increments by one for next read data. Ref. Fig. 3.5.6.

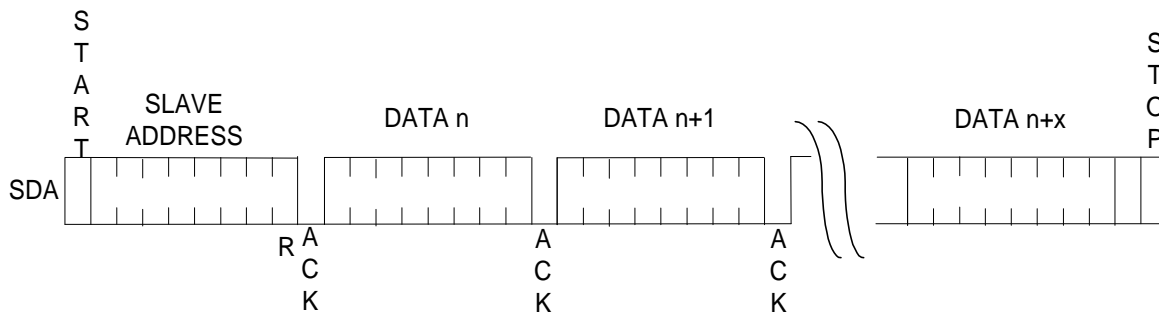


Fig. 3.5.6 Sequential Read

3.5.2 3-wire Serial Bus

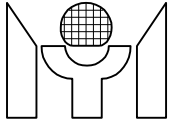
The 3-wire serial interface use 3 wires, SCK (clock) and SDA(data I) and SDAO(data O). The SCK is used as the sampling clock, SDA is an input signal for data, and SDAO is an output signal for data. The handshaking protocol is the same as for the 2-wire I2C serial bus.

- AD[0] SCK, serial bus clock.
AD[1] SDA, serial bus data in.
AD[2] SDAO, serial bus data out.

3.5.3 8-bit Direct Bus

The Direct Bus use AD[7:0], HWR#, HRD#, ALE, HCS# as the interface with host. ALE is used to latch read or write address from AD[7:0] and HRD#, HWR# to access data. Ref. Fig. 3.5.7.

AD[7:0] Address and data multiplex bus.



HRD# CPU read data strobe, Active Low.
HWR# CPU write data strobe, Active Low.
ALE ALE =1 latch read or write address, ALE=0 represents I/O data.
HCS# Enable signal for CPU access, Active Low.

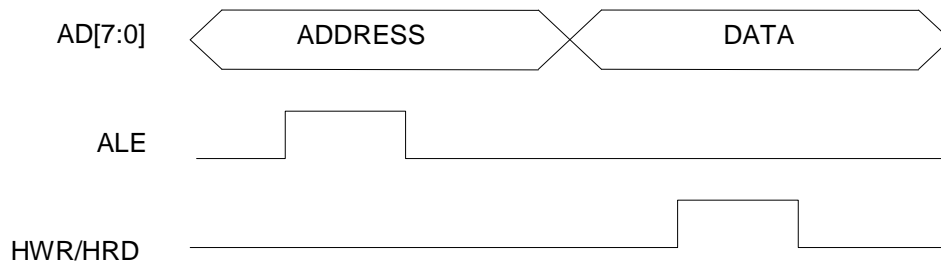


Fig. 3.5.7 Direct Bus Timing

3.5.4 Interrupt

MTL002 supports one interrupt output signal (IRQ) which can be programmed to provide SYNC related or function status related interrupts to the system. Upon receiving the interrupt request, Firmware needs to firstly check the interrupt event by reading the Interrupt Flag Control registers (Reg. E8h and E9h) to decide what events are happening. After the operation is finished, Firmware needs to clear interrupt status by writing the same registers Reg. E8h and E9h. Furthermore, by using the Interrupt Flag Enable registers (Reg. EAh and EBh), each interrupt event can be masked.

3.5.5 Bi-directional GPIO

MTL002 supports four General Purpose Input and Output (GPIO) pins GPIO[3:0] on chip. The GPIO[3:0] pins are bi-directional GPIO pins. There are two functions for GPIO[1:0] pins. One is to set them as bi-directional GPIO pins, and the other is to set them as Composite decoded VSYNC/HSYNC for A/D converters in VGA input path. The data and I/O direction of GPIO[3:0] pins are respectively controlled by Reg. F4h and F5h, and each bit in registers is respectively mapped to GPIO[3:0] one by one. The following description is the process to control GPIO[0] and GPIO[2] in detail, and the control processes of GPIO[1] and GPIO[3] are also the same as follows respectively.

̂ Bi-directional GPIO control process

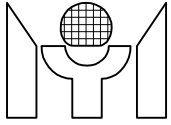
- Setting Reg. F5h/D2 = 0 or 1 to assign GPIO[2] as input or output.
- Writing data to Reg. F4h/D2 when GPIO[2] is assigned to output status, otherwise reading data from Reg. F4h/D2 when GPIO[2] is input.

̂ ADVS/ADHS Output control process

- Setting Reg. F5h/D0 = 1 to assign GPIO[0] as output.
- Setting Reg. F6h/D0 = 0 to select output source from Reg. F4h/D6 or setting it as 1 to make GPIO[0] pin to output ADHS which is HSYNC signal decoded from VGA input Composite signal by the MTL002.
- Writing data to F4h/D0 when GPIO[0] is assigned to output only GPIO pin, that is, F6h/D0 = 0 and F5h/D0 = 0. If F6h/D0 is set to 1, the GPIO[0] pin outputs ADHS for AD converters in VGA input path.

3.5.6 Update Register Contents

I/O write operation to some consecutive register set can have the “Double Buffer” effect by setting the Reg. C1h/D4. Written data is first stored in an intermediate bank of latches and then transferred to the active register set by setting Reg. C1h/D1-0.



3.6 On-Chip PLL

General Description

The MTL002 needs two clock sources to drive synchronous circuits on chip. These clocks are generated from the internal Phase Lock Loop (PLL) circuits with reference to the oscillator clock which is applied to pin XI and XO by an external quartz crystal at 14.31818 MHz. First one is the same as to the oscillator clock at frequency (14.31818 MHz) to detect and measure graphic vertical and horizontal SYNC Frequency, Polarity as well as Presence. The second is the display clock for display controller on chip and output signals to LCD panel.

3.6.1 Reference Clock

It is the counting basis of counter values in SYNC Processor such as VS and HS period count registers; that is, the read back values from these registers must multiply the period of this clock to estimate VS and HS frequency. Incorporating with polarity and frequency information of VS and HS, it can show the input graphic image mode and pixel clock frequency.

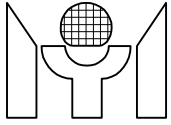
3.6.2 Display Clock

This clock is the synchronous clock for LCD panel. According to the LCD panel resolution of applications, the display clock range is from 50 MHz to 100 MHz by means of choosing a set of appropriate values for M, N as well as R. The formula used to calculate the desired frequency of display clock is as follows:

$$f_{mclk} = f_{osc} F (M+2)/(N+2) F 1/R$$

Where

f_{mclk}	: the desired display clock
f_{osc}	: oscillator clock with 14.31818 MHz
M	: post-divider ratio
N	: pre-divider ratio
R	: optional divider ratio



4. REGISTER DESCRIPTION

INPUT CONTROL REGISTERS

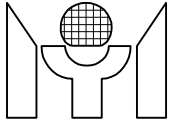
Address	Mode	Registers	Reset value
00h	R/W	Input Image Vertical Active Line Start - Low	20h
01h	R/W	Input Image Vertical Active Line Start - High	00h
02h	R/W	Input Image Vertical Active Lines - Low	E0h
03h	R/W	Input Image Vertical Active Lines - High	01h
04h	R/W	Input Image Horizontal Active Pixel Start - Low	8Bh
05h	R/W	Input Image Horizontal Active Pixel Start - High	00h
06h	R/W	Input Image Horizontal Active Pixels - Low	80h
07h	R/W	Input Image Horizontal Active Pixels - High	02h
10h	R/W	Input Image Control Register 0	00h
11h	R/W	Input Image Control Register 1	00h
12h	R/W	Input Image Control Register 2	00h
13h	R/W	Input Image Control Register 3	00h
14h	R/W	Input Image Control Register 4	00h
15h	R/W	Input Image Control Register 5	00h
16h	R/W	Input Image Control Register 6	00h
1Ah	R/W	Input Delay Control 2	00h
1Ch	R/W	HS1 Sample Window Forward Extend	00h
1Dh	R/W	HS1 Sample Window Backward Extend	00h
1Fh	RO	Input Image Status Register	-
20h	R/W	Input Image Back Porch Guard Band	00h
21h	R/W	Input Image Front Porch Guard Band	00h

FRAME SYNC REGISTERS

Address	Mode	Registers	Reset value
2Ch	R/W	Input Image Vertical Lock Position - Low	22h
2Dh	R/W	Input Image Vertical Lock Position - High	00h
2Eh	R/W	Input Image Horizontal Lock Position - Low	00h
2Fh	R/W	Input Image Horizontal Lock Position - High	00h

AUTO CALIBRATION REGISTERS

Address	Mode	Registers	Reset value
30h	R/W	Auto Calibration Control 0	80h
31h	R/W	Auto Calibration Control 1	00h
34h	RO	Auto Calibration RED Value - Byte 0	-
35h	RO	Auto Calibration RED Value - Byte 1	-
36h	RO	Auto Calibration RED Value - Byte 2	-
37h	RO	Auto Calibration RED Value - Byte 3	-
38h	RO	Auto Calibration GREEN Value - Byte 0	-
39h	RO	Auto Calibration GREEN Value - Byte 1	-
3Ah	RO	Auto Calibration GREEN Value - Byte 2	-
3Bh	RO	Auto Calibration GREEN Value - Byte 3	-
3Ch	RO	Auto Calibration BLUE Value - Byte 0	-
3Dh	RO	Auto Calibration BLUE Value - Byte 1	-
3Eh	RO	Auto Calibration BLUE Value - Byte 2	-
3Fh	RO	Auto Calibration BLUE Value - Byte 3	-
40h	R/W	Pixel Grab V Reference Position - Low	00h
41h	R/W	Pixel Grab V Reference Position - High	00h



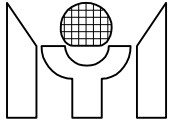
42h	R/W	Pixel Grab H Reference Position - Low	00h
43h	R/W	Pixel Grab H Reference Position - High	00h
44h	R/W	Histogram Reference Color - RED	00h
45h	R/W	Histogram Reference Color - GREEN	00h
46h	R/W	Histogram Reference Color - BLUE	00h

SYNC PROCESSOR REGISTERS

Address	Mode	Registers	Reset value
48h	R/W	SYNC Processor Control	00h
49h	R/W	Auto Position Control	00h
4Ah	R/W	Auto Position Reference Color - RED	00h
4Bh	R/W	Auto Position Reference Color - GREEN	00h
4Ch	R/W	Auto Position Reference Color - BLUE	00h
4Eh	R/W	Clamp Pulse Control 0	00h
4Fh	R/W	Clamp Pulse Control 1	00h
50h	RO	Input VS Period Count by REFCLK - Low	-
51h	RO	Input VS Period Count by REFCLK - High	-
52h	RO	Input V Back Porch Count by Input HS - Low	-
53h	RO	Input V Back Porch Count by Input HS - High	-
54h	RO	Input V Active Lines Count by Input HS - Low	-
55h	RO	Input V Active Lines Count by Input HS - High	-
56h	RO	Input V Total Lines Count by Input HS - Low	-
57h	RO	Input V Total Lines Count by Input HS - High	-
58h	RO	Input HS Period Count by REFCLK - Low	-
59h	RO	Input HS Period Count by REFCLK - High	-
5Ah	RO	Input H Back Porch Count by Input Pixel Clock - Low	-
5Bh	RO	Input H Back Porch Count by Input Pixel Clock - High	-
5Ch	RO	Input H Active Pixels Count by Input Pixel Clock - Low	-
5Dh	RO	Input H Active Pixels Count by Input Pixel Clock - High	-
5Eh	RO	Input H Total Pixels Count by Input Pixel Clock - Low	-
5Fh	RO	Input H Total Pixels Count by Input Pixel Clock - High	-

DISPLAY CONTROL REGISTERS

Address	Mode	Registers	Reset value
60h	R/W	Display Vertical Total - Low	48h
61h	R/W	Display Vertical Total - High	03h
62h	R/W	Display Vertical SYNC End- Low	05h
63h	R/W	Display Vertical SYNC End - High	00h
64h	R/W	Display Vertical Active Start - Low	22h
65h	R/W	Display Vertical Active Start - High	00h
66h	R/W	Display Vertical Active End - Low	22h
67h	R/W	Display Vertical Active End - High	03h
70h	R/W	Display Horizontal Total - Low	2Bh
71h	R/W	Display Horizontal Total - High	05h
72h	R/W	Display Horizontal SYNC End - Low	10h
73h	R/W	Display Horizontal SYNC End - High	00h
74h	R/W	Display Horizontal Active Start - Low	27h
75h	R/W	Display Horizontal Active Start - High	01h
76h	R/W	Display Horizontal Active End - Low	27h
77h	R/W	Display Horizontal Active End - High	05h



7Fh	R/W	NFB Timing Control	60h
88h	R/W	Output Image Control Register 0	01h
89h	R/W	Output Image Control Register 1	00h
8Ah	R/W	Output Image Control Register 2	00h
90h	R/W	Color Gain Control - RED	80h
91h	R/W	Color Gain Control - GREEN	80h
92h	R/W	Color Gain Control - BLUE	80h
93h	R/W	Brightness Control - RED	00h
94h	R/W	Brightness Control - GREEN	00h
95h	R/W	Brightness Control - BLUE	00h
9Fh	R/W	Gamma Table Data Port	-
A0h	R/W	OSD Control Register 0	08h
A1h	R/W	OSD Control Register 1	00h
A4h	R/W	Output Invert Control	00h
A5h	R/W	Output Tri-State Control	00h
A6h	R/W	Output Clocks Delay Adjustment	00h
A7h	R/W	Output Clocks Duty Cycle Adjustment	00h
A9h	R/W	Output Miscellaneous Control	00h
AAh	R/W	Output Vertical Line Number - Low	FFh
ABh	R/W	Output Vertical Line Number - High	02h
ACh	RO	Output Horizontal Total Pixel Number – Low	-
ADh	RO	Output Horizontal Total Pixel Number – High	-
A Eh	RO	Output Horizontal Total Residue Number – Low	-
AFh	RO	Output Horizontal Total Residue Number - High	-

ZOOM CONTROL REGISTERS

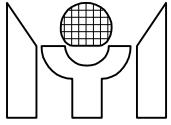
Address	Mode	Registers	Reset value
B0h	R/W	Zoom Control Register 0	66h
B1h	R/W	Zoom Control Register 1	00h
B4h	R/W	Zoom Vertical Scale Ratio - Low	E0h
B5h	R/W	Zoom Vertical Scale Ratio - High	9Fh
B6h	R/W	Zoom Horizontal Scale Ratio - Low	E8h
B7h	R/W	Zoom Horizontal Scale Ratio - High	9Fh
BFh	R/W	Interpolation Table Data Port	-

HOST CONTROL REGISTERS

Address	Mode	Registers	Reset value
C1h	R/W	Host Control Register 1	00h
CBh	RO	Host Access Mode Status	-

CLOCK CONTROL REGISTERS

Address	Mode	Registers	Reset value
E0h	R/W	Clock Control Register	00h
E1h	WO	Clock Synthesizer Value Load	-
E2h	R/W	Clock Synthesizer N Value	0Bh
E3h	R/W	Clock Synthesizer M Value	32h
E6h	R/W	Clock Synthesizer R Value	00h



INTERRUPT CONTROL REGISTERS

Address	Mode	Registers	Reset value
E8h	R/W	SYNC Interrupt Flag Control	00h
E9h	R/W	General Interrupt Flag Control	00h
EAh	R/W	SYNC Interrupt Enable	00h
EBh	R/W	General Interrupt Enable	00h
ECh	R/W	HS Frequency Change interrupt Compare	00h

MISCELLANEOUS REGISTERS

Address	Mode	Registers	Reset value
F1h	R/W	Power Management Control	00h
F4h	R/W	GPIO Control Register	00h
F5h	R/W	GPIO Direction Control	00h
F6h	R/W	GPIO Misc Control	00h

Input Image Vertical Active Line Start - Low (Address 00h) (R/W)

It defines the low byte of the start position of the Vertical Active Window.

D7-0 IV_ACT_START[7:0]

Input Image Vertical Active Line Start - High (Address 01h) (R/W)

It defines the high byte of the start position of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_START[10:8]

Input Image Vertical Active Lines - Low (Address 02h) (R/W)

It defines the low byte of the number of active lines of the Vertical Active Window.

D7-0 IV_ACT_LEN[7:0]

Input Image Vertical Active Lines - High (Address 03h) (R/W)

It defines the high byte of the number of active lines of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_LEN[10:8]

Input Image Horizontal Active Pixel Start - Low (Address 04h) (R/W)

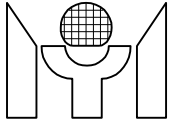
It defines the low byte of the start position of the Horizontal Active Window.

D7-0 IH_ACT_START[7:0]

Input Image Horizontal Active Pixel Start - High (Address 05h) (R/W)

It defines the high byte of the start position of the Horizontal Active Window.

D7-3 Reserved



D2-0 IH_ACT_START[10:8]

Input Image Horizontal Active Pixels - Low (Address 06h) (R/W)

It defines the low byte of the number of active pixels of the Horizontal Active Window.

D7-0 IH_ACT_WIDTH[7:0]

Input Image Horizontal Active Pixels - High (Address 07h) (R/W)

It defines the high byte of the number of active pixels of the Horizontal Active Window.

D7-3 Reserved

D2-0 IH_ACT_WIDTH[10:8]

Input Image Control Register 0 (Address 10h) (R/W)

- D7 Horizontal Sampling Point Reference
0: from Input HSYNC.
1: from Input HREF (only for Video Decoder).
- D6 Input YCBCR Format
0: 4-2-2
1: 4-1-1
- D5 Digital RGB 6 bit Mode
0: 8 bits
1: 6 bits
- D4 Digital RGB Mode Select
0: RGB Input from ADC
1: RGB Input from Panel Link
- D3 Input Image Format
0: RGB888
1: YCBCR
- D2 Reserved
- D1 Input Image Source
0: from Graphic source through ADC.
1: from Video source through Video Decoder like SAA7111A.
- D0 ADC Configuration
0: Double Pixel mode
1: Single Pixel mode

Input Image Control Register 1 (Address 11h) (R/W)

- D7 Reserved
- D6-5 Reserved
- D4 De-interlace mode Select
0: Spatial Filtering write mode



1: Toggle Field write mode

D3-1 Reserved

D0 Reserved

Input Image Control Register 2 (Address 12h) (R/W)

D7 Input ODD Field Invert
0: Normal
1: Invert

D6 External Input Interlace Select
0: Non-interlace
1: Interlace

D5 External Input VSYNC Polarity
0: Active Low
1: Active High

D4 External Input HSYNC Polarity
0: Active Low
1: Active High

D3 Input ODD Field Source
0: from Internal Detection
1: from External pin.

D2 Input Interlace Source
0: from Internal detection
1: from Register setting (D6)

D1 Input VSYNC Polarity Source
0: from Internal detection
1: from Register setting (D5)

D0 Input HSYNC Polarity Source
0: from Internal detection
1: from Register setting (D4)

Input Image Control Register 3 (Address 13h) (R/W)

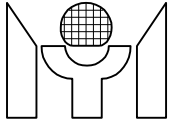
D7 Active Position Area for Auto Position in TMDS
0: from Internal Detection
1: from External Data Enable (TDIE)

D6-4 Reserved

D3 Data Enable in TMDS Select
0: from Pin TDIE
1: from Pin RAWHS

D2 Sync On Green Select
0: Select Normal HSYNC/ Composite Sync
1: Select Sync On Green

D1 Input Vertical Timing based on VSYNC



0: Leading Edge
1: Trailing Edge

D0 Input Horizontal Timing based on HSYNC
0: Leading Edge
1: Trailing Edge

Input Image Control Register 4 (Address 14h) (R/W)

D7 Input ODD Field Detection Point
0: at the start of VSYNC pulse.
1: at the end of VSYNC pulse.

D6 Input Image Port A, B Data and Clocks Swap
0: Normal
1: Swap

D5 Reserved

D4 Input Image CBCR Order Swap
0: Normal
1: Swap

D3 Input Image Port A, B V/H SYNC Swap
0: Normal
1: Swap

D2-0 Reserved

Input Image Control Register 5 (Address 15h) (R/W)

D7 Horizontal Pixel Valid Select
0: from Internal Programming
1: from External HREF/TDIE

D6-0 Reserved

Input Image Control Register 6 (Address 16h) (R/W)

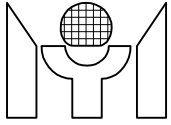
D7 Bit Order in Port B
0: Normal
1: Reverse

D6 Bit Order in Port A
0: Normal
1: Reverse

*D5 Flush Line Buffer Enable
0: Disable
1: Enable

D4 Input Video CREF Signal Invert Enable
0: Normal
1: Invert

D3 Video Clock Selection
0: LLC2



1: LLC & CREF

D2	ADC HS Polarity Invert when D1=1 0: Active Low 1: Active High
D1	Raw HS path Enable 0: Disable 1: Enable
D0	Input Image Port Selection in Single Pixel mode (For Video or Double Pixel mode, this bit has no function.) 0: Port A 1: Port B

Input Delay Control 2 (Address 1Ah) (R/W)

D7-4	Input VSYNC Delay Adjustment 1111: 15ns gate delay 1110: 14ns gate delay 1101: 13ns gate delay 1100: 12ns gate delay 1011: 3 IDCLKs delay 1010: 2 IDCLKs delay 1001: 1 IDCLK delay 1000: 8ns gate delay 0111: 7ns gate delay 0110: 6ns gate delay 0101: 5ns gate delay 0100: 4ns gate delay 0011: 3ns gate delay 0010: 2ns gate delay 0001: 1ns gate delay 0000: No delay
D3-0	Input HSYNC Delay Adjustment 16 steps to change, each of them is 1ns delay/step.

Input HS Pulse Width Forward Extend (Address 1Ch) (R/W)

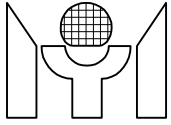
D7-0	Input HS Pulse Width Forward Extend by IDCLK HS1FWEXT[7:0]: Used when Interlace First/Second Field Detection.
------	--

Input HS Pulse Width Backward Extend (Address 1Dh) (R/W)

D7-0	Input HS Pulse Width Backward Extend by IDCLK HS1BWEXT[7:0]: Used when Interlace First/Second Field Detection.
------	---

Input Image Status Register (Address 1Fh) (RO)

D7	Display VSYNC Monitor Show Display VSYNC signal directly.
D6	Input VSYNC Monitor Show Input VSYNC signal directly.
D5	External Input Interlace Status



0: Non-interlace
1: Interlace

- D4 Extracted CVSYNC Present Status
 0: Not Present
 1: Present
- D3 External Input VSYNC Present Status
 0: Not Present
 1: Present
- D2 External Input HSYNC Present Status
 0: Not Present
 1: Present
- D1 External Input VSYNC Polarity Status
 0: Active Low
 1: Active High
- D0 External Input HSYNC Polarity Status
 0: Active Low
 1: Active High

Input Image Back Porch Guard Band (Address 20h) (R/W)

- D7-0 Input Image Back Porch Guard Band by IDCLK
 HBPGb[7:0]: Used in Auto Position detection to mask out unwanted data.

Input Image Front Porch Guard Band (Address 21h) (R/W)

- D7-0 Input Image Front Porch Guard Band by IDCLK
 HFPGB[7:0]: Used in Auto Position detection to mask out unwanted data.

Input Image Vertical Lock Position - Low (Address 2Ch) (R/W)

It defines the low byte of the number of input lines where Display image timing synchronizes the input image source.

- D7-0 IPV_LOCK_POS[7:0]

Input Image Vertical Lock Position - High (Address 2Dh) (R/W)

It defines the high byte of the number of input lines where Display image timing synchronizes the input image source.

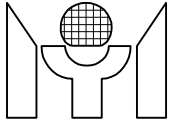
- D7-3 Reserved
- D2-0 IPV_LOCK_POS[10:8]

Input Image Horizontal Lock Position - Low (Address 2Eh) (R/W)

It defines the low byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

- D7-0 IPH_LOCK_POS[7:0]

Input Image Horizontal Lock Position - High (Address 2Fh) (R/W)



It defines the high byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

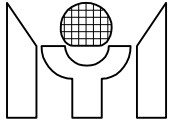
- D7-3 Reserved
- D2-0 IPH_LOCK_POS[10:8]

Auto Calibration Control 0 (Address 30h) (R/W)

- D7 Pixel Grab Ready Flag **(RO)**
0: Ready
1: Not Ready
- D6 Pixel Grab Update Enable
0: Stop updating
1: Continue updating
- D5 Threshold Select
Used in Histogram mode or MIN/MAX mode.
0: High bound / MAX
1: Low bound / MIN
- D4 Phase Calibration Method Select
0: MYSON proprietary method
1: Difference Value method
- D3-2 Auto Calibration Modes Select
The measured value is available one item at a time,
selected as shown:
00: Phase Calibration Mode
01: Histogram Mode
10: MIN/MAX Mode
11: Pixel Grab Mode
- D1 Auto Calibration Burst Mode Enable
(except Pixel Grab Mode)
0: Single Mode
1: Burst Mode
- D0 Auto Calibration Enable **(W)**
(except Pixel Grab Value)
0: Disable
1: Enable
Auto Calibration Ready Flag **(R)**
0: Ready
1: Not Ready

Auto Calibration Control 1 (Address 31h) (R/W)

- D7-3 Reserved
- D2-0 Mask LSBs of Input Image Select
It is used only for Phase Calibration to mask noise.
000: No Mask
001: Mask bit0
010: Mask bit0,1



011: Mask bit0,1,2
100: Mask bit0,1,2,3
101: Mask bit0,1,2,3,4
110: Mask bit0,1,2,3,4,5
111: Mask bit0,0,1,2,3,4,5,6

Auto Calibration RED Value - Byte 0 (Address 34h) (RO)

It states the byte 0 of the number of Phase Calibration RED value in one frame or the byte 0 of the number of Histogram Red value in one frame or the Pixel Grab RED value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[7:0]

Auto Calibration RED Value - Byte 1 (Address 35h) (RO)

It states the byte 1 of the number of Phase Calibration RED value in one frame or the byte 1 of the number of Histogram Red value in one frame or the Pixel Grab GREEN value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[15:8]

Auto Calibration RED Value - Byte 2 (Address 36h) (RO)

It states the byte 2 of the number of Phase Calibration RED value in one frame or the byte 2 of the number of Histogram Red value in one frame or the Pixel Grab BLUE value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[23:16]

Auto Calibration RED Value - Byte 3 (Address 37h) (RO)

It states the byte 3 of the number of Phase Calibration RED value in one frame.

D7-6 Reserved

D5-0 CALVAL_R[29:24]

Auto Calibration GREEN Value - Byte 0 (Address 38h) (RO)

It states the byte 0 of the number of Phase Calibration GREEN value in one frame or the byte 0 of the number of Histogram GREEN value in one frame or the Pixel Grab RED value in SECOND field of Interlace mode.

D7-0 CALVAL_G[7:0]

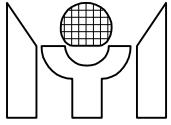
Auto Calibration GREEN Value - Byte 1 (Address 39h) (RO)

It states the byte 1 of the number of Phase Calibration GREEN value in one frame or the byte 1 of the number of Histogram GREEN value in one frame or the Pixel Grab GREEN value in SECOND field of Interlace mode.

D7-0 CALVAL_G[15:8]

Auto Calibration GREEN Value - Byte 2 (Address 3Ah) (RO)

It states the byte 2 of the number of Phase Calibration GREEN value in one frame



or the byte 2 of the number of Histogram GREEN value in one frame or the Pixel Grab BLUE value in SECOND field of Interlace mode.

D7-0 CALVAL_G[23:16]

Auto Calibration GREEN Value - Byte 3 (Address 3Bh) (RO)

It states the byte 3 of the number of Phase Calibration GREEN value in one frame.

D7-6 Reserved

D5-0 CALVAL_G[29:24]

Auto Calibration BLUE Value - Byte 0 (Address 3Ch) (RO)

It states the byte 0 of the number of Phase Calibration BLUE value in one frame or the byte 0 of the number of Histogram BLUE value in one frame or the MIN/MAX RED value in one frame.

D7-0 CALVAL_B[7:0]

Auto Calibration BLUE Value - Byte 1 (Address 3Dh) (RO)

It states the byte 1 of the number of Phase Calibration BLUE value in one frame or the byte 1 of the number of Histogram BLUE value in one frame or the MIN/MAX GREEN value in one frame.

D7-0 CALVAL_B[15:8]

Auto Calibration BLUE Value - Byte 2 (Address 3Eh) (RO)

It states the byte 2 of the number of Phase Calibration BLUE value in one frame or the byte 2 of the number of Histogram BLUE value in one frame or the MIN/MAX BLUE value in one frame.

D7-0 CALVAL_B[23:16]

Auto Calibration BLUE Value - Byte 3 (Address 3Fh) (RO)

It states the byte 3 of the number of Phase Calibration BLUE value in one frame.

D7-6 Reserved

D5-0 CALVAL_B[29:24]

Pixel Grab V Reference Position - Low (Address 40h) (R/W)

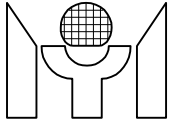
It states the low byte of Vertical Reference Position in Pixel Grab Mode.

D7-0 VGRAB_POS[7:0]

Pixel Grab V Reference Position - High (Address 41h) (R/W)

It states the high byte of Vertical Reference Position in Pixel Grab Mode.

D7-3 Reserved



D2-0 VGRAB_POS[10:8]

Pixel Grab H Reference Position - Low (Address 42h) (R/W)

It states the low byte of Horizontal Reference Position in Pixel Grab Mode.

D7-0 HGRAB_POS[7:0]

Pixel Grab H Reference Position - High (Address 43h) (R/W)

It states the high byte of Horizontal Reference Position in Pixel Grab Mode.

D7-3 Reserved

D2-0 HGRAB_POS[10:8]

Histogram Reference Color - RED (Address 44h) (R/W)

It states the Histogram Reference RED Color in Histogram Mode.

D7-0 HIST_R[7:0]

Histogram Reference Color - GREEN (Address 45h) (R/W)

It states the Histogram Reference GREEN Color in Histogram Mode.

D7-0 HIST_G[7:0]

Histogram Reference Color - BLUE (Address 46h) (R/W)

It states the Histogram Reference BLUE Color in Histogram Mode.

D7-0 HIST_B[7:0]

SYNC Processor Control (Address 48h) (R/W)

D7-2 Reserved

D1-0 SYNC Source
00: from H/V SYNC
01: from CVSYNC (Composite SYNC)
1x: Auto switch to CVSYNC when CVSYNC is present, but VSYNC not.

Auto Position Control (Address 49h) (R/W)

D7-2 Reserved

D1 Auto Position Burst Mode Enable
0: Single Mode
1: Burst Mode

D0 Auto Position Enable (**W**)
0: Disable
1: Enable
Auto Position Ready Flag (**R**)



0: Ready
1: Not Ready

Auto Position Reference Color - RED (Address 4Ah) (R/W)

It defines the red component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_RED[7:0]

Auto Position Reference Color - GREEN (Address 4Bh) (R/W)

It defines the green component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_GREEN[7:0]

Auto Position Reference Color - BLUE (Address 4Ch) (R/W)

It defines the blue component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_BLUE[7:0]

Clamp Pulse Control 0 (Address 4Eh) (R/W)

D7 Clamp Pulse Mask
0: Normal
1: Mask out Clamp Pulse

D6 Clamp Pulse Start Reference Edge
0: From Input HSYNC trailing edge.
1: From Input HSYNC leading edge.

D5 Clamp Pulse output Polarity
0: Active High
1: Active Low

D4-0 Clamp Pulse Start
Start of Clamp Pulse after the selected edge of Input HSYNC by Input DCLK.

Clamp Pulse Control 1 (Address 4Fh) (R/W)

D7-5 Reserved

D4-0 Clamp Pulse Width
To Adjust Clamp Pulse Width by Input DCLK.

Input VS Period Count by REFCLK - Low (Address 50h) (RO)

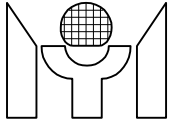
It states the low byte of the number of REFCLK of the Vertical Sync period measurement.

D7-0 VSPRD[7:0]

Input VS Period Count by REFCLK - High (Address 51h) (RO)

It states the high byte of the number of REFCLK of the Vertical Sync period measurement.

D7-4 Reserved



D3-0 VSPRD[11:8]

Input V Back Porch Count by Input HS - Low (Address 52h) (RO)

It states the low byte of the number of lines between the end of VSYNC and the active image.

D7-0 VBPW[7:0]

Input V Back Porch Count by Input HS - High (Address 53h) (RO)

It states the high byte of the number of lines between the end of VSYNC and the active image

D7-3 Reserved

D2-0 VBPW[10:8]

Input V Active Image Count by Input HS - Low (Address 54h) (RO)

It states the low byte of the number of the active image lines.

D7-0 VACTW[7:0]

Input V Active Image Count by Input HS - High (Address 55h) (RO)

It states the high byte of the number of the active image lines

D7-3 Reserved

D2-0 VACTW[10:8]

Input V Total Image Count by Input HS - Low (Address 56h) (RO)

It states the low byte of the number of the total image lines.

D7-0 VTOTW[7:0]

Input V Total Image Count by Input HS - High (Address 57h) (RO)

It states the high byte of the number of the total image lines.

D7-3 Reserved

D2-0 VTOTW[10:8]

Input HS Period Count by REFCLK - Low (Address 58h) (RO)

It states the low byte of the number of REFCLKs of the Horizontal Sync period measurement.

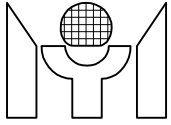
D7-0 HSPRD[7:0]

Input HS Period Count by REFCLK - High (Address 59h) (RO)

It states the high byte of the number of REFCLKs of the Horizontal Sync period measurement.

D7-5 Reserved

D4-0 HSPRD[12:8]



Input H Back Porch Count by Input Pixel Clock -Low (Address 5Ah) (RO)

It states the low byte of the number of pixels between the end of HSYNC and the active image.

D7-0 HBPW[7:0]

Input H Back Porch Count by Input Pixel Clock -High (Address 5Bh) (RO)

It states the high byte of the number of pixels between the end of HSYNC and the active image.

D7-3 Reserved

D2-0 HBPW[10:8]

Input H Active Image Count by Input Pixel Clock-Low(Address 5Ch) (RO)

It states the low byte of the number of the Horizontal active image pixels.

D7-0 HACTW[7:0]

Input H Active Image Count by Input Pixel Clock-High(Address 5Dh)(RO)

It states the high byte of the number of the Horizontal active image pixels.

D7-3 Reserved

D2-0 HACTW[10:8]

Input H Total Image Count by Input Pixel Clock- Low (Address 5Eh) (RO)

It states the low byte of the number of the Horizontal total image pixels.

D7-0 HTOTW[7:0]

Input H Total Image Count by Input Pixel Clock- High (Address 5Fh) (RO)

It states the high byte of the number of the Horizontal total image pixels.

D7-3 Reserved

D2-0 HTOTW[10:8]

Display Vertical Total - Low (Address 60h) (R/W)

It defines the low byte of the number of lines per display frame.

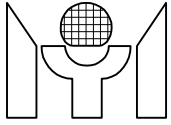
D7-0 DV_TOTAL[7:0]

Display Vertical Total - High (Address 61h) (R/W)

It defines the high byte of the number of lines per display frame.

D7-3 Reserved

D2-0 DV_TOTAL[10:8]



Display Vertical SYNC End - Low (Address 62h) (R/W)

It defines the low byte of Vertical SYNC end position in lines.

D7-0 DV_SYNC_END[7:0]

Display Vertical SYNC End - High (Address 63h) (R/W)

It defines the high byte of Vertical SYNC end position in lines.

D7-3 Reserved

D2-0 DV_SYNC_END[10:8]

Note: Display Vertical SYNC Start is always equal 0.

Display Vertical Active Start - Low (Address 64h) (R/W)

It defines the low byte of Vertical Active region start position in lines.

D7-0 DV_ACT_START[7:0]

Display Vertical Active Start - High (Address 65h) (R/W)

It defines the high byte of Vertical Active region start position in lines.

D7-3 Reserved

D2-0 DV_ACT_START[10:8]

Display Vertical Active End - Low (Address 66h) (R/W)

It defines the low byte of Vertical Active region end position in lines.

D7-0 DV_ACT_END[7:0]

Display Vertical Active End - High (Address 67h) (R/W)

It defines the high byte of Vertical Active region end position in lines.

D7-3 Reserved

D2-0 DV_ACT_END[10:8]

Display Horizontal Total - Low (Address 70h) (R/W)

It defines the low byte of the number of display clock cycles per display line.

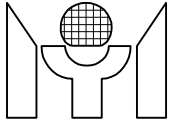
D7-0 DH_TOTAL[7:0]

Display Horizontal Total - High (Address 71h) (R/W)

It defines the high byte of the number of display clock cycles per display line.

D7-3 Reserved

D2-0 DH_TOTAL[10:8]



Display Horizontal SYNC End - Low (Address 72h) (R/W)

It defines the low byte of Horizontal SYNC end position in display clock cycles.

D7-0 DH_SYNC_END[7:0]

Display Horizontal SYNC End - High (Address 73h) (R/W)

It defines the high byte of Horizontal SYNC end position in display clock cycles.

D7-3 Reserved

D2-0 DH_SYNC_END[10:8]

Note: Display Horizontal SYNC Start is always equal 0.

Display Horizontal Active Start - Low (Address 74h) (R/W)

It defines the low byte of Horizontal Active region start position in display clock cycles.

D7-0 DH_ACT_START[7:0]

Display Horizontal Active Start - High (Address 75h) (R/W)

It defines the high byte of Horizontal Active region start position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_START[10:8]

Display Horizontal Active End - Low (Address 76h) (R/W)

It defines the low byte of Horizontal Active region end position in display clock cycles.

D7-0 DH_ACT_END[7:0]

Display Horizontal Active End - High (Address 77h) (R/W)

It defines the high byte of Horizontal Active region end position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_END[10:8]

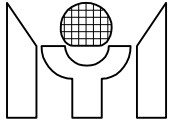
NFB Timing Control (Address 7Fh)

It defines the NFB timing setting.

D7-0 Free Running mode Select
 60h: Normal
 80h: Free Running

Output Image Control Register 0 (Address 88h) (R/W)

D7-5 Reserved



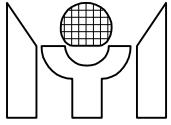
D4	OUTPUT port MSB / LSB Exchange 0: No Exchange 1: Exchange
D3	Reserved
D2	Output Pixel 18 bit RGB Mode Select 0: 24 bit RGB 1: 18 bit RGB
D1	Output Dual Pixel Data Exchange 0: Normal 1: Exchange
D0	Output Dual Pixel Select 0: Dual Pixel 1: Single Pixel

Output Image Control Register 1 (Address 89h) (R/W)

D7-6	Reserved
D5	RGB Brightness Control Enable 0: Disable 1: Enable
D4	RGB Gain Control Enable 0: Disable 1: Enable
D3-2	Reserved
D1	Border Window Function 0: OFF 1: ON
D0	Output Blank Screen 0: Normal 1: Output Pixel masked as BLACK color

Output Image Control Register 2 (Address 8Ah) (R/W)

D7	Reserved
D6	Temporal Dithering Enable 0: Static Dithering 1: Temporal Dithering
D5	Reserved
D4	Dithering Enable 0: Disable 1: Enable
D3-2	Reserved
D1	Gamma Table R/W Access Enable



0: Disable
1: Enable

D0 Gamma Correction Function
0: OFF
1: ON

Color Gain Control - RED (Address 90h) (R/W)

It can be used to adjust the gain of RED component of the Display Image.

D7-0 RGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - GREEN (Address 91h) (R/W)

It can be used to adjust the gain of GREEN component of the Display Image.

D7-0 GGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - BLUE (Address 92h) (R/W)

It can be used to adjust the gain of BLUE component of the Display Image.

D7-0 BGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Brightness Control - RED (Address 93h) (R/W)

It can be used to adjust the brightness of RED component of the Display Image.

D7-0 RBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Color Brightness Control - GREEN (Address 94h) (R/W)

It can be used to adjust the brightness of GREEN component of the Display Image.

D7-0 GBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Color Brightness Control - BLUE (Address 95h) (R/W)

It can be used to adjust the brightness of BLUE component of the Display Image.

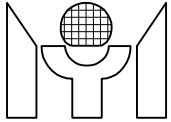
D7-0 BBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Border Window Color - RED (Address 96h) (R/W)

When the Display Image is not expanded to full screen, it can be specified as the RED component of the border color.

D7-0 BCR[7:0]

Border Window Color - GREEN (Address 97h) (R/W)



When the Display Image is not expanded to full screen, it can be specified as the GREEN component of the border color.

D7-0 BCG[7:0]

Border Window Color - BLUE (Address 98h) (R/W)

When the Display Image is not expanded to full screen, it can be specified as the BLUE component of the border color.

D7-0 BCB[7:0]

Gamma Table Data Port (Address 9Fh) (R/W)

Since the Gamma Table is downloadable, this data port is the entry address.

D7-0 GAMMA_PORT[7:0]

OSD Control Register 0 (Address A0h) (R/W)

- D7 OSD Output Clock Select
0: from Internal Display Dot Clock
1: from Internal Display Dot Clock x 2
- D6-4 Reserved
- D3 OSD Function
0: OFF
1: ON
- D2 OSD Intensity Enable (For MOTOROLA)
0: Disable
1: Enable
- D1-0 OSD TYPE Select
00: OSDRGB = {R0000000, G0000000, B0000000}
01: OSDRGB = {RR000000, GG000000, BB000000}
10: OSDRGB = {RRRR0000, GGGG0000, BBBB0000}
11: OSDRGB = {RRRRRRRR, GGGGGGGG, BBBBBBBB}
R = OSDR, G = OSDG, B = OSDB

OSD Control Register 1 (Address A1h) (R/W)

- D7 OSD Output HS Invert
0: Normal
1: Invert.
- D6 OSD Output DCLK Invert
0: Normal
1: Invert.
- D5-4 OSD Output HS Delay
4 steps to change, each of them is 1ns delay/step.
- D3 OSD Input Data Sample Clock Invert
0: Normal.



1: Invert.

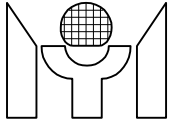
D2-0 OSD Input Data Sample Clock Delay
8 steps to change, each of them is 1ns delay/step.

Output Invert Control (Address A4h) (R/W)

D7	Reserved
D6	RGB Data Invert Enable 0: Disable 1: Enable
D5	Display DHCLK Invert 0: Normal 1: Invert
D4	Display DCLK Invert 0: Normal 1: Invert
D3	Reserved
D2	Display Data Enable (DDEN) Invert 0: Normal 1: Invert
D1	Display VSYNC Invert 0: Normal 1: Invert
D0	Display HSYNC Invert 0: Normal 1: Invert

Output Tri_state Control (Address A5h) (R/W)

D7	Display Data R2OUT, G2OUT, B2OUT Output Disable 0: Normal 1: Tri_stated
D6	Display Data R1OUT, G1OUT, B1OUT Output Disable 0: Normal 1: Tri_stated
D5	Display DHCLK Output Disable 0: Normal 1: Tri_stated
D4	Display DCLK Output Disable 0: Normal 1: Tri_stated
D3	OSD OCLK / OVSYNC / OHSYNC Output Disable 0: Normal 1: Tri_stated



D2	Display Data Enable (DDEN) Output Disable 0: Normal 1: Tri_stated
D1	Display VSYNC Output Disable 0: Normal 1: Tri_stated
D0	Display HSYNC Output Disable 0: Normal 1: Tri_stated

Output Clocks Delay Adjustment (Address A6h) (R/W)

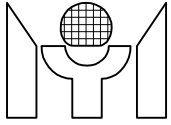
D7-4	Display DHCLK delay adjustment 16 steps to adjust, Typical 1ns delay/step
D3-0	Display DCLK delay adjustment 16 steps to adjust, Typical 1ns delay/step

Output Clocks Duty Cycle Adjustment (Address A7h) (R/W)

D7	Display DHCLK duty cycle Increase/Decrease 0: Decrease 1: Increase
D6-4	Display DHCLK duty cycle adjustment 8 steps to adjust, Typical 0.5ns delay/step
D3	Display DCLK duty cycle Increase/Decrease 0: Decrease 1: Increase
D2-0	Display DCLK duty cycle adjustment 8 steps to adjust, Typical 0.5ns delay/step

Output Miscellaneous Control (Address A9h) (R/W)

D7	Second field Line Buffer Overflow status for Interlace input (RO) 0: Not Overflow 1: Overflow
D6	Second field Line Buffer Underflow status for Interlace input (RO) 0: Not Underflow 1: Underflow
D5	First field Line Buffer Overflow status for Interlace input or Line buffer Overflow status for Non-interlace input (RO) 0: Not Overflow 1: Overflow
D4	First field Line Buffer Underflow status for Interlace input or Line Buffer Overflow status for Non-interlace input (RO) 0: Not Underflow 1: Underflow
D3	Auto Output Horizontal Total Calculation Start (W)



0: Disable
1: Enable
Auto Output Horizontal Total Calculation Ready Flag (R)
0: Ready
1: Not Ready

D2-0 Reserved

Output Vertical Active Line Number - Low (Address AAh) (R/W)

It defines the low byte of Output Vertical Active Line Number only used for getting the values of Reg. ACh and ADh.

D7-0 OVDE[7:0]

Output Vertical Active Line Number - High (Address ABh) (R/W)

It defines the high byte of Output Vertical Active Line Number only used for getting the values of Reg. ACh and ADh.

D1-0 OVDE[9:8]

Output Horizontal Total Pixel Number - Low (Address ACh) (RO)

It states the low byte of Output Horizontal Total Pixel Number.

D7-0 OHTOT[7:0]

Output Horizontal Total Pixel Number - High (Address ADh) (RO)

It states the high byte of Output Horizontal Total Pixel Number.

D2-0 OHTOT[10:8]

Output Horizontal Total Residue Number - Low (Address AEh) (RO)

It states the low byte of Output Horizontal Total Pixel Residue Number.

D7-0 OHTOT_RES[7:0]

Output Horizontal Total Residue Number - High (Address AFh) (RO)

It states the high byte of Output Horizontal Total Pixel Residue Number.

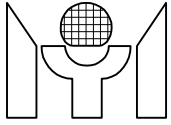
D1-0 OHTOT_RES[9:8]

Zoom Control Register 0 (Address B0h) (R/W)

D7 Reserved

D6-4 Vertical Scale Select
0XX: PASS mode
10X: DUPLICATE mode
110: BILINEAR mode
111: INTERPOLATION TABLE mode

D3 Reserved



D2-0 Horizontal Scale Select
0xx: PASS mode
10x: DUPLICATE mode
110: BILINEAR mode
111: INTERPOLATION TABLE mode

Zoom Control Register 1 (Address B1h) (R/W)

D7-1 Reserved

*D3 Horizontal Zoom Factor mode
0: Uniform Scale mode
1: Extension Boundary Scale mode

*D2 Vertical Zoom Factor mode
0: Uniform Scale mode
1: Extension Boundary Scale mode

D0 Interpolation Table R/W Access Enable
0: Disable
1: Enable

Zoom Vertical Scale Ratio – Low (Address B4h) (R/W)

It defines the low byte of vertical scale ratio value for scale up.

D7-0 ZVSF[7:0]

Zoom Vertical Scale Ratio - High (Address B5h) (R/W)

It defines the low byte of vertical scale ratio value for scale up.

D7-0 ZVSF[15:8]

ZVSF = $\text{CEIL}[(\text{input_height} - 1) / (\text{output_height} - 1) * 2^{16}]$ for Uniform Scale mode
ZVSF = $\text{CEIL}[(\text{input_height} / \text{output_height}) * 2^{16}]$ for Extension Boundary Scale mode

Zoom Horizontal Scale Ratio - Low (Address B6h) (R/W)

It defines the low byte of horizontal scale ratio value for scale up.

D7-0 ZHSF[7:0]

Zoom Horizontal Scale Ratio - High (Address B7h) (R/W)

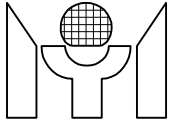
It defines the high byte of horizontal scale ratio value for scale up.

D7-0 ZHSF[15:8]

ZHSF = $\text{CEIL}[(\text{input_width} - 1) / (\text{output_width} - 1) * 2^{16}]$ for Uniform Scale mode
ZHSF = $\text{CEIL}[(\text{input_width} / \text{output_width}) * 2^{16}]$ for Extension Boundary Scale mode

Interpolation Table Data Port (Address BFh) (R/W)

It defines the entry address of the Interpolation table data port.



D7-0 TFPORT[7:0]

Host Control Register 1 (Address C1h) (R/W)

D7	Reserved
D6	I2C Bus Address No Increment 0: Normal 1: No Increment
D5	Double Buffer load Select 0: Immediately 1: Delay to Display VSYNC
D4	Registers Double Buffer function Enable 0: Disable 1: Enable
D3-2	Reserved
D1	Display Registers Double Buffer Load (WO)
D0	Input Registers Double Buffer Load (WO)

Host Access Mode Status (Address CBh) (RO)

D7-2	Reserved
D1-0	Host Access Mode 0x: 3-wire Serial mode 10: 2-wire Serial mode (IIC) 11: 8-bit Parallel mode

Clock Synthesizer Control Register (Address E0h) (R/W)

D7-0	Display Clock Selection 40h: Internal Display Clock (PLL) Note: Reg. F1h/D3 must be 1. 25h: External Display Clock 1 A5h: External Display Clock 2
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Clock Synthesizer Value Load (Address E1h) (WO)

D7-1	Reserved
D0	Display Clock Synthesizer Value Load (WO)

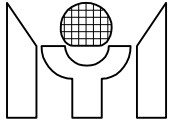
Display Clock Synthesizer N Value (Address E2h) (R/W)

D7-0	Display Clock Synthesizer N value
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Display Clock Synthesizer M Value (Address E3h) (R/W)

D7-0	Display Clock Synthesizer M value
------	-----------------------------------

Clock Synthesizer R Value (Address E6h) (R/W)



D7 Reserved

D6-4 REFCLK Clock Divider value
000: No divided
001: Divided by 2
010: Divided by 4
011: Divided by 8
100: Divided by 3
101: Divided by 6
110: Divided by 12
111: Divided by 24

D3-2 Reserved

D1-0 Display Clock Synthesizer R value
00: No divided
01: Divided by 2
1x: Divided by 4

SYNC Interrupt Flag Control (Address E8h) (R)

It contains the status of SYNC Interrupts.

D7 Display VSYNC Pulse Interrupt Status
0: No Display VSYNC pulse detected
1: Any Display VSYNC pulse detected

D6 Input VSYNC Pulse Interrupt Status
0: No Input VSYNC pulse detected
1: Any Input VSYNC pulse detected

D5 VSYNC Presence Change Status
0: No Change
1: Change

D4 HSYNC Presence Change Status
0: No Change
1: Change

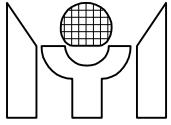
D3 VSYNC Polarity Change Status
0: No Change
1: Change

D2 HSYNC Polarity Change Status
0: No Change
1: Change

D1 VSYNC Frequency Change Status
0: No Change
1: Change

D0 HSYNC Frequency Change Status
0: No Change
1: Change

SYNC Interrupt Flag Control (Address E8h) (W)



It is used to clear the corresponding SYNC interrupt signal when Software finishes serving the interrupt service routine.

D7	Clear Display VSYNC Pulse Interrupt Enable 0: Disable 1: Enable
D6	Clear Input VSYNC Pulse Interrupt Enable 0: Disable 1: Enable
D5	Clear VSYNC Presence Change Interrupt Enable 0: Disable 1: Enable
D4	Clear HSYNC Presence Change Interrupt Enable 0: Disable 1: Enable
D3	Clear VSYNC Polarity Change Interrupt Enable 0: Disable 1: Enable
D2	Clear HSYNC Polarity Change Interrupt Enable 0: Disable 1: Enable
D1	Clear VSYNC Frequency Change Interrupt Enable 0: Disable 1: Enable
D0	Clear HSYNC Frequency Change Interrupt Enable 0: Disable 1: Enable

General Interrupt Flag Control (Address E9h) (R)

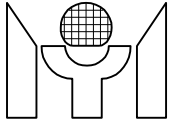
It contains the status of General Interrupts.

D7-3	Reserved
D2	Reserved
D1	Auto Position Finish Status (valid for Single mode only) 0: Not Finish 1: Finish
D0	Auto Calibration Finish Status (valid for Single mode only) 0: Not Finish 1: Finish

General Interrupt Flag Control (Address E9h) (W)

It is used to clear the corresponding general interrupt signal when Software finishes serving the interrupt service routine.

D7-3	Reserved
------	----------



D2 Reserved

D1 Clear Auto Position Finish Interrupt Enable
0: Disable
1: Enable

D0 Clear Auto Calibration Finish Interrupt Enable
0: Disable
1: Enable

SYNC Interrupt Flag Enable (Address EAh) (R/W)

It is used to enable SYNC Interrupt function.

D7 Display VSYNC Pulse Interrupt Enable
0: Disable
1: Enable

D6 Input VSYNC Pulse Interrupt Enable
0: Disable
1: Enable

D5 VSYNC Presence Change Interrupt Enable
0: Disable
1: Enable

D4 HSYNC Presence Change Interrupt Enable
0: Disable
1: Enable

D3 VSYNC Polarity Change Interrupt Enable
0: Disable
1: Enable

D2 HSYNC Polarity Change Interrupt Enable
0: Disable
1: Enable

D1 VSYNC Frequency Change Interrupt Enable
0: Disable
1: Enable

D0 HSYNC Frequency Change Interrupt Enable
0: Disable
1: Enable

General Interrupt Flag Enable (Address EBh) (R/W)

It is used to enable General Interrupt functions.

D7-3 Reserved

D2 Reserved

D1 Auto Position Finish Interrupt Enable
0: Disable



1: Enable

D0 Auto Calibration Finish Interrupt Enable
0: Disable
1: Enable

HS Frequency Change Interrupt Compare (Address ECh) (R/W)

It is used to control Interrupt generation by comparing the frequency change value when Input HS Frequency Changes.

D7-0 HSCMPREG[7:0]

Power Management Control (Address F1h) (R/W)

D7 Reserved

D6 Power Down Gamma & Interpolation Table
0: Normal
1: Power Down

D5 Reserved

D4 Power Down Line Buffers
0: Normal
1: Power Down

D3 Power Down Oscillator PAD
0: Power Down
1: Normal

D2 Reserved

D1 Power Down all the clocks except REFCLK
0: Normal
1: Power Down

D0 Software Reset Enable
0: Disable
1: Enable

GPIO Control Register (Address F4h) (R/W)

It controls the data of the GPIO pins.

D7-4 Reserved

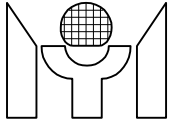
D3-0 GPIO[3:0]

GPIO Direction Control (Address F5h) (R/W)

It controls the In/Out direction of the GPIO pins, where “0” means Input, and “1” means Output.

D7-4 Reserved

D3-0 GPIO[3:0] In/Out Select

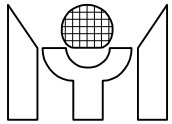


0: Input
1: Output

GPIO Misc Control (Address F6h) (R/W)

It defines the GPIO pins miscellaneous control.

D7-1	Reserved
D0	GPIO[1:0] Output Pins Source 0: from Reg. F4h GPIO[1:0] 1: from ADVS/ADHS



5. ELECTRICAL CHARACTERISTICS

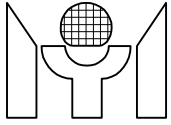
5.1 DC CHARACTERISTICS

Table 5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Vcc	Operation Voltage	3.0	3.3	3.6	V
Tamb	Operating Ambient Temperature	0		70	°C
Tstg	Storage Temperature	-55		150	°C

Table 5.2 DC Electrical Characteristics for 3.3 V Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.0			V
Vt-	Input Schmitt Trigger Low Voltage at pins SDA and SCK			1.0		
Vt+	Input Schmitt Trigger High Voltage at pins SDA and SCK			1.7		
VOL	Output Low Voltage				0.4	V
VOH	Output High Voltage		2.4			V
RI	Input Pull-up/Down Resistance	VIL = 0v or VIH = VCC		75		Kohm
ILI	Input Leakage Current		-10		10	uA
ILO	Output Leakage Current		-20		20	uA



5.2 AC CHARACTERISTICS

À Input Interface Timing

Figure 5.2.1 Input Interface Timing

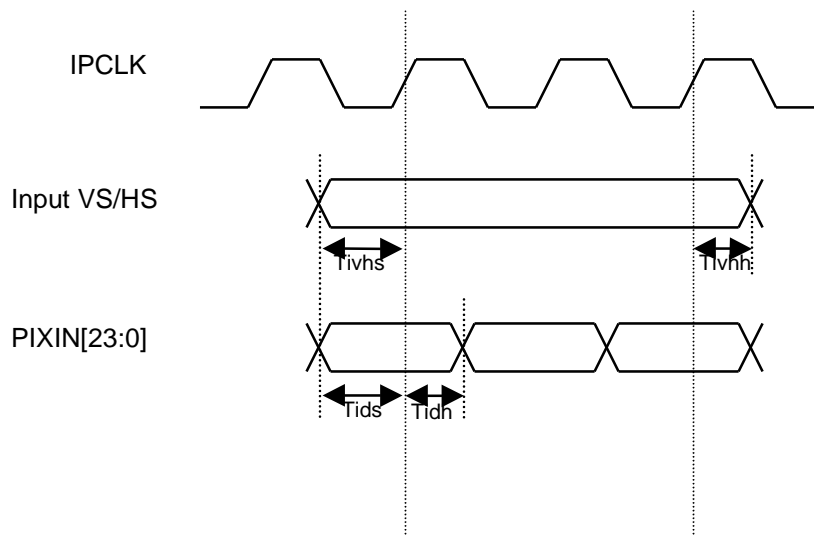
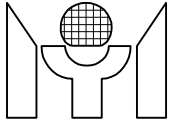


Table 5.2.1 Input Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tids	Input Image Signal Setup Time for IPCLK	2		ns
Tidh	Input Image Signal Hold Time for IPCLK	3		ns
Tivhs	Input VSYNC/HSYNC Setup Time for IPCLK	2		ns
Tivhh	Input VSYNC/HSYNC Hold Time for IPCLK	3		ns



Ā **Output Interface Timing**

Figure 5.2.2 Output Interface Timing

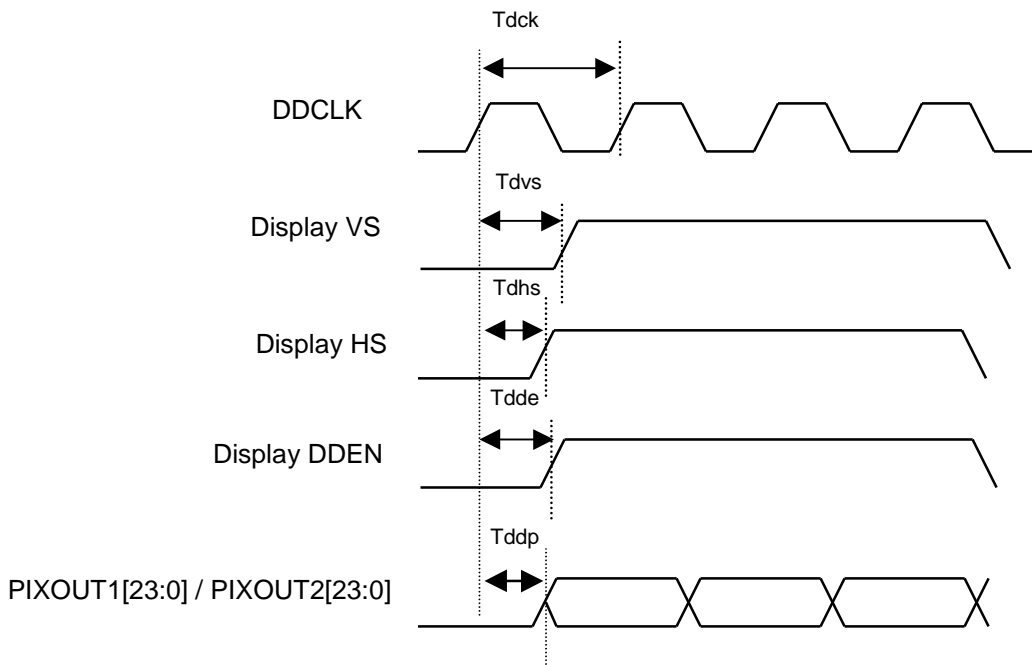
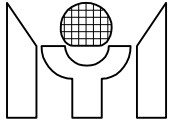


Table 5.2.2 Output Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tdck	Display Clock DDCLK Frequency	10		ns
Tdvs	Display VSYNC Output Delay to DDCLK	2		ns
Tdhs	Display HSYNC Output Delay to DDCLK	0.5		ns
Tdde	Display DDEN Output Delay to DDCLK	1		ns
Tddp	Display Data Output Delay to DDCLK	1.5		ns

Note: DDCLK phase can be adjusted relative to data and control outputs using the DDCLK_INV (Reg. A4h/D5-4) and DDCLK_DELAY[2:0] (Reg. A6h/D7-0) programming controls.



Ā **OSD Interface Timing**

Figure 5.2.3 OSD Interface Timing

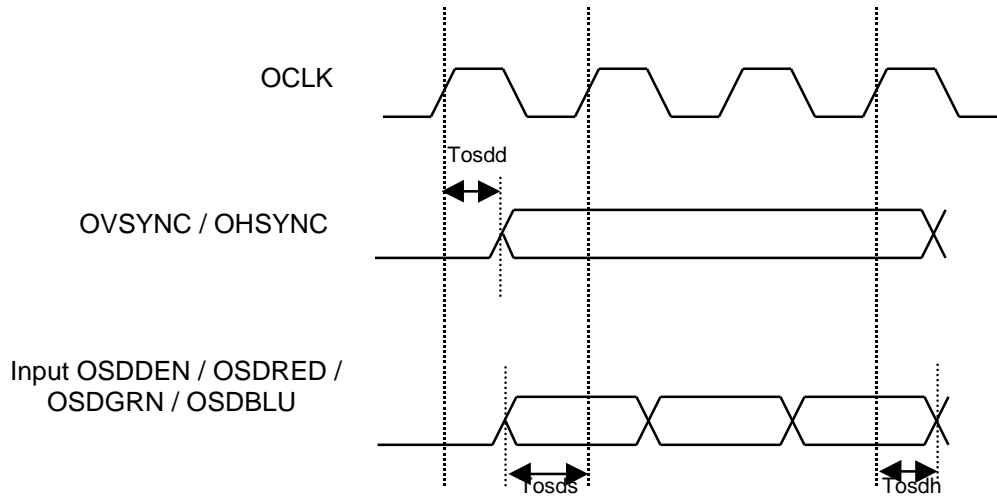
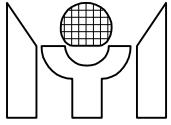


Table 5.2.3 OSD Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tosdd	OSD VS / HS Output Delay to OCLK	2		ns
Tosds	OSD Signal Input Setup Time for OCLK	5.5		ns
Tosdh	OSD Signal Input Hold Time for OCLK	0		ns

Note: OCLK phase can be adjusted using OCLK_INV (Reg. A1h/D3) programming control and OHSYNC phase can be adjusted using OHSYNC_DELAY[1:0] (Reg. A1h/D5-4) programming control.



Ā I2C Host Interface Timing

Figure 5.2.4 I2C Host Interface Timing

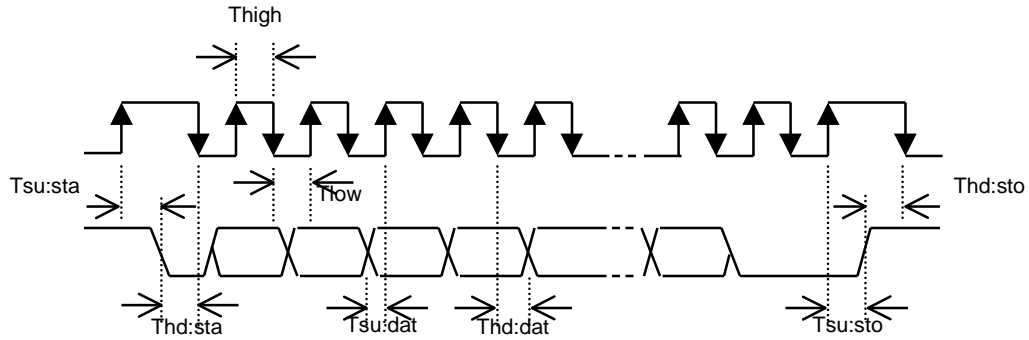
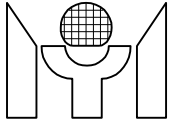


Table 5.2.4 I2C Host Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{high}	Clock High Period	500		ns
T_{low}	Clock Low Period	500		ns
$T_{su:dat}$	Data in Setup Time	200		ns
$T_{hd:dat}$	Data in Hold Time	100		ns
$T_{su:sta}$	Start condition Setup Time	500		ns
$T_{hd:sta}$	Start condition Hold Time	500		ns
$T_{su:sto}$	Stop condition Setup Time	500		ns
$T_{hd:sto}$	Stop condition Hold Time	500		ns



8-bit Direct Host Interface Timing

Figure 5.2.5 8-bit Direct Host Interface Timing

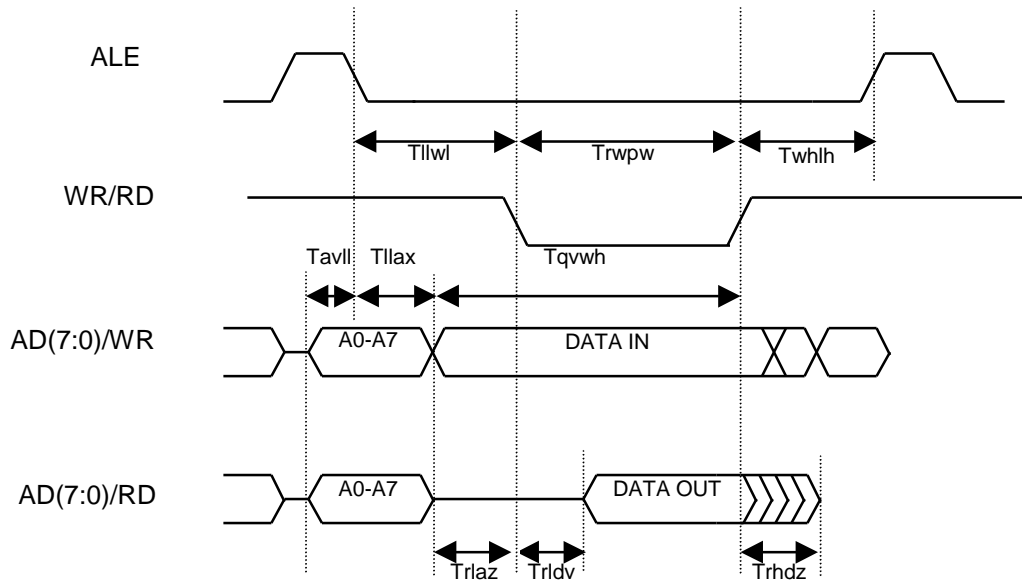


Table 5.2.5 8-bit Direct Host Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tavll	Address Valid to ALE Low	3		ns
Tllax	Address Hold After ALE Low	5		ns
Trwpw	WR/RD Pulse Width	35		ns
Tllwl	ALE Low to WR/RD Low	5		ns
Tqvwh	Data Valid to WR High	3		ns
Twhqx	Data Hold After WR	10		ns
Twhlh	WR/RD High to ALE High – Register IO R/W	0		ns
Trlaz	RD Low to Address Float	-5		ns
Trldv	RD Low to Valid Data In		30	ns
Trhdz	Data Float after RD High	0	15	ns

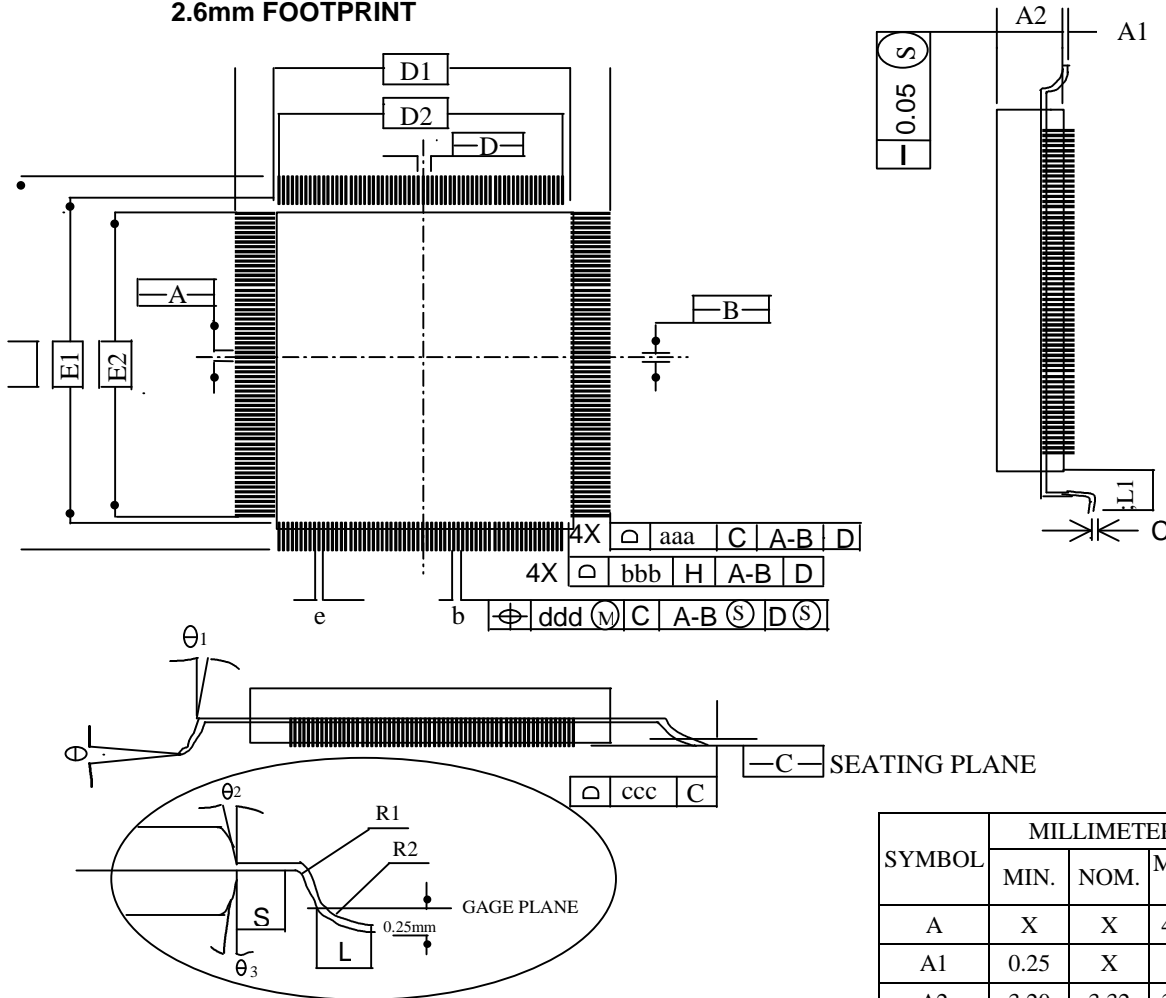


6. PACKAGE DIMENSION

120/128/132/144/160/184/208/256L OFP

28 X 28 X 3.32 mm

2.6mm FOOTPRINT



MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
0.17	0.20	0.27	0.007	0.008	0.011
0.50 BSC.			0.020 BSC.		
25.50			1.004		
25.50			1.004		
TOLERANCES OF FORM AND POSITION					
0.20			0.008		
0.20			0.008		
X	0.08	X	X	0.003	X
X	0.08	X	X	0.003	X

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	X	X	4.10	X	X	0.161
A1	0.25	X	X	0.010	X	X
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	30.60 BSC			1.205 BSC		
D1	28.00 BSC			1.102 BSC		
E	30.60 BSC			1.205 BSC		
E1	28.00 BSC			1.102 BSC		
R2	0.08	X	0.25	0.003	X	0.010
R1	0.08	X	X	0.003	X	X
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	X	X	0°	X	X
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
C	0.09	0.15	0.20	0.004	0.005	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.30			0.051 REF		
S	0.20	X	X	0.008	X	X

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.