



# PRELIMINARY MX23L12811

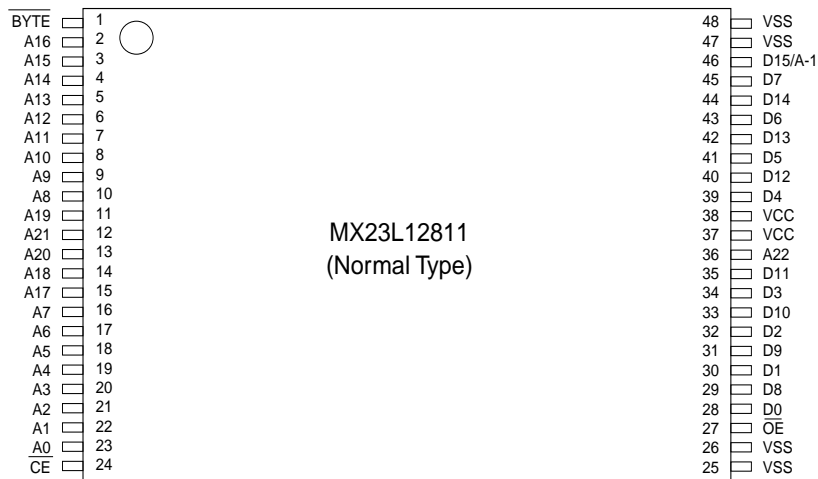
## NEW 128M-BIT (16M x 8/8M x 16) MASK ROM WITH PAGE MODE (TSOP PACKAGE)

### FEATURES

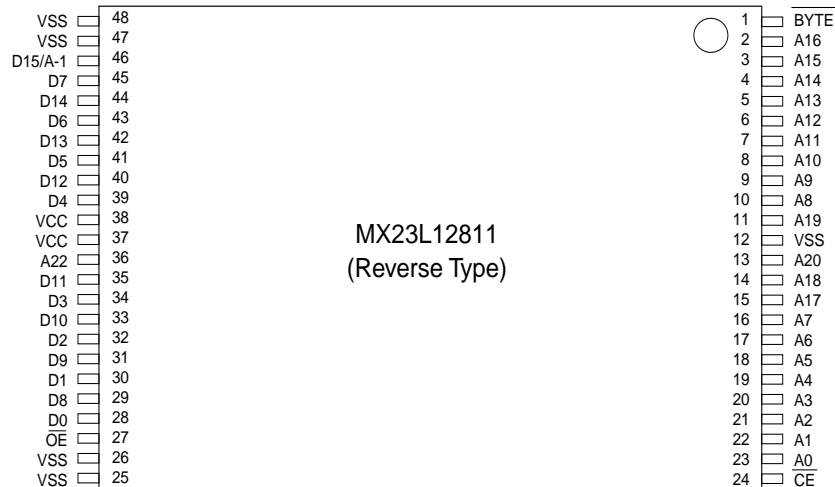
- Bit organization
  - 16M x 8 (byte mode)
  - 8M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
  - Page access: 30ns (max.)
- Page size
  - 8 words per page
- Current
  - Operating: 40mA
  - Standby: 15uA
- Supply voltage
  - 2.7V~3.6V for 120ns
  - 3.0V~3.6V for 100ns
- Package
  - 48 pin TSOP (12mm x 20mm)
  - 48 pin TSOP reverse type
- Temperature
  - 0 ~ 70°C

### PIN CONFIGURATION

#### 48TSOP (Normal Type)



#### 48TSOP (Reverse Type)



## PIN DESCRIPTION

Symbol	Pin Function
A0~A22	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input

Symbol	Pin Function
$\overline{OE}$	Output Enable Input
$\overline{Byte}$	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

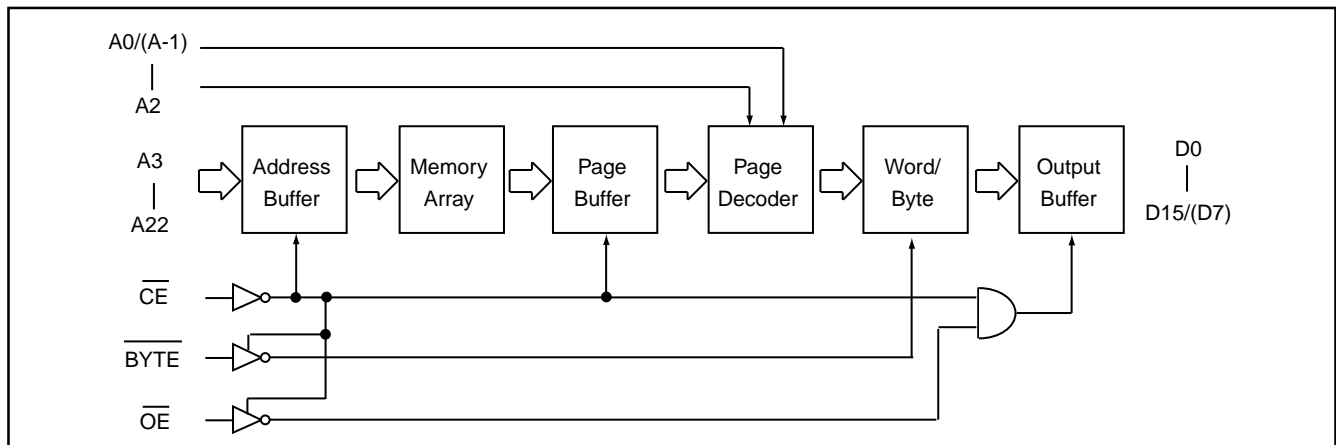
## ORDER INFORMATION

Part No.	Access Time	Page Time	Package	VCC
MX23L12811TC-10	100ns	30ns	48 pin TSOP	3.0V~3.6V
MX23L12811TC-12	120ns	30ns	48 pin TSOP	3.0V~3.6V
*MX23L12811TC-12	120ns	30ns	48 pin TSOP	2.7V~3.6V (under development)
MX23L12811RC-10	100ns	30ns	48 pin TSOP (Reverse type)	3.0V~3.6V
MX23L12811RC-12	120ns	30ns	48 pin TSOP (Reverse type)	3.0V~3.6V
*MX23L12811RC-12	120ns	30ns	48 pin TSOP (Reverse type)	2.7V~3.6V (under development)

## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, inputs may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	40mA	f=5MHz, all outputs open, CE = VIL (Chip Enable) OE = VIH (Output Disabled)
Standby Current (TTL)	ISTB1	-	1mA	CE = VIH
Standby Current (CMOS)	ISTB2	-	15uA	CE > VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

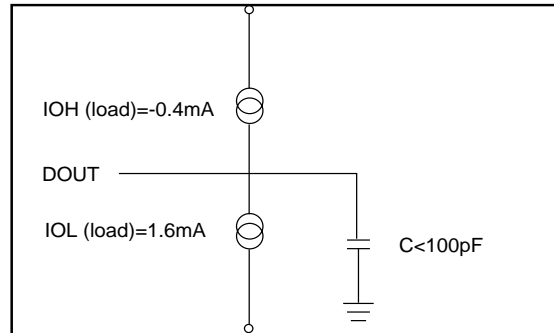
**AC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

Item	Symbol	23L12811-10		23L12811-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	100ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	30ns
Output Enable Time	tOE	-	30ns	-	30ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



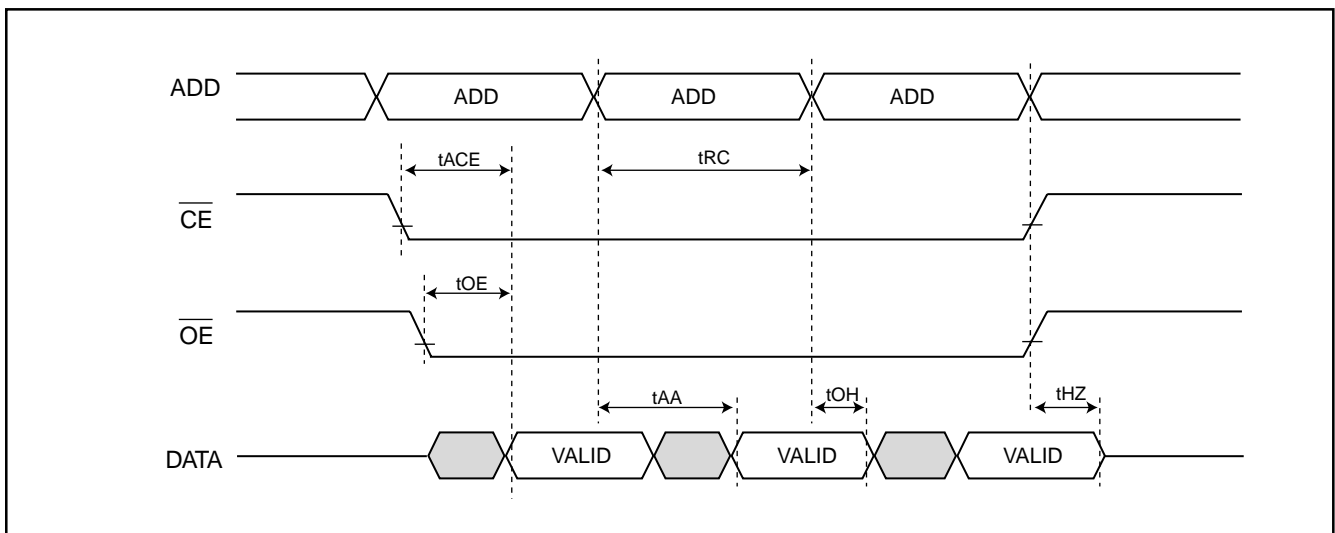
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

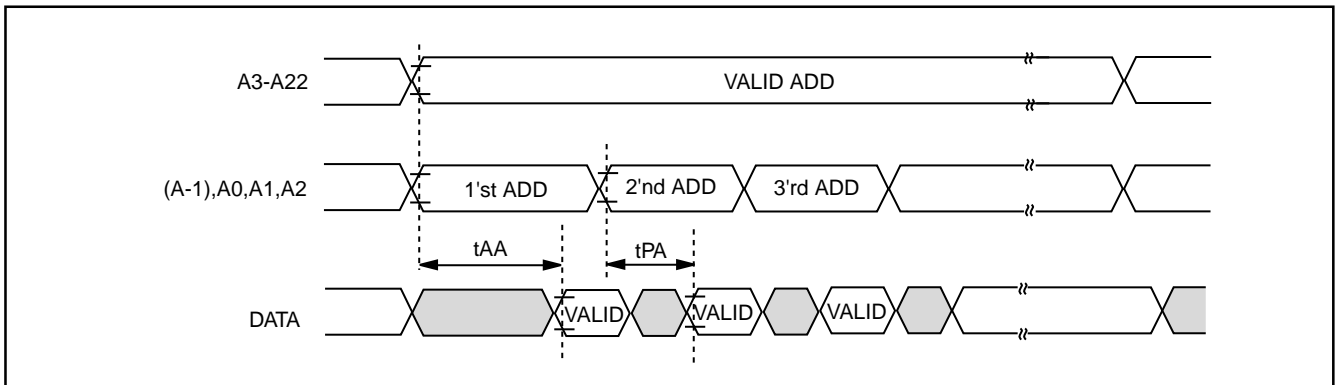
Output loading capacitance includes load board's and all stray capacitance.

## TIMING DIAGRAM

### RANDOM READ

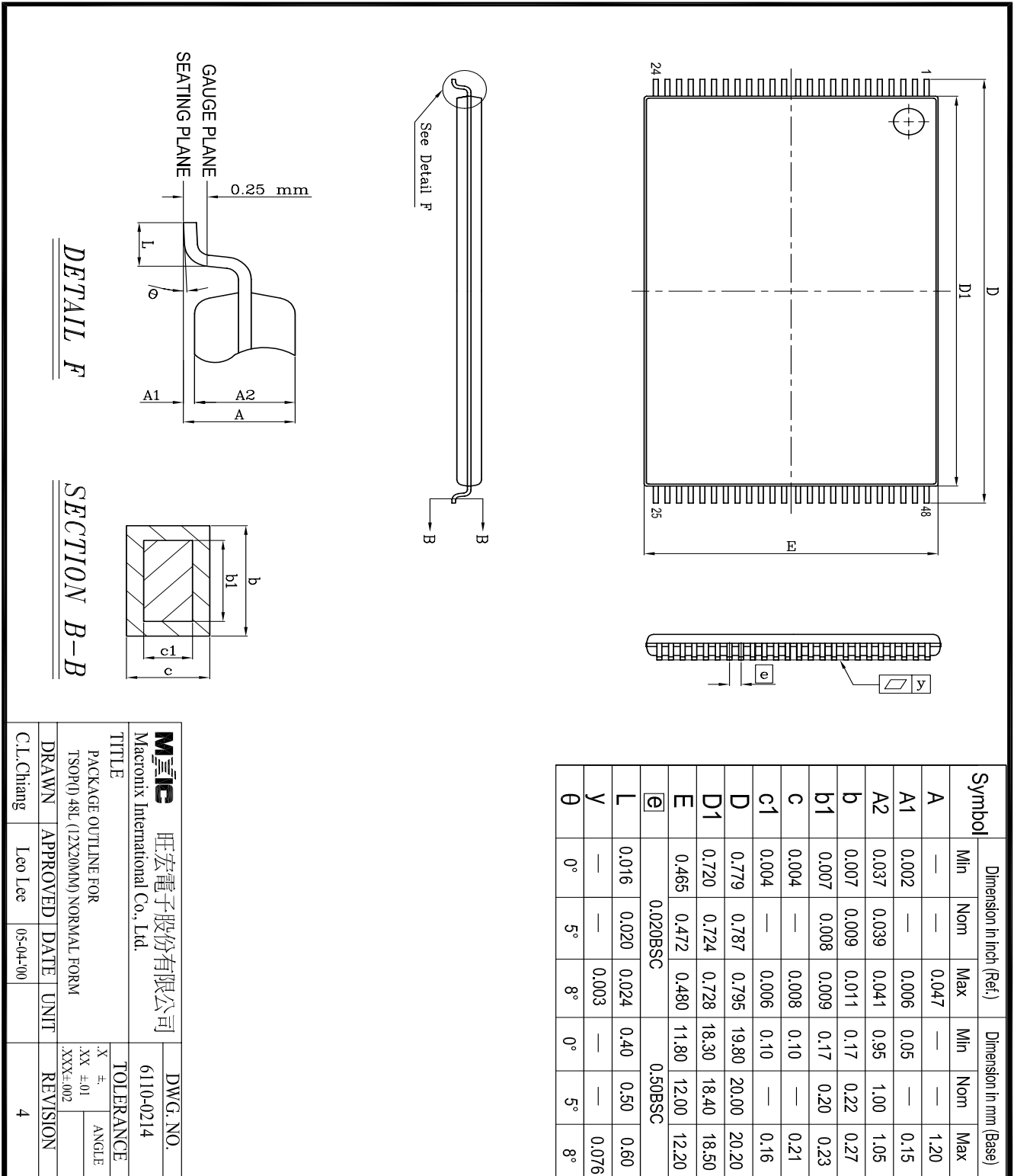


### PAGE READ



## PACKAGE INFORMATION

### 48-PIN PLASTIC TSOP (NORMAL FORM)

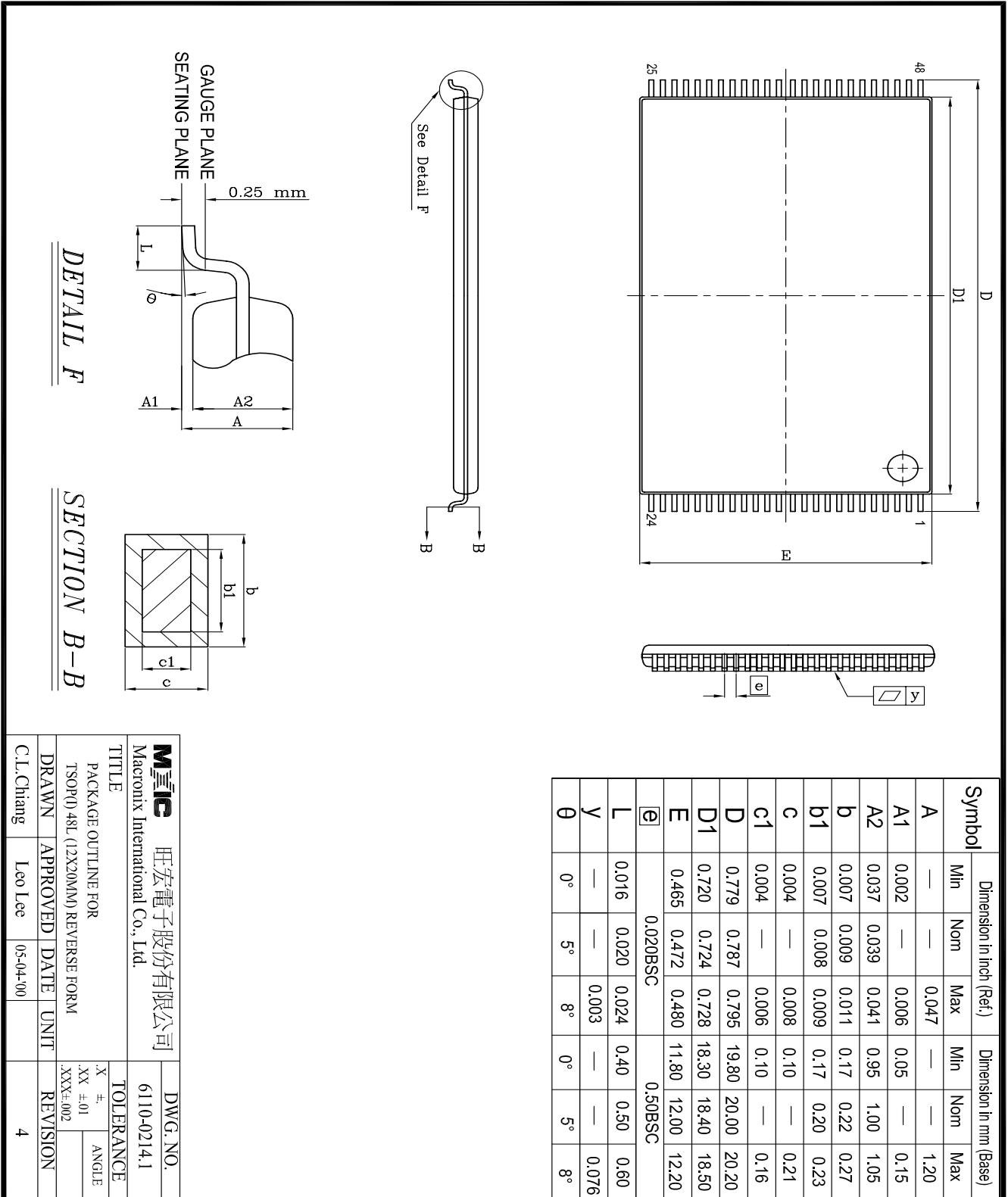


**DETAIL F**

**SECTION B-B**

旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO.	
6110-0214			
TITLE			
PACKAGE OUTLINE FOR			
TSOP(0) 48L (12X20MM) NORMAL FORM			
DRAWN		APPROVED	
C.L.Chang		Leo Lee	
DATE		UNIT	
05-04-00			
REVISION		4	
TOLERANCE		ANGLE	
.X ±.			
.XX ±.01			
.XXX ±.002			

## 48-PIN PLASTIC TSOP (REVERSE FORM)



<b>MAGIC</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0214.1	
TITLE PACKAGE OUTLINE FOR TSOP(D) 48L (12X20MM) REVERSE FORM			
DRAWN C.L.Chiang	APPROVED Leo Lee	DATE 05-04-00	UNIT REVISION 4
TOLERANCE .X ± .XX ±.01 .XXX±.002		ANGLE	

**REVISION HISTORY**

<b>Revision #</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.2	DC Characteristics ISTB2(CMOS Standby Current) 5uA-->15uA	P3	DEC/15/1999
	AC Characteristics TPA(Page Mode Access Time) 50ns-->30ns	P3	
	AC Characteristics TOE(Output Enable Time) 50ns-->30ns	P3	
1.3	Del Package 44-pin SOP	P1,5	JUL/14/2000
1.4	Modify Current Operating:60mA-->40mA	P1	DEC/12/2000
	Modify ICC1:60mA-->40mA, f=5MHz, all outputs open	P3	
	Del ICC2	P3	
1.5	Modify Current Operating:40mA-->50mA	P1	DEC/14/2000
	Modify ICC1:40mA-->50mA	P3	
1.6	1.Modify Fast access time:120ns-->100ns	P1,3	AUG/28/2001
	2.Modify Operating:50mA-->40mA	P1	
	3.Added Temperature:0~70°C	P1	
	4.Modify Supply Voltage : 3.3V±10%-->2.7V~3.6V	P1,3	
	5.Modify Package Information	P5,6	
1.7	1.Add Supply Voltage: 2.7~3.6V for 120ns, 3.0~3.6V for 100ns	P1,2	OCT/12/2001
	2.Modify Order Information	P2	
	3.Add $\overline{CE}=V_{IL}$ , $\overline{OE}=V_{IH}$ in DC Characteristics	P3	



**MX23L12811**

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