MX29LV128M H/L

128M-BIT SINGLE VOLTAGE 3V ONLY UNIFORM SECTOR FLASH MEMORY

FEATURES

GENERAL FEATURES

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Configuration
  - 16,777,216 x 8 / 8,388,608 x 16 switchable
- Sector structure
  - 64KB(32KW) x 256
- Sector Protection/Chip Unprotect
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changes
  - Provides temporary sector group unprotect function for code changes in previously protected sector groups
- Secured Silicon Sector
  - Provides a 128-word OTP area for permanent, secure identification
  - Can be programmed and locked at factory or by customer
- Latch-up protected to 250mA from -1V to VCC + 1V
- Low VCC write inhibit is equal to or less than 1.5V
- Compatible with JEDEC standard
  - Pin-out and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 90R/100ns
  - Page read time: 25ns
  - Sector erase time: 0.5s (typ.)
  - 4 word/8 byte page read buffer
  - 16 word/ 32 byte write buffer: reduces programming time for multiple-word/byte updates
- Low Power Consumption
  - Active read current: 18mA(typ.)
  - Active write current: 20mA(typ.)
  - Standby current: 20uA(typ.)
- Minimum 100,000 erase/program cycle
- 20-years data retention

SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access.
- Program Suspend/Program Resume
  - Suspend program operation to read other sectors
- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data/program other sectors
- Status Reply
  - Data# polling & Toggle bits provide detection of program and erase operation completion

HARDWARE FEATURES

- Ready/Busy (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input
  - Write protect (WP#) function allows protection highest or lowest sector, regardless of sector protection settings
  - ACC (high voltage) accelerates programming time for higher throughput during system

PACKAGE

- 56-pin TSOP
- **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX29LV128M H/L is a 128-mega bit Flash memory organized as 16M bytes of 8 bits or 8M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV128M H/L is packaged in 56-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV128M H/L offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV128M H/L has separate chip enable (CE#) and output enable (OE#) controls.

MXIC's Flash memories augment EPROM functionality

with in-circuit electrical erasure and programming. The MX29LV128M H/L uses a command register to manage this functionality.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29LV128M H/L uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

AUTOMATIC PROGRAMMING

The MX29LV128M H/L is byte/word/page programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA# polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LV128M H/L is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

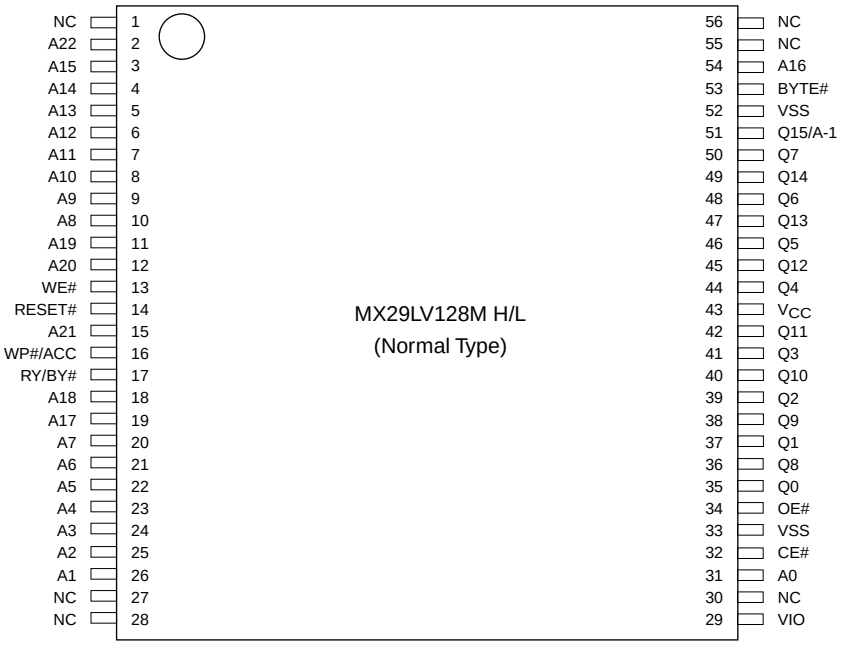
Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE# .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV128M H/L electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

PIN CONFIGURATION

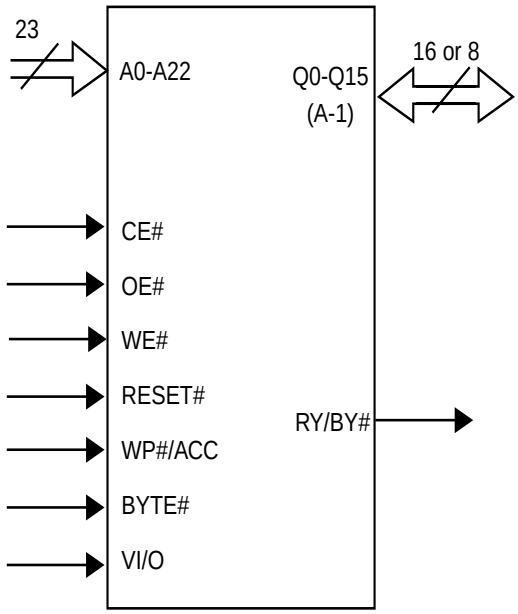
56 TSOP



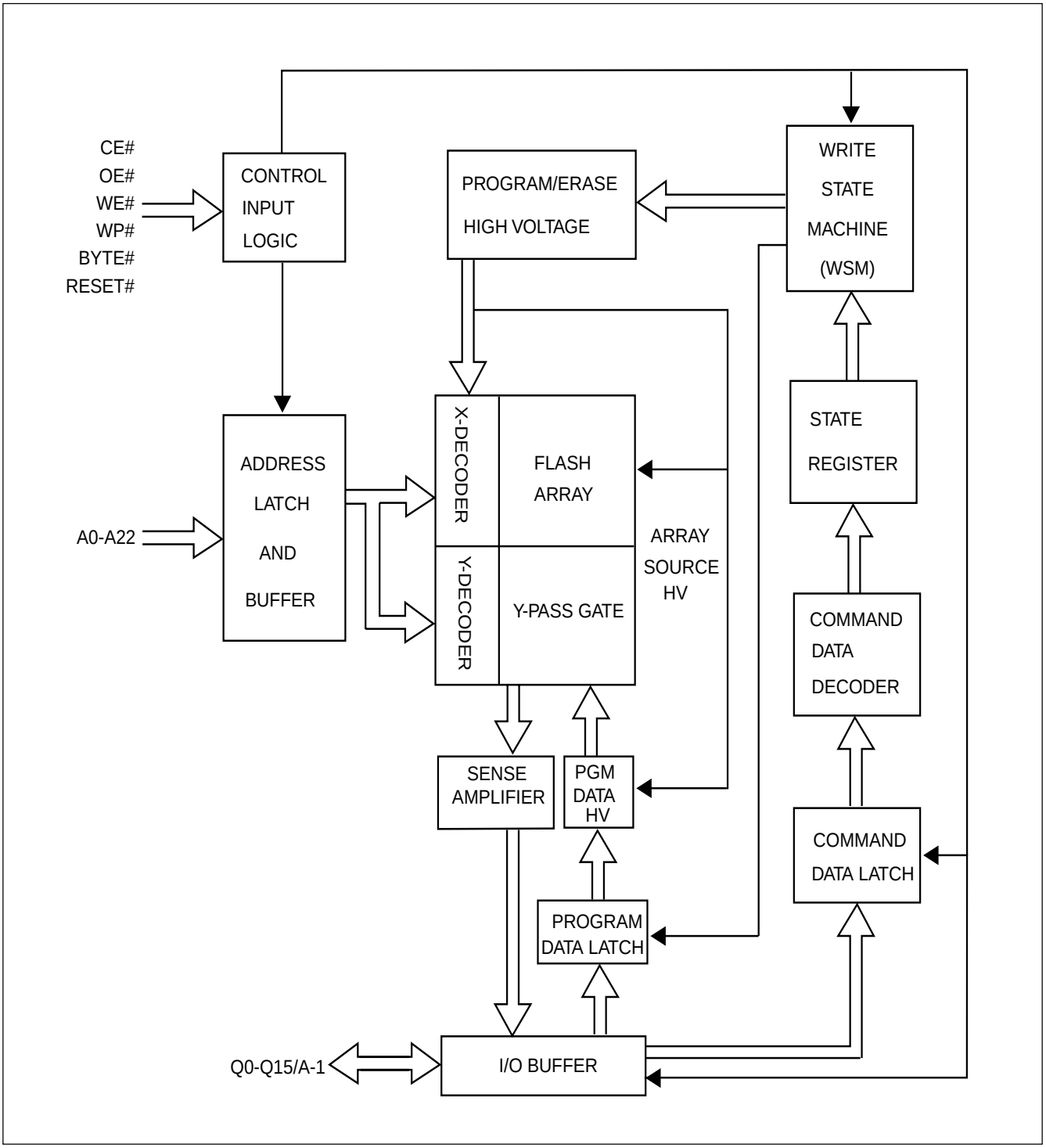
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A22	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC	Hardware Write Protect/Programming Acceleration input
RY/BY#	Read/Busy Output
BYTE#	Selects 8 bit or 16 bit mode
VCC	+3.0V single power supply
VI/O	Output Buffer Power (2.7V~3.6V this input should be tied directly to VCC)
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM



MX29LV128M H/L SECTOR ADDRESS TABLE

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	00000000	64/32	000000-0FFFF	000000-07FFF
SA1	00000001	64/32	010000-1FFFF	008000-0FFFF
SA2	00000010	64/32	020000-2FFFF	010000-17FFF
SA3	00000011	64/32	030000-3FFFF	018000-1FFFF
SA4	00000100	64/32	040000-4FFFF	020000-27FFF
SA5	00000101	64/32	050000-5FFFF	028000-2FFFF
SA6	00000110	64/32	060000-6FFFF	030000-37FFF
SA7	00000111	64/32	070000-7FFFF	038000-3FFFF
SA8	00001000	64/32	080000-8FFFF	040000-47FFF
SA9	00001001	64/32	090000-9FFFF	048000-4FFFF
SA10	00001010	64/32	0A0000-AFFFF	050000-57FFF
SA11	00001011	64/32	0B0000-BFFFF	058000-5FFFF
SA12	00001100	64/32	0C0000-CFFFF	060000-67FFF
SA13	00001101	64/32	0D0000-DFFFF	068000-6FFFF
SA14	00001110	64/32	0E0000-EFFFF	070000-77FFF
SA15	00001111	64/32	0F0000-FFFFF	078000-7FFFF
SA16	00010000	64/32	100000-0FFFF	080000-87FFF
SA17	00010001	64/32	110000-1FFFF	088000-8FFFF
SA18	00010010	64/32	120000-2FFFF	090000-97FFF
SA19	00010011	64/32	130000-3FFFF	098000-9FFFF
SA20	00010100	64/32	140000-4FFFF	0A0000-A7FFF
SA21	00010101	64/32	150000-5FFFF	0A8000-AFFFF
SA22	00010110	64/32	160000-6FFFF	0B0000-B7FFF
SA23	00010111	64/32	170000-7FFFF	0B8000-BFFFF
SA24	00011000	64/32	180000-8FFFF	0C0000-C7FFF
SA25	00011001	64/32	190000-9FFFF	0C8000-CFFFF
SA26	00011010	64/32	1A0000-AFFFF	0D0000-D7FFF
SA27	00011011	64/32	1B0000-BFFFF	0D8000-DFFFF
SA28	00011100	64/32	1C0000-CFFFF	0E0000-E7FFF
SA29	00011101	64/32	1D0000-DFFFF	0E8000-EFFFF
SA30	00011110	64/32	1E0000-EFFFF	0F0000-F7FFF
SA31	00011111	64/32	1F0000-FFFFF	0F8000-FFFFF
SA32	00100000	64/32	200000-0FFFF	100000-07FFF
SA33	00100001	64/32	210000-1FFFF	108000-0FFFF
SA34	00100010	64/32	220000-2FFFF	110000-17FFF
SA35	00100011	64/32	230000-3FFFF	118000-1FFFF
SA36	00100100	64/32	240000-4FFFF	120000-27FFF
SA37	00100101	64/32	250000-5FFFF	128000-2FFFF
SA38	00100110	64/32	260000-6FFFF	130000-37FFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA39	00100111	64/32	270000-7FFFF	138000-3FFFF
SA40	00101000	64/32	280000-8FFFF	140000-47FFF
SA41	00101001	64/32	290000-9FFFF	148000-4FFFF
SA42	00101010	64/32	2A0000-AFFFF	150000-57FFF
SA43	00101011	64/32	2B0000-BFFFF	158000-5FFFF
SA44	00101100	64/32	2C0000-CFFFF	160000-67FFF
SA45	00101101	64/32	2D0000-DFFFF	168000-6FFFF
SA46	00101110	64/32	2E0000-EFFFF	170000-77FFF
SA47	00101111	64/32	2F0000-FFFFF	178000-7FFFF
SA48	00110000	64/32	300000-0FFFF	180000-87FFF
SA49	00110001	64/32	310000-1FFFF	188000-8FFFF
SA50	00110010	64/32	320000-2FFFF	190000-97FFF
SA51	00110011	64/32	330000-3FFFF	198000-9FFFF
SA52	00110100	64/32	340000-4FFFF	1A0000-A7FFF
SA53	00110101	64/32	350000-5FFFF	1A8000-AFFFF
SA54	00110110	64/32	360000-6FFFF	1B0000-B7FFF
SA55	00110111	64/32	370000-7FFFF	1B8000-BFFFF
SA56	00111000	64/32	380000-8FFFF	1C0000-C7FFF
SA57	00111001	64/32	390000-9FFFF	1C8000-CFFFF
SA58	00111010	64/32	3A0000-AFFFF	1D0000-D7FFF
SA59	00111011	64/32	3B0000-BFFFF	1D8000-DFFFF
SA60	00111100	64/32	3C0000-CFFFF	1E0000-E7FFF
SA61	00111101	64/32	3D0000-DFFFF	1E8000-EFFFF
SA62	00111110	64/32	3E0000-EFFFF	1F0000-F7FFF
SA63	00111111	64/32	3F0000-FFFFF	1F8000-FFFFF
SA64	01000000	64/32	400000-0FFFF	200000-07FFF
SA65	01000001	64/32	410000-1FFFF	208000-0FFFF
SA66	01000010	64/32	420000-2FFFF	210000-17FFF
SA67	01000011	64/32	430000-3FFFF	218000-1FFFF
SA68	01000100	64/32	440000-4FFFF	220000-27FFF
SA69	01000101	64/32	450000-5FFFF	228000-2FFFF
SA70	01000110	64/32	460000-6FFFF	230000-37FFF
SA71	01000111	64/32	470000-7FFFF	238000-3FFFF
SA72	01001000	64/32	480000-8FFFF	240000-47FFF
SA73	01001001	64/32	490000-9FFFF	248000-4FFFF
SA74	01001010	64/32	4A0000-AFFFF	250000-57FFF
SA75	01001011	64/32	4B0000-BFFFF	258000-5FFFF
SA76	01001100	64/32	4C0000-CFFFF	260000-67FFF
SA77	01001101	64/32	4D0000-DFFFF	268000-6FFFF
SA78	01001110	64/32	4E0000-EFFFF	270000-77FFF
SA79	01001111	64/32	4F0000-FFFFF	278000-7FFFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA80	01010000	64/32	500000-0FFFF	280000-87FFF
SA81	01010001	64/32	510000-1FFFF	288000-8FFFF
SA82	01010010	64/32	520000-2FFFF	290000-97FFF
SA83	01010011	64/32	530000-3FFFF	298000-9FFFF
SA84	01010100	64/32	540000-4FFFF	2A0000-A7FFF
SA85	01010101	64/32	550000-5FFFF	2A8000-AFFFF
SA86	01010110	64/32	560000-6FFFF	2B0000-B7FFF
SA87	01010111	64/32	570000-7FFFF	2B8000-BFFFF
SA88	01011000	64/32	580000-8FFFF	2C0000-C7FFF
SA89	01011001	64/32	590000-9FFFF	2C8000-CFFFF
SA90	01011010	64/32	5A0000-AFFFF	2D0000-D7FFF
SA91	01011011	64/32	5B0000-BFFFF	2D8000-DFFFF
SA92	01011100	64/32	5C0000-CFFFF	2E0000-E7FFF
SA93	01011101	64/32	5D0000-DFFFF	2E8000-EFFFF
SA94	01011110	64/32	5E0000-EFFFF	2F0000-F7FFF
SA95	01011111	64/32	5F0000-FFFFF	2F8000-FFFFF
SA96	01100000	64/32	600000-0FFFF	300000-07FFF
SA97	01100001	64/32	610000-1FFFF	308000-0FFFF
SA98	01100010	64/32	620000-2FFFF	310000-17FFF
SA99	01100011	64/32	630000-3FFFF	318000-1FFFF
SA100	01100100	64/32	640000-4FFFF	320000-27FFF
SA101	01100101	64/32	650000-5FFFF	328000-2FFFF
SA102	01100110	64/32	660000-6FFFF	330000-37FFF
SA103	01100111	64/32	670000-7FFFF	338000-3FFFF
SA104	01101000	64/32	680000-8FFFF	340000-47FFF
SA105	01101001	64/32	690000-9FFFF	348000-4FFFF
SA106	01101010	64/32	6A0000-AFFFF	350000-57FFF
SA107	01101011	64/32	6B0000-BFFFF	358000-5FFFF
SA108	01101100	64/32	6C0000-CFFFF	360000-67FFF
SA109	01101101	64/32	6D0000-DFFFF	368000-6FFFF
SA110	01101110	64/32	6E0000-EFFFF	370000-77FFF
SA111	01101111	64/32	6F0000-FFFFF	378000-7FFFF
SA112	01110000	64/32	700000-0FFFF	380000-87FFF
SA113	01110001	64/32	710000-1FFFF	388000-8FFFF
SA114	01110010	64/32	720000-2FFFF	390000-97FFF
SA115	01110011	64/32	730000-3FFFF	398000-9FFFF
SA116	01110100	64/32	740000-4FFFF	3A0000-A7FFF
SA117	01110101	64/32	750000-5FFFF	3A8000-AFFFF
SA118	01110110	64/32	760000-6FFFF	3B0000-B7FFF
SA119	01110111	64/32	770000-7FFFF	3B8000-BFFFF
SA120	01111000	64/32	780000-8FFFF	3C0000-C7FFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA121	01111001	64/32	790000-9FFFF	3C8000-CFFFF
SA122	01111010	64/32	7A0000-AFFFF	3D0000-D7FFF
SA123	01111011	64/32	7B0000-BFFFF	3D8000-DFFFF
SA124	01111100	64/32	7C0000-CFFFF	3E0000-E7FFF
SA125	01111101	64/32	7D0000-DFFFF	3E8000-EFFFF
SA126	01111110	64/32	7E0000-EFFFF	3F0000-F7FFF
SA127	01111111	64/32	7F0000-FFFFF	3F8000-FFFFF
SA128	10000000	64/32	800000-0FFFF	400000-07FFF
SA129	10000001	64/32	810000-1FFFF	408000-0FFFF
SA130	10000010	64/32	820000-2FFFF	410000-17FFF
SA131	10000011	64/32	830000-3FFFF	418000-1FFFF
SA132	10000100	64/32	840000-4FFFF	420000-27FFF
SA133	10000101	64/32	850000-5FFFF	428000-2FFFF
SA134	10000110	64/32	860000-6FFFF	430000-37FFF
SA135	10000111	64/32	870000-7FFFF	438000-3FFFF
SA136	10001000	64/32	880000-8FFFF	440000-47FFF
SA137	10001001	64/32	890000-9FFFF	448000-4FFFF
SA138	10001010	64/32	8A0000-AFFFF	450000-57FFF
SA139	10001011	64/32	8B0000-BFFFF	458000-5FFFF
SA140	10001100	64/32	8C0000-CFFFF	460000-67FFF
SA141	10001101	64/32	8D0000-DFFFF	468000-6FFFF
SA142	10001110	64/32	8E0000-EFFFF	470000-77FFF
SA143	10001111	64/32	8F0000-FFFFF	478000-7FFFF
SA144	10010000	64/32	900000-0FFFF	480000-87FFF
SA145	10010001	64/32	910000-1FFFF	488000-8FFFF
SA146	10010010	64/32	920000-2FFFF	490000-97FFF
SA147	10010011	64/32	930000-3FFFF	498000-9FFFF
SA148	10010100	64/32	940000-4FFFF	4A0000-A7FFF
SA149	10010101	64/32	950000-5FFFF	4A8000-AFFFF
SA150	10010110	64/32	960000-6FFFF	4B0000-B7FFF
SA151	10010111	64/32	970000-7FFFF	4B8000-BFFFF
SA152	10011000	64/32	980000-8FFFF	4C0000-C7FFF
SA153	10011001	64/32	990000-9FFFF	4C8000-CFFFF
SA154	10011010	64/32	9A0000-AFFFF	4D0000-D7FFF
SA155	10011011	64/32	9B0000-BFFFF	4D8000-DFFFF
SA156	10011100	64/32	9C0000-CFFFF	4E0000-E7FFF
SA157	10011101	64/32	9D0000-DFFFF	4E8000-EFFFF
SA158	10011110	64/32	9E0000-EFFFF	4F0000-F7FFF
SA159	10011111	64/32	9F0000-FFFFF	4F8000-FFFFF
SA160	10100000	64/32	A00000-0FFFF	500000-07FFF
SA161	10100001	64/32	A10000-1FFFF	508000-0FFFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA162	10100010	64/32	A20000-2FFFF	510000-17FFF
SA163	10100011	64/32	A30000-3FFFF	518000-1FFFF
SA164	10100100	64/32	A40000-4FFFF	520000-27FFF
SA165	10100101	64/32	A50000-5FFFF	528000-2FFFF
SA166	10100110	64/32	A60000-6FFFF	530000-37FFF
SA167	10100111	64/32	A70000-7FFFF	538000-3FFFF
SA168	10101000	64/32	A80000-8FFFF	540000-47FFF
SA169	10101001	64/32	A90000-9FFFF	548000-4FFFF
SA170	10101010	64/32	AA0000-AFFFF	550000-57FFF
SA171	10101011	64/32	AB0000-BFFFF	558000-5FFFF
SA172	10101100	64/32	AC0000-CFFFF	560000-67FFF
SA173	10101101	64/32	AD0000-DFFFF	568000-6FFFF
SA174	10101110	64/32	AE0000-EFFFF	570000-77FFF
SA175	10101111	64/32	AF0000-FFFFF	578000-7FFFF
SA176	10110000	64/32	B00000-0FFFF	580000-87FFF
SA177	10110001	64/32	B10000-1FFFF	588000-8FFFF
SA178	10110010	64/32	B20000-2FFFF	590000-97FFF
SA179	10110011	64/32	B30000-3FFFF	598000-9FFFF
SA180	10110100	64/32	B40000-4FFFF	5A0000-A7FFF
SA181	10110101	64/32	B50000-5FFFF	5A8000-AFFFF
SA182	10110110	64/32	B60000-6FFFF	5B0000-B7FFF
SA183	10110111	64/32	B70000-7FFFF	5B8000-BFFFF
SA184	10111000	64/32	B80000-8FFFF	5C0000-C7FFF
SA185	10111001	64/32	B90000-9FFFF	5C8000-CFFFF
SA186	10111010	64/32	BA0000-AFFFF	5D0000-D7FFF
SA187	10111011	64/32	BB0000-BFFFF	5D8000-DFFFF
SA188	10111100	64/32	BC0000-CFFFF	5E0000-E7FFF
SA189	10111101	64/32	BD0000-DFFFF	5E8000-EFFFF
SA190	10111110	64/32	BE0000-EFFFF	5F0000-F7FFF
SA191	10111111	64/32	BF0000-FFFFF	5F8000-FFFFF
SA192	11000000	64/32	C00000-0FFFF	600000-07FFF
SA193	11000001	64/32	C10000-1FFFF	608000-0FFFF
SA194	11000010	64/32	C20000-2FFFF	610000-17FFF
SA195	11000011	64/32	C30000-3FFFF	618000-1FFFF
SA196	11000100	64/32	C40000-4FFFF	620000-27FFF
SA197	11000101	64/32	C50000-5FFFF	628000-2FFFF
SA198	11000110	64/32	C60000-6FFFF	630000-37FFF
SA199	11000111	64/32	C70000-7FFFF	638000-3FFFF
SA200	11001000	64/32	C80000-8FFFF	640000-47FFF
SA201	11001001	64/32	C90000-9FFFF	648000-4FFFF
SA202	11001010	64/32	CA0000-AFFFF	650000-57FFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA203	11001011	64/32	CB0000-BFFFF	658000-5FFFF
SA204	11001100	64/32	CC0000-CFFFF	660000-67FFF
SA205	11001101	64/32	CD0000-DFFFF	668000-6FFFF
SA206	11001110	64/32	CE0000-EFFFF	670000-77FFF
SA207	11001111	64/32	CF0000-FFFFF	678000-7FFFF
SA208	11010000	64/32	D00000-0FFFF	680000-87FFF
SA209	11010001	64/32	D10000-1FFFF	688000-8FFFF
SA210	11010010	64/32	D20000-2FFFF	690000-97FFF
SA211	11010011	64/32	D30000-3FFFF	698000-9FFFF
SA212	11010100	64/32	D40000-4FFFF	6A0000-A7FFF
SA213	11010101	64/32	D50000-5FFFF	6A8000-AFFFF
SA214	11010110	64/32	D60000-6FFFF	6B0000-B7FFF
SA215	11010111	64/32	D70000-7FFFF	6B8000-BFFFF
SA216	11011000	64/32	D80000-8FFFF	6C0000-C7FFF
SA217	11011001	64/32	D90000-9FFFF	6C8000-CFFFF
SA218	11011010	64/32	DA0000-AFFFF	6D0000-D7FFF
SA219	11011011	64/32	DB0000-BFFFF	6D8000-DFFFF
SA220	11011100	64/32	DC0000-CFFFF	6E0000-E7FFF
SA221	11011101	64/32	DD0000-DFFFF	6E8000-EFFFF
SA222	11011110	64/32	DE0000-EFFFF	6F0000-F7FFF
SA223	11011111	64/32	DF0000-FFFFF	6F8000-FFFFF
SA224	11100000	64/32	E00000-0FFFF	700000-07FFF
SA225	11100001	64/32	E10000-1FFFF	708000-0FFFF
SA226	11100010	64/32	E20000-2FFFF	710000-17FFF
SA227	11100011	64/32	E30000-3FFFF	718000-1FFFF
SA228	11100100	64/32	E40000-4FFFF	720000-27FFF
SA229	11100101	64/32	E50000-5FFFF	728000-2FFFF
SA230	11100110	64/32	E60000-6FFFF	730000-37FFF
SA231	11100111	64/32	E70000-7FFFF	738000-3FFFF
SA232	11101000	64/32	E80000-8FFFF	740000-47FFF
SA233	11101001	64/32	E90000-9FFFF	748000-4FFFF
SA234	11101010	64/32	EA0000-AFFFF	750000-57FFF
SA235	11101011	64/32	EB0000-BFFFF	758000-5FFFF
SA236	11101100	64/32	EC0000-CFFFF	760000-67FFF
SA237	11101101	64/32	ED0000-DFFFF	768000-6FFFF
SA238	11101110	64/32	EE0000-EFFFF	770000-77FFF
SA239	11101111	64/32	EF0000-FFFFF	778000-7FFFF
SA240	11110000	64/32	F00000-0FFFF	780000-87FFF

Sector	Sector Address A22-A15	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA241	11110001	64/32	F10000-1FFFF	788000-8FFFF
SA242	11110010	64/32	F20000-2FFFF	790000-97FFF
SA243	11110011	64/32	F30000-3FFFF	798000-9FFFF
SA244	11110100	64/32	F40000-4FFFF	7A0000-A7FFF
SA245	11110101	64/32	F50000-5FFFF	7A8000-AFFFF
SA246	11110110	64/32	F60000-6FFFF	7B0000-B7FFF
SA247	11110111	64/32	F70000-7FFFF	7B8000-BFFFF
SA248	11111000	64/32	F80000-8FFFF	7C0000-C7FFF
SA249	11111001	64/32	F90000-9FFFF	7C8000-CFFFF
SA250	11111010	64/32	FA0000-AFFFF	7D0000-D7FFF
SA251	11111011	64/32	FB0000-BFFFF	7D8000-DFFFF
SA252	11111100	64/32	FC0000-CFFFF	7E0000-E7FFF
SA253	11111101	64/32	FD0000-DFFFF	7E8000-EFFFF
SA254	11111110	64/32	FE0000-EFFFF	7F0000-F7FFF
SA255	11111111	64/32	FF0000-FFFFF	7F8000-FFFFF

MX29LV128M H/L Sector Group Protection Address Table

Sector Group	A22-A15
SA0	00000000
SA1	00000001
SA2	00000010
SA3	00000011
SA4-SA7	000001xx
SA8-SA11	000010xx
SA12-SA15	000011xx
SA16-SA19	000100xx
SA20-SA23	000101xx
SA24-SA27	000110xx
SA28-SA31	000111xx
SA32-SA35	001000xx
SA36-SA39	001001xx
SA40-SA43	001010xx
SA44-SA47	001011xx
SA48-SA51	001100xx
SA52-SA55	001101xx
SA56-SA59	001110xx
SA60-SA63	001111xx
SA64-SA67	010000xx
SA68-SA71	010001xx
SA72-SA75	010010xx
SA76-SA79	010011xx
SA80-SA83	010100xx
SA84-SA87	010101xx
SA88-SA91	010110xx
SA92-SA95	010111xx
SA96-SA99	011000xx
SA100-SA103	011001xx
SA104-SA107	011010xx
SA108-SA111	011011xx
SA112-SA115	011100xx
SA116-SA119	011101xx
SA120-SA123	011110xx
SA124-SA127	011111xx

Sector Group	A22-A15
SA128-SA131	100000xx
SA132-SA135	100001xx
SA136-SA139	100010xx
SA140-SA143	100011xx
SA144-SA147	100100xx
SA148-SA151	100101xx
SA152-SA155	100110xx
SA156-SA159	100111xx
SA160-SA163	101000xx
SA164-SA167	101001xx
SA168-SA171	101010xx
SA172-SA175	101011xx
SA176-SA179	101100xx
SA180-SA183	101101xx
SA184-SA187	101110xx
SA188-SA191	101111xx
SA192-SA195	110000xx
SA196-SA199	110001xx
SA200-SA203	110010xx
SA204-SA207	110011xx
SA208-SA211	110100xx
SA202-SA215	110101xx
SA206-SA219	110110xx
SA220-SA223	110111xx
SA224-SA227	111000xx
SA228-SA231	111001xx
SA232-SA235	111010xx
SA236-SA239	111011xx
SA240-SA243	111100xx
SA244-SA247	111101xx
SA248-SA251	111110xx
SA252	11111100
SA253	11111101
SA254	11111110
SA255	11111111

Table 1. BUS OPERATION (1)

Operation	CE#	OE#	WE#	RE-SET#	WP#	ACC	Address	Q0~Q7	Q8~Q15	
									Word Mode	Byte Mode
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}	Q8-Q14= High Z Q15=A-1
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)	(Note 4	Q8-Q14= High Z Q15=A-1
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)	(Note 4)	Q8-Q14= High Z Q15=A-1
Standby	VCC± 0.3V	X	X	VCC± 0.3V	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	Sector Addresses, A6=L,A3=L, A2=L, A1=H,A0=L	(Note 4)	X	X
Chip unprotect (Note 2)	L	H	L	V_{ID}	H	X	Sector Addresses, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	X	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend:
L=Logic LOW=V_{IL}, H=Logic High=V_{IH}, V_{ID}=12.0±0.5V, V_{HH}=12.0±0.5V, X=Don't Care, A_{IN}=Address IN, D_{IN}=Data IN, D_{OUT}=Data OUT

Notes:
1. Address are A21:A0 in word mode; A21:A-1 in byte mode. Sector addresses are A21:A15 in both modes.
2. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotect" section.
3. If WP#=VIL, the first sectors remain protected. If WP#=VIH, the highest or lowest sector protection depends on whether they were last protected or unprotect using the method described in "Sector/ Sector Block Protection and Unprotect".
4. D_{IN} or D_{OUT} as required by command sequence, Data# polling or sector protect algorithm (see Figure 15).

Table 2. AUTOSELECT CODES (High Voltage Method)

Description		CE#	OE#	WE#	A22 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q8 to Q15		Q7 to Q0
														Word Mode	Byte Mode	
Manufacturer ID		L	L	H	X	X	VID	X	L	X	L	L	L	00	X	C2h
29LV128MH/L	Cycle 1	L	L	H	X	X	VID	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	12h
	Cycle 3										H	H	H	22	X	00h
Sector Group Protection Verification		L	L	H	SA	X	VID	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (Q7), WP# protects highest address sector		L	L	H	X	X	VID	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
Secured Silicon Sector Indicator Bit (Q7), WP# protects lowest address sector		L	L	H	X	X	VID	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't care.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

PAGE MODE READ

The MX29LV128M H/L offers "fast page mode read" function. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A0~A1(Word Mode)/A-1~A1(Byte Mode) This is an asynchronous operation; the microprocessor supplies the specific word location.

The system performance could be enhanced by initiating 1 normal read and 3 fast page read (for word mode A0-A1) or 7 fast page read (for byte mode A-1~A1). When CE# is deasserted and reasserted for a subsequent access, the access time is tACC or tCE. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

WRITING COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory, the system must drive WE# and CE# to VIL, and OE# to VIH.

An erase operation can erase one sector, multiple sectors, or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

WRITE BUFFER

Write Buffer Programming allows the system to write a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

ACCELERATED PROGRAM OPERATION

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing VHH from the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

STANDBY MODE

When using both pins of CE# and RESET#, the device enter CMOS Standby with both pins held at VCC ±0.3V. If CE# and RESET# are held at VIH, but not within the range of VCC ±0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, VCC active current (ICC2) is required even CE# = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes, before it is ready to read data.

AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when address remain stable for tACC+30ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC4 in the DC Characteristics table represents the automatic sleep mode current specification.

OUTPUT DISABLE

With the OE# input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

RESET# OPERATION

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the RESET# pulse. When RESET# is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If RESET# is held at VIL but not within VSS±0.3V, the standby current will be greater.

The RESET# pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET# pin returns to VIH.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 3 for the timing diagram.

SECTOR GROUP PROTECT OPERATION

The MX29LV128M H/L features hardware sector group protection. This feature will disable both program and erase operations for these sector group protected. In this device, a sector group consists of four adjacent sectors which are protected or unprotected at the same time. To activate this mode, the programming equipment must force VID on address pin A9 and control pin OE#, (suggest VID = 12V) A6 = VIL and CE# = VIL. (see Table 2) Programming of the protection circuitry begins on the falling edge of the WE# pulse and is terminated on the rising edge. Please refer to sector group protect algorithm and waveform.

MX29LV128M H/L also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE# and OE# at VIL and WE# at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT OPERATION

The MX29LV128M H/L also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE# and address pin A9. The CE# pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotect mechanism begins on the falling edge of the WE# pulse and is terminated on the rising edge.

MX29LV128M H/L also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

It is also possible to determine if the chip is unprotect in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotect sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

WRITE PROTECT (WP#)

The write protect function provides a hardware method to protect sector without using V_{ID}.

If the system asserts VIL on the WP# pin, the device disables program and erase functions in the first (MX29LV128MH) or last (MX29LV128ML) sector independently of whether those sectors were protected or unprotect using the method described in Sector/Sector Group Protection and Chip Unprotect".

If the system asserts VIH on the WP# pin, the device reverts to whether the first (MX29LV128MH) or last (MX29LV128ML) sector were last set to be protected or unprotect. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotect using the method described in "Sector/Sector Group Protection and Chip Unprotect".

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

This feature allows temporary unprotect of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as unprotect sector. Once VID is remove from the RESET# pin, all the previously protected sectors are protected again.

SILICON ID READ OPERATION

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX29LV128M H/L provides hardware method to access the silicon ID read operation. Which method requires VID on A9 pin, VIL on CE#, OE#, A6, and A1 pins. Which apply VIL on A0 pin, the device will output MXIC's manufacture code of which apply VIH on A0 pin, the device will output MX29LV128M H/L device code.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV128M H/L provides hardware method for sector group protect status verify. Which method requires VID on A9 pin, VIH on WE# and A1 pins, VIL on CE#, OE#, A6, and A0 pins, and sector address on A16 to A21 pins. Which the identified sector is protected, the device will output 01H. Which the identified sector is not protect, the device will output 00H.

DATA PROTECTION

The MX29LV128M H/L is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

SECURED SILICON SECTOR

The MX29LV128M H/L features a OTP memory region where the system may access through a command sequence to create a permanent part identification as so called Electronic Serial Number (ESN) in the device. Once this region is programmed, any further modification on the region is impossible. The secured silicon sector is a 128 words in length, and uses a Secured Silicon Sector Indicator Bit (Q7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevent duplication of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The MX29LV128M H/L offers the device with Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory , and has the Secured Silicon Sector Indicator Bit permanently set to a "1". The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to utilize that sector in any form they prefer. The customer-lockable version has the secured sector Indicator Bit permanently set to a "0". Therefore, the Secured Silicon Sector Indicator Bit prevents customer, lockable device from being used to replace devices that are factory locked.

The system access the Secured Silicon Sector through a command sequence (refer to "Enter Secured Silicon/ Exit Secured Silicon Sector command Sequence). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the address normally occupied by the first sector SA0. Once entry the Secured Silicon Sector the operation of boot sectors is disabled but the operation of main sectors is as normally. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending command to sector SA0.

Secured Silicon Sector address range	ESN factory locked	Customer lockable
000000h-000007h	ESN	Determined by Customer
000008h-00007Fh	Unavailable	

FACTORY LOCKED:Secured Silicon Sector Programmed and Protected At the Factory

In device with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. A factory locked device has an 8-word random ESN at address 000000h-000007h.

CUSTOMER LOCKABLE:Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 128-word Secured Silicon Sector. Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotected the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 15, except that RESET# may be at either VIH or VID. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that method is only applicable to the Secured Silicon Sector.

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then alternate method of sector protection described in the :Sector Group Protection and Unprotect" section.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on CE# or WE# will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

POWER-UP SEQUENCE

The MX29LV128M H/L powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

POWER-UP WRITE INHIBIT

If WE#=CE#=VIL and OE#=VIH during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

POWER SUPPLY DE COUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SOFTWARE COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data are latched on rising edge of WE# or CE#, whichever happens first.

TABLE 3. MX29LV128M H/L COMMAND DEFINITIONS

Command		Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycles	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Automatic Select (Note 7)														
Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	C2H				
	Byte	4	AAA	AA	555	55	AAA	90	X00	C2H				
Device ID (Note 8)	Word	4	555	AA	2AA	55	555	90	X01	ID1	X0E	ID2	X0F	ID3
	Byte	4	AAA	AA	555	55	AAA	90	X02	ID1	X1C	ID2	X1E	ID3
Secured Sector Factory Protect (Note 9)	Word	4	555	AA	2AA	55	555	90	X03	see note 9				
	Byte	4	AAA	AA	555	55	AAA	90	X06					
Sector Group Protect Verify (Note 10)	Word	4	555	AA	2AA	55	555	90	(SA)X02	XX00/ XX01				
	Byte	4	AAA	AA	555	55	AAA	90	(SA)X04					
Enter Secured Silicon Sector	Word	3	555	AA	2AA	55	555	88						
	Byte	3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 11)	Word	6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
	Byte	6	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash	Word	1	SA	29										
	Byte	1	SA	29										
Write to Buffer Abort Reset (Note 12)	Word	3	555	AA	2AA	55	555	F0						
	Byte	3	AAA	AA	555	55	AAA	F0						
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 13)		1	XXX	B0										
Program/Erase Resume (Note 14)		1	XXX	30										
CFI Query (Note 15)	Word	1	55	98										
	Byte	1	AA	98										

Legend:
X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happen later.
DDI=Data of device identifier
C2H for manufacture code

PD=Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.
SA=Address of the sector to be erase or verified (in autoselect mode).
Address bits A21-A12 uniquely select any sector.
WBL=Write Buffer Location. Address must be within the same write buffer page as PA.
WC=Word Count. Number of write buffer locations to load minus 1.
BC=Byte Count. Number of write buffer locations to load minus 1.

Notes:
1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or automatic select data, all bus cycles are write operation.
4. Address bits are don't care for unlock and command cycles, except when PA or SA is required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the automatic select mode or if Q5 goes high.
7. The fourth cycle of the automatic select command sequence is a read cycle.
8. The device ID must be read in three cycles. The data is 01h for top boot and 00h for bottom boot.
9. If WP# protects the highest address sectors, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the lowest address sectors, the data is 88h for factory locked and 08h for not factor locked.
10. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
11. The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21(Word Mode) / 37(Byte Mode).
12. Command sequence resets device for next command after aborted write-to-buffer operation.
13. The system may read and program functions in non-erasing sectors, or enter the automatic select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
14. The Erase Resume command is valid only during the Erase Suspend mode.
15. Command is valid when device is ready to read array data or when device is in automatic select mode.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the automatic select mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 2 shows the address and data requirements. This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires VID on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the automatic select mode and return to reading array data.

BYTE/WORD PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 3 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hard-

ware reset immediately terminates the programming operation. The Byte/Word Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}-4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. Q7, Q6, Q5, and Q1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by Q1 = 1, Q7 = DATA# (for the last address location loaded), Q6 = toggle, and Q5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer

programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15us maximum (5 us typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. See Write Operation Status for more information.

SETUP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H, or the sector erase command 30H.

The MX29LV128M H/L contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code. A read cycle with A1=VIL, A0=VIH returns the device code.

AUTOMATIC CHIP/SECTOR ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically pre-program and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 3 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6, Q2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 10 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 9 for timing diagrams.

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later , while the command (data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 50us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is issued during the sector erase operation, the device requires a maximum 20us to suspend the sector erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Erase Resume, program data to, or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV128M H/L is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 4.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code (none)	17	2E	0000
	18	30	0000
Address for secondary algorithm extended query table (none)	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address h (x16)	Address h (x8)	Data h
VCC supply, minimum (2.7V)	1B	36	0027
VCC supply, maximum (3.6V)	1C	38	0036
VPP supply, minimum (none)	1D	3A	0000
VPP supply, maximum (none)	1E	3C	0000
Typical timeout for single word/byte write (2^N us)	1F	3E	0007
Typical timeout for maximum size buffer write (2^N us)	20	40	0007
Typical timeout for individual block erase (2^N ms)	21	42	000A
Typical timeout for full chip erase (2^N ms)	22	44	0000
Maximum timeout for single word/byte write times (2^N X Typ)	23	46	0001
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	48	0005
Maximum timeout for individual block erase times (2^N X Typ)	25	4A	0004
Maximum timeout for full chip erase times (not supported)	26	4C	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address h (x16)	Address h (x8)	Data h
Device size (2^n bytes)	27	4E	0018
Flash device interface code	28	50	0002
	29	52	0000
Maximum number of bytes in multi-byte write = 2^n	2A	54	0005
	2B	56	0000
Number of erase block regions	2C	58	0001
Erase block region 1 information	2D	5A	00FF
[2E,2D] = # of blocks in region -1	2E	5C	0000
[30, 2F] = size in multiples of 256-bytes	2F	5E	0000
	30	60	0001
	31	62	0000
Erase Block Region 2 Information (refer to CFI publication 100)	32	64	0000
	33	66	0000
	34	68	0000
	35	6A	0000
Erase Block Region 3 Information (refer to CFI publication 100)	36	6C	0000
	37	6E	0000
	38	70	0000
	39	72	0000
Erase Block Region 4 Information (refer to CFI publication 100)	3A	74	0000
	3B	76	0000
	3C	78	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "PRI"	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0033
Address sensitive unlock (0=required, 1= not required)	45	8A	0000
Erase suspend (2= to read and write)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0001
Temporary sector unprotect (1=supported)	48	90	0001
Sector protect/unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode type (0=not supported)	4B	96	0000
Page mode type (0=not supported)	4C	98	0001
ACC (Acceleration) Supply Minimum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4D	9A	00B5
ACC (Acceleration) Supply Maximum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4E	9C	00C5
Top/Bottom Boot Sector Flag 02h=Bottom Boot Device, 03h=Top Boot Device 04h=uniform sectors bottom WP# protect, 05h=uniform sectors top WP# protect	4F	9E	0004/ 0005
Program Suspend 00h=Not Supported, 01h=Supported	50	A0	0001

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY#. Table 5 and the following subsections describe the functions of these bits. Q7, RY/BY#, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table 5. Write Operation Status

Status		Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Byte/Word Program in Auto Program Algorithm		Q7#	Toggle	0	N/A	No Toggle	0	0
Auto Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	N/A	1
	Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Q7#	Toggle	0	N/A	N/A	N/A	0
Program Suspend	Program-Suspended Read (Program-Suspended Sector)	Invalid (not allowed)						1
	Program-Suspended Read (Non-Program-Suspended Sector)	Data						1
Write-to-Buffer	Busy	Q7#	Toggle	0	N/A	N/A	0	0
	Abort	Q7#	Toggle	0	N/A	N/A	1	0

Notes:
1. Q5 switches to "1" when an Word/Byte Program, Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on Q5 for more information.
2. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. Q1 switches to "1" when the device has aborted the write-to-buffer operation.

Q7: Data# Polling

The Data# Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data# Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data# Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE#) is asserted low.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles for 100us and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by com-

parison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 5 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5:Program/Erase Timing

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte/word programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1". Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, Q5 produces a "1".

Q3:Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or

Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

If the time between additional erase commands from the system can be less than 50us, the system need not to monitor Q3.

Q1: Write-to-Buffer Abort

Q1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions Q1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

RY/BY#:READY/BUSY OUTPUT

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to VCC .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, OE#, and

RESET# (Note 2) . . . .-0.5 V to +12.5 V

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20ns.
2. Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0° C to +70° C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40° C to +85° C

VCC Supply Voltages

VCC for full voltage range. . . . . +2.7 V to 3.6 V

VCC for regulated voltage range. . . . . +3.0 V to 3.6 V

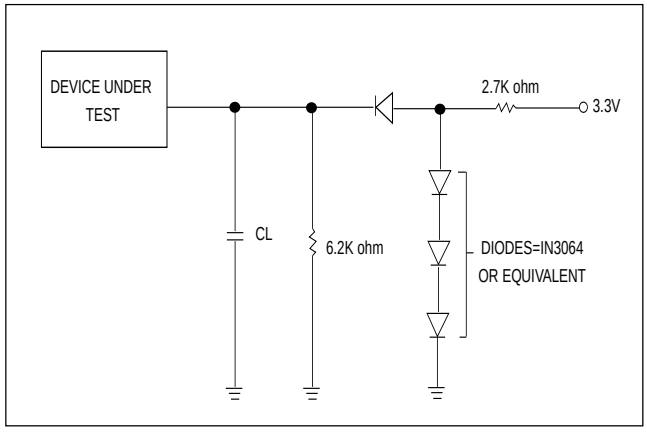
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS TA=-40° C to 85° C, VCC=2.7V~3.6V (VCC=3.0V~3.6V for 90R)

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
I LI	Input Load Current (Note 1)	VIN = VSS to VCC , VCC = VCC max				±1.0	uA
I LIT	A9 Input Leakage Current	VCC=VCC max; A9 = 12.5V				35	uA
I LO	Output Leakage Current	VOUT = VSS to VCC , VCC = VCC max				±1.0	uA
ICC1	VCC Initial Read Current (Notes 2,3)	CE# = VIL, OE# = VIH	10 MHz		35	50	mA
			5 MHz		18	25	mA
			1 MHz		5	20	mA
ICC2	VCC Intra-Page Read Current (Notes 2,3)	CE# = VIL , OE# = VIH	10 MHz		5	20	mA
			40 MHz		10	40	mA
ICC3	VCC Active Write Current (Notes 2,4,6)	CE# = VIL , OE# = VIH			50	60	mA
ICC4	VCC Standby Current (Note 2)	CE#, RESET# = VCC ±0.3V WP# = VIH			20	50	uA
ICC5	VCC Reset Current (Note 2)	RESET# =VSS ±0.3V WP# = VIH			20	50	uA
ICC6	Automatic Sleep Mode (Notes 2,5)	VIL = VSS ±0.3V, VIH = VCC ±0.3V, WP# = VIH			20	50	uA
VIL	Input Low Voltage			-0.5		0.8	V
VIH	Input High Voltage			0.7xVCC		VCC+0.5	V
VHH	Voltage for ACC Program Acceleration	VCC = 2.7V ~ 3.6V		11.5	12.0	12.5	V
VID	Voltage for Autoselect and Temporary Sector Unprotect	VCC = 3.0 V ±10%		11.5	12.0	12.5	V
VOL	Output Low Voltage	IOL= 4.0mA,VCC=VCC min				0.45	V
VOH1	Output High Voltage	IOH=-2.0mA,VCC=VCC min		0.85VCC			V
VOH2		IOH=-100uA,VCC=VCC min		VCC-0.4			V
VLKO	Low VCC Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:
1. On the WP#/ACC pin only, the maximum input load current when WP# = VIL is ±5.0uA.
2. Maximum ICC specifications are tested with VCC = VCC max.
3. The ICC current listed is typically is less than 2 mA/MHz, with OE# at VIH. Typical specifications are for VCC = 3.0V.
4. ICC active while Embedded Erase or Embedded Program is in progress.
5. Automatic sleep mode enables the low power mode when addresses remain stable for t ACC + 30 ns.
6. Not 100% tested.
7. A9=12.5V when TA=0° C to 85° C, A9=12V when when TA=-40° C to 0° C.

SWITCHING TEST CIRCUITS



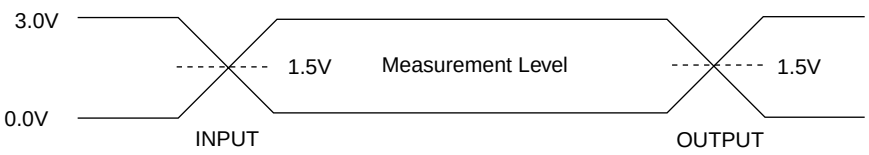
TEST SPECIFICATIONS

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, CL (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0-3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State(High Z)

SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

Read-Only Operations TA=-40° C to 85° C, VCC=2.7V~3.6V (VCC=3.0V~3.6V for 90R)

Parameter Std.	Description		Test Setup		Speed Options		Unit
					90R	100	
tRC	Read Cycle Time (Note 1)			Min	90	100	ns
tACC	Address to Output Delay		CE#, OE#=VIL	Max	90	100	ns
tCE	Chip Enable to Output Delay		OE#=VIL	Max	90	100	ns
tPACC	Page Access Time			Max	25	25	ns
tOE	Output Enable to Output Delay			Max	35	35	ns
tDF	Chip Enable to Output High Z (Note 1)			Max	16		ns
tDF	Output Enable to Output High Z (Note 1)			Max	16		ns
tOH	Output Hold Time From Address, CE# or OE#, whichever Occurs First			Min	0		ns
tOEH	Output Enable Hold Time (Note 1)	Read		Min	35		ns
		Toggle and Data# Polling		Min	10		ns

Notes:
1. Not 100% tested.
2. See SWITCHING TEST CIRCUITS and TEST SPECIFICATIONS TABLE for test specifications.

Figure 1. READ TIMING WAVEFORMS

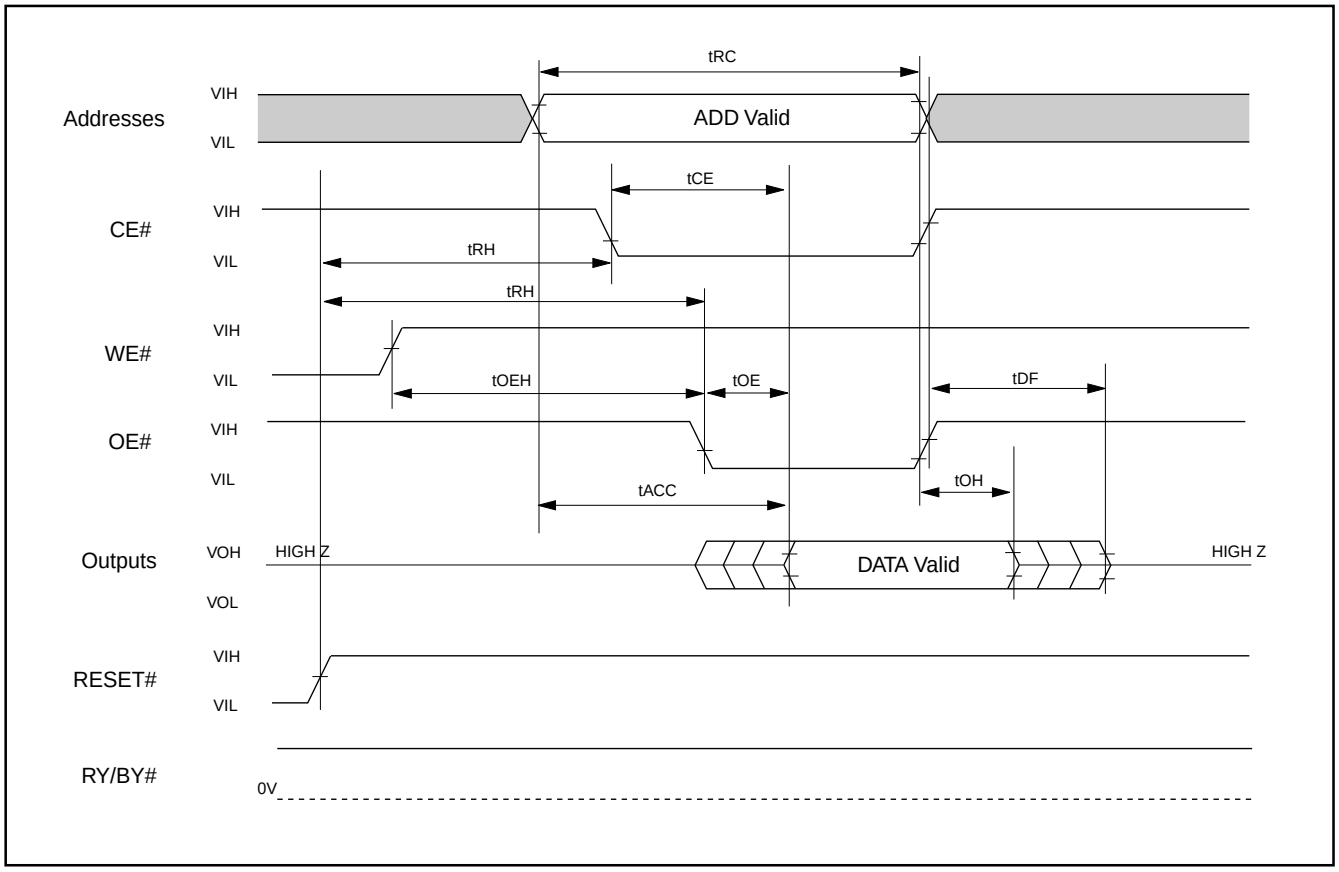
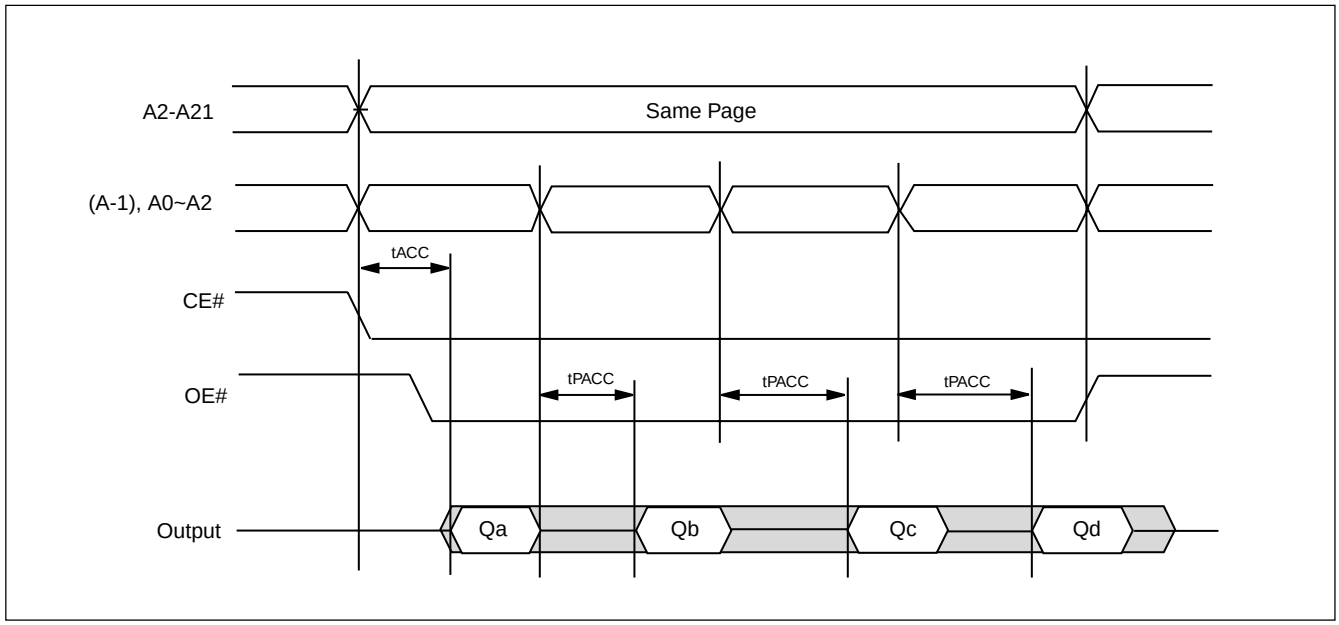


Figure 2. PAGE READ TIMING WAVEFORMS

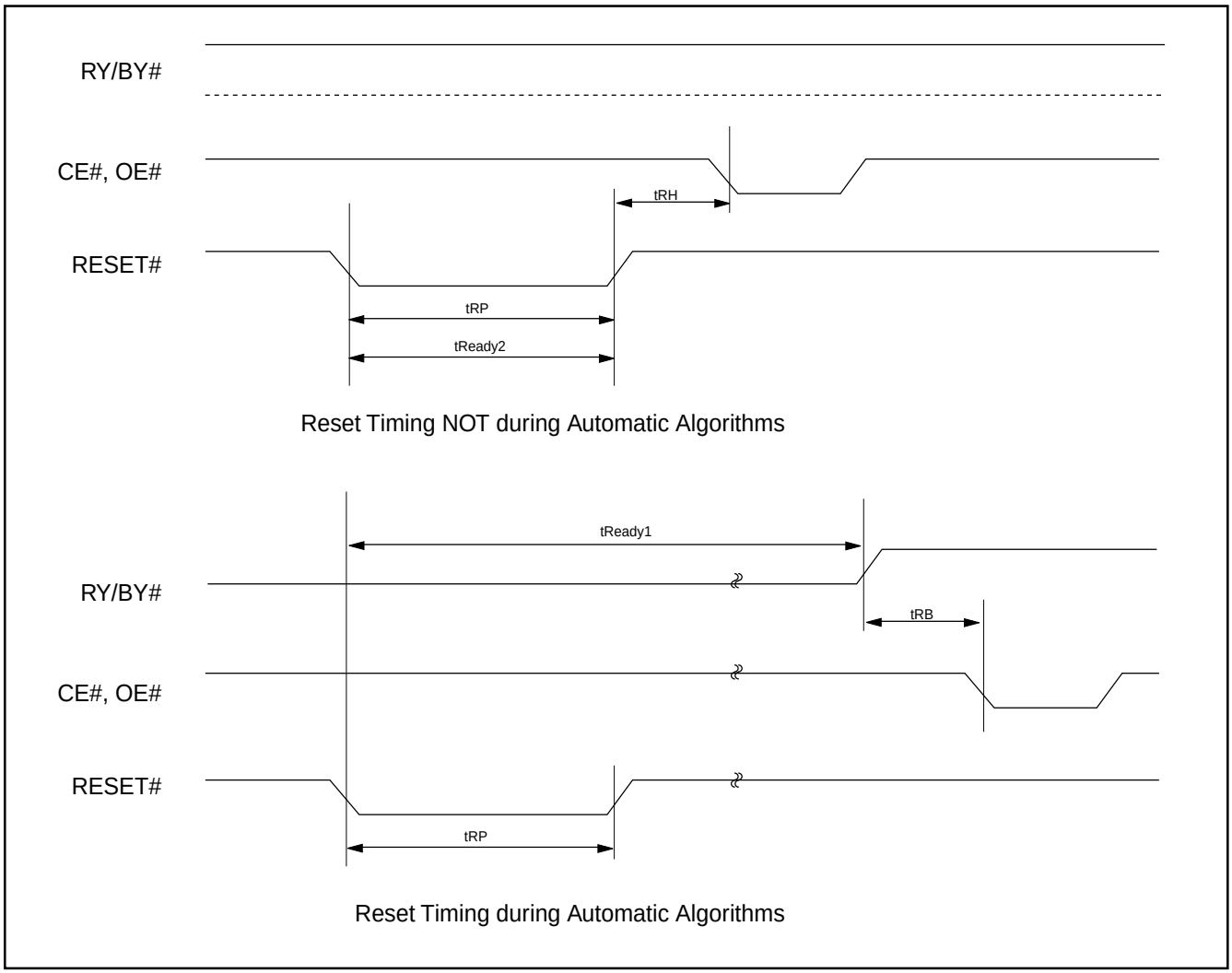


AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET# PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET# High Time Before Read (See Note)	MIN	50	ns
tRB	RY/BY# Recovery Time(to CE#, OE# go low)	MIN	0	ns
tRPD	RESET# Low to Standby Mode	MIN	20	us

Note:Not 100% tested

Figure 3. RESET# TIMING WAVEFORM



AC CHARACTERISTICS

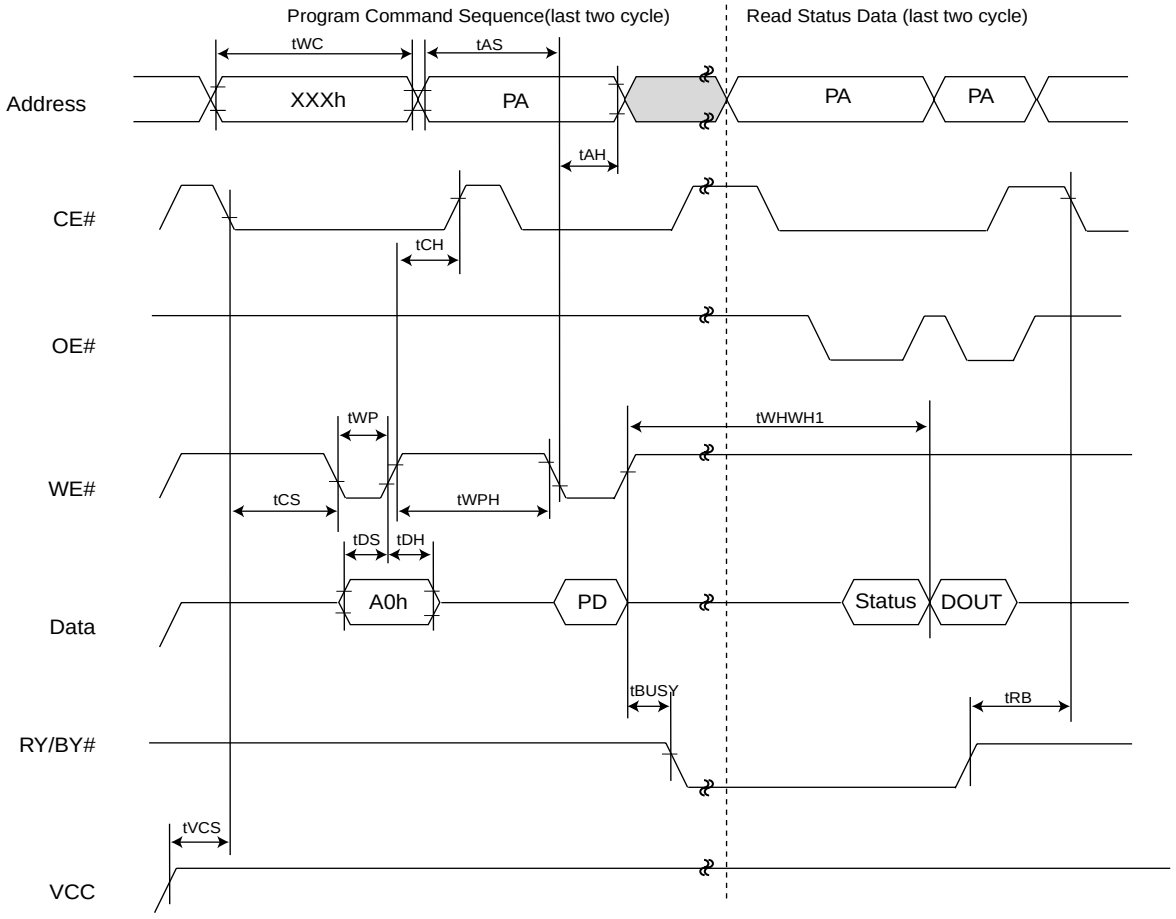
Erase and Program Operations TA=-40° C to 85° C, VCC=2.7V~3.6V (VCC=3.0V~3.6V for 90R)

Parameter Std.	Description			Speed Options 90R	Speed Options 100	Unit
tWC	Write Cycle Time (Note 1)		Min	90	100	ns
tAS	Address Setup Time		Min	0		ns
tASO	Address Setup Time to OE# low during toggle bit polling		Min	15		ns
tAH	Address Hold Time		Min	45		ns
tAHT	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0		ns
tDS	Data Setup Time		Min	35		ns
tDH	Data Hold Time		Min	0		ns
tCEPH	CE# High During Toggle Bit Polling		Min	20		ns
tOEPH	Output Enable High during toggle bit polling		Min	20		ns
tGHWL	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
tGHEL	Read Recovery Time Before Write		Min	0		ns
tCS	CE# Setup Time		Min	0		ns
tCH	CE# Hold Time		Min	0		ns
tWP	Write Pulse Width		Min	35		ns
tWPH	Write Pulse Width High		Min	30		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)		Typ	240		us
	Single Word/Byte Program Operation (Notes 2,5)	Byte	Typ	60		us
		Word	Typ	60		us
	Accelerated Single Word/Byte Programming Operation (Notes 2,5)	Byte	Typ	54		us
		Word	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	0.5		sec
tVCS	VCC Setup Time (Note 1)		Min	50		us
tRB	Write Recovery Time from RY/BY#		Min	0		ns
tBUSY	Program/Erase Valid to RY/BY# Delay		Min	90	100	ns
tVHH	VHH Rise and Fall Time (Note 1)		Min	250		ns
tPOLL	Program Valid Before Status Polling (Note 6)		Max	4		us

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-16 words/1-32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC PROGRAM TIMING WAVEFORMS



Note :
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

Figure 5. ACCELERATED PROGRAM TIMING DIAGRAM

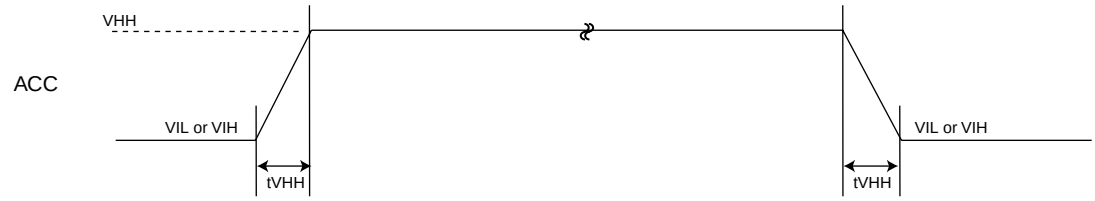


Figure 6. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

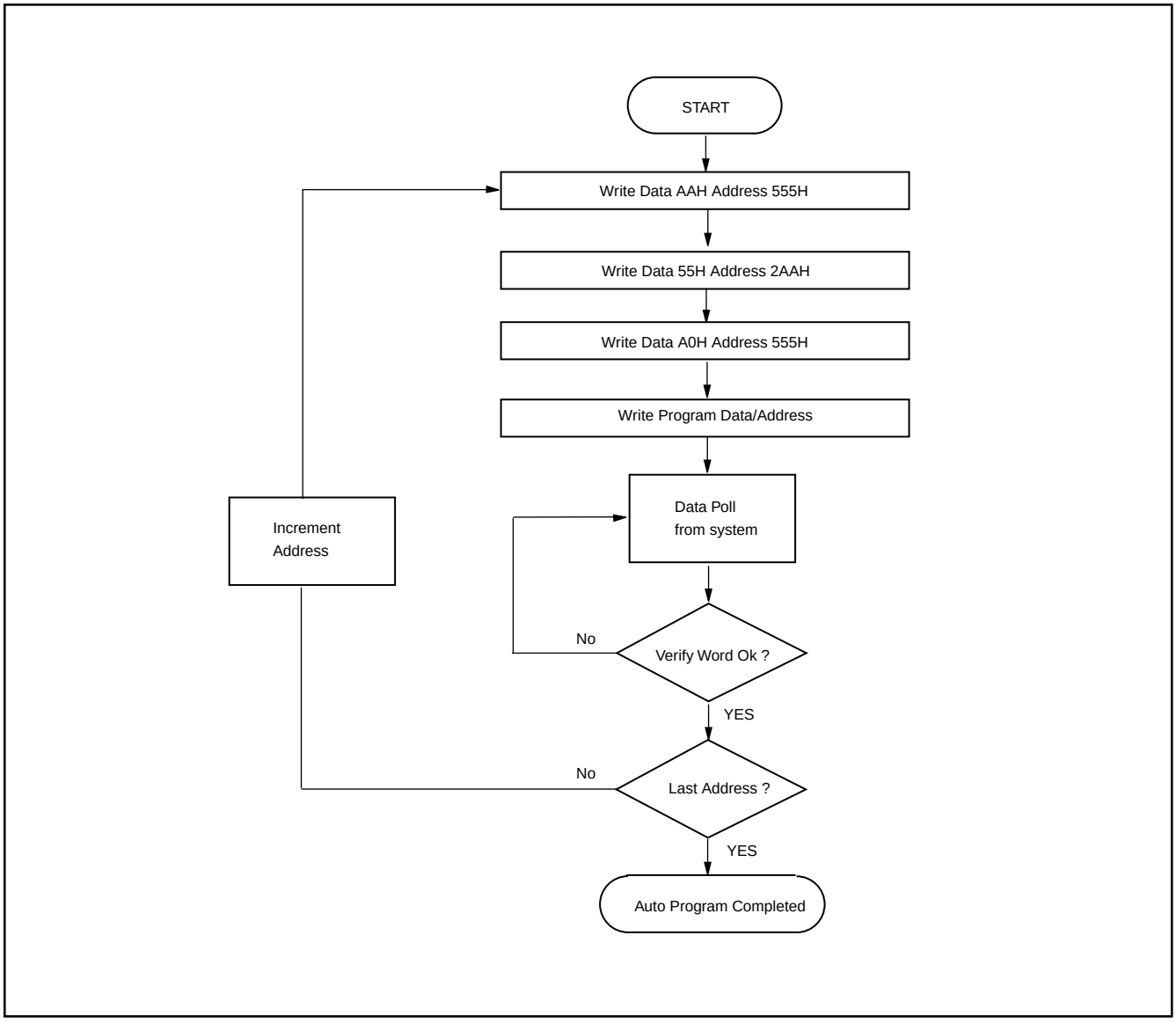
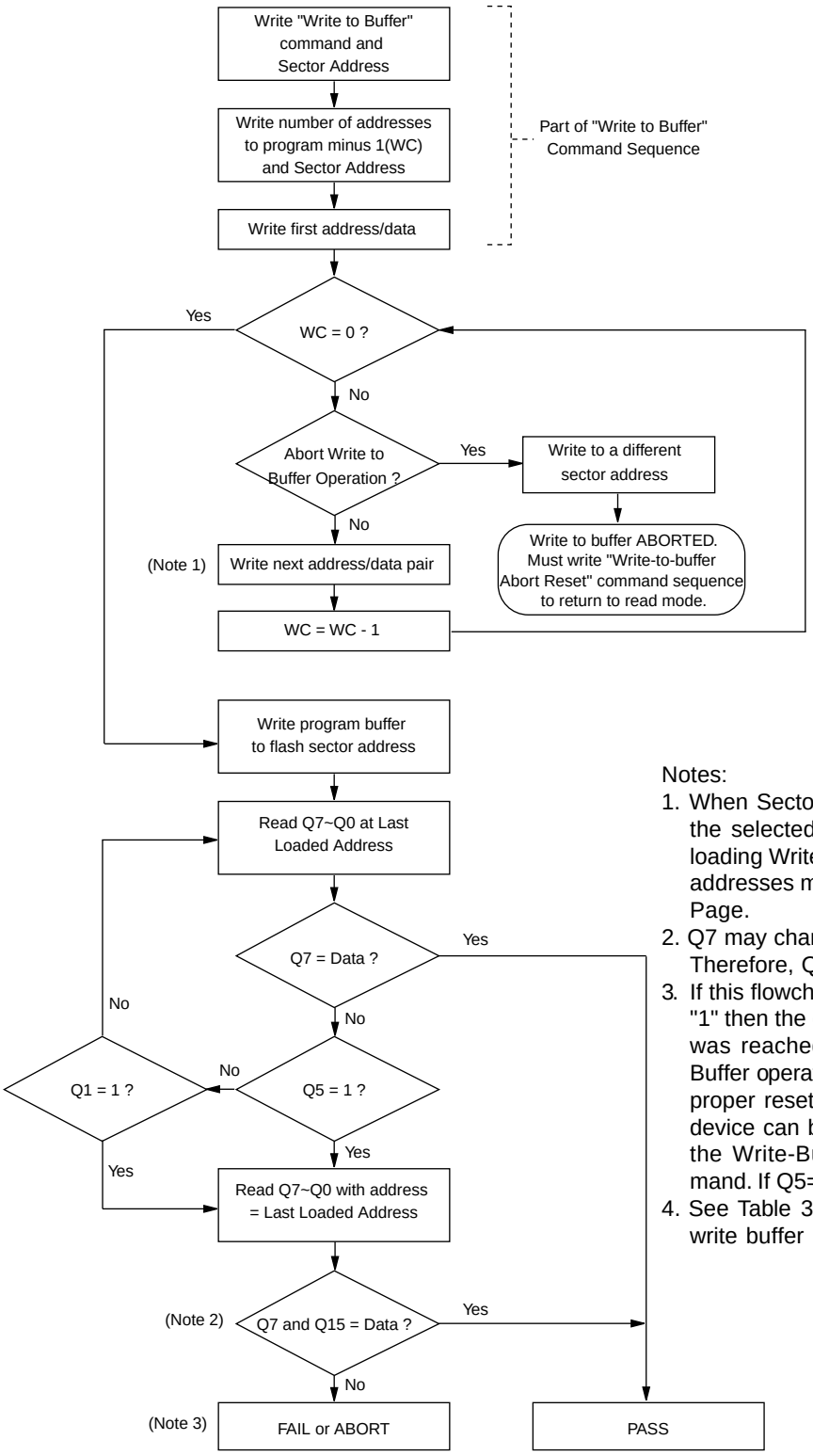


Figure 7. WRITE BUFFER PROGRAMMING ALGORITHM FLOWCHART



Notes:

1. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.
2. Q7 may change simultaneously with Q5. Therefore, Q7 should be verified.
3. If this flowchart location was reached because Q5= "1" then the device FAILED. If this flowchart location was reached because Q1="1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If Q1=1, write the Write-Buffer-Programming-Abort-Reset command. If Q5=1, write the Reset command.
4. See Table 3 for command sequences required for write buffer programming.

Figure 8. PROGRAM SUSPEND/RESUME FLOWCHART

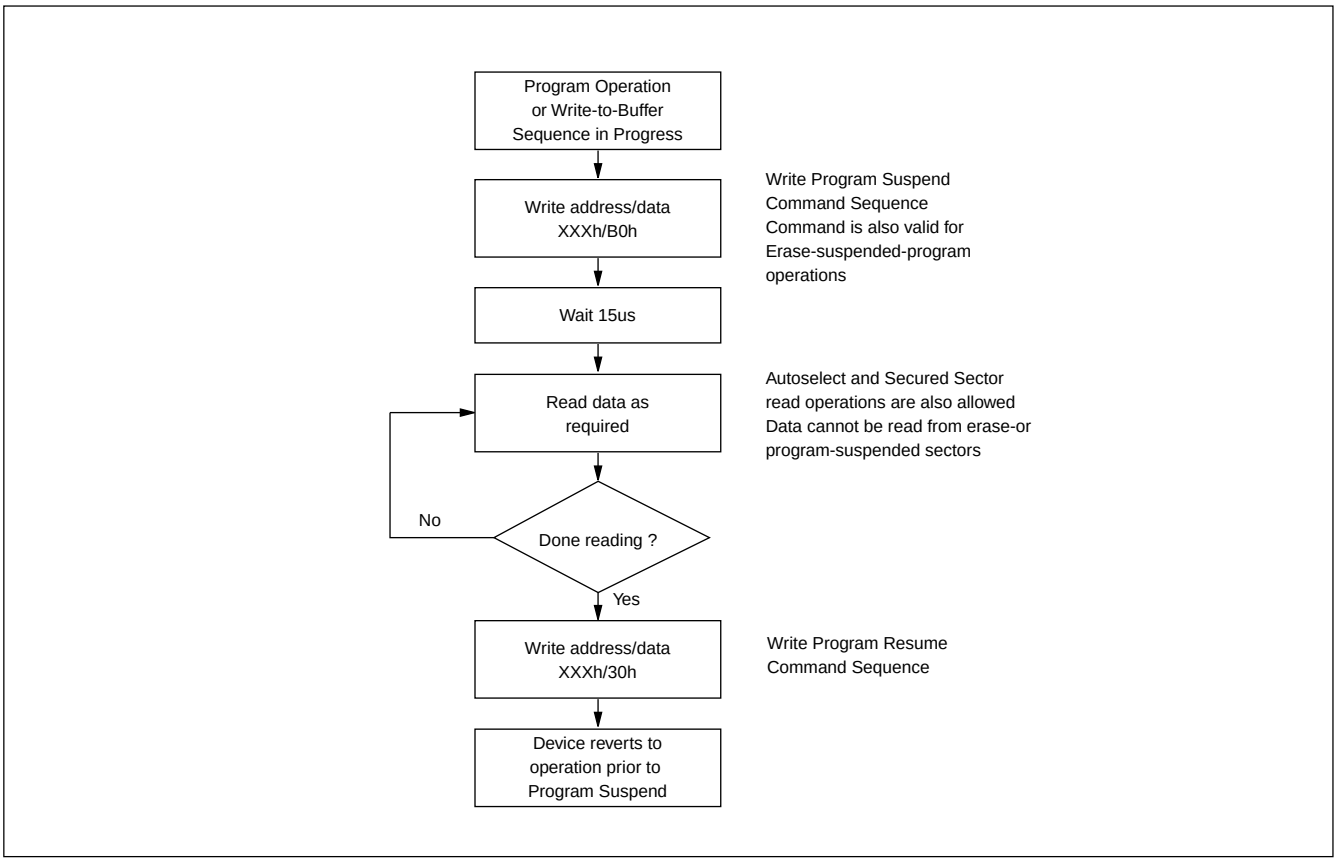
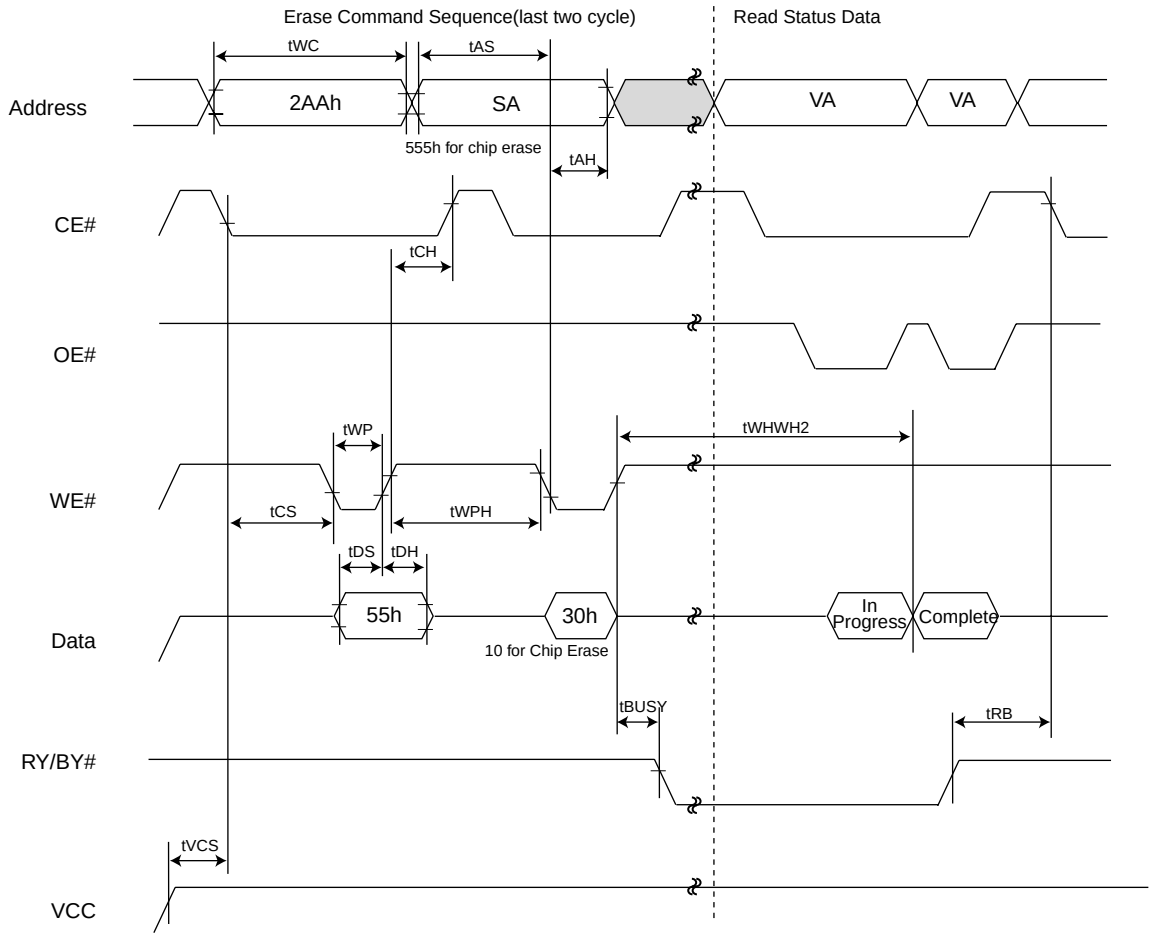


Figure 9. AUTOMATIC CHIP/SECTOR ERASE TIMING WAVEFORM



Note :

1.SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Figure 10. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

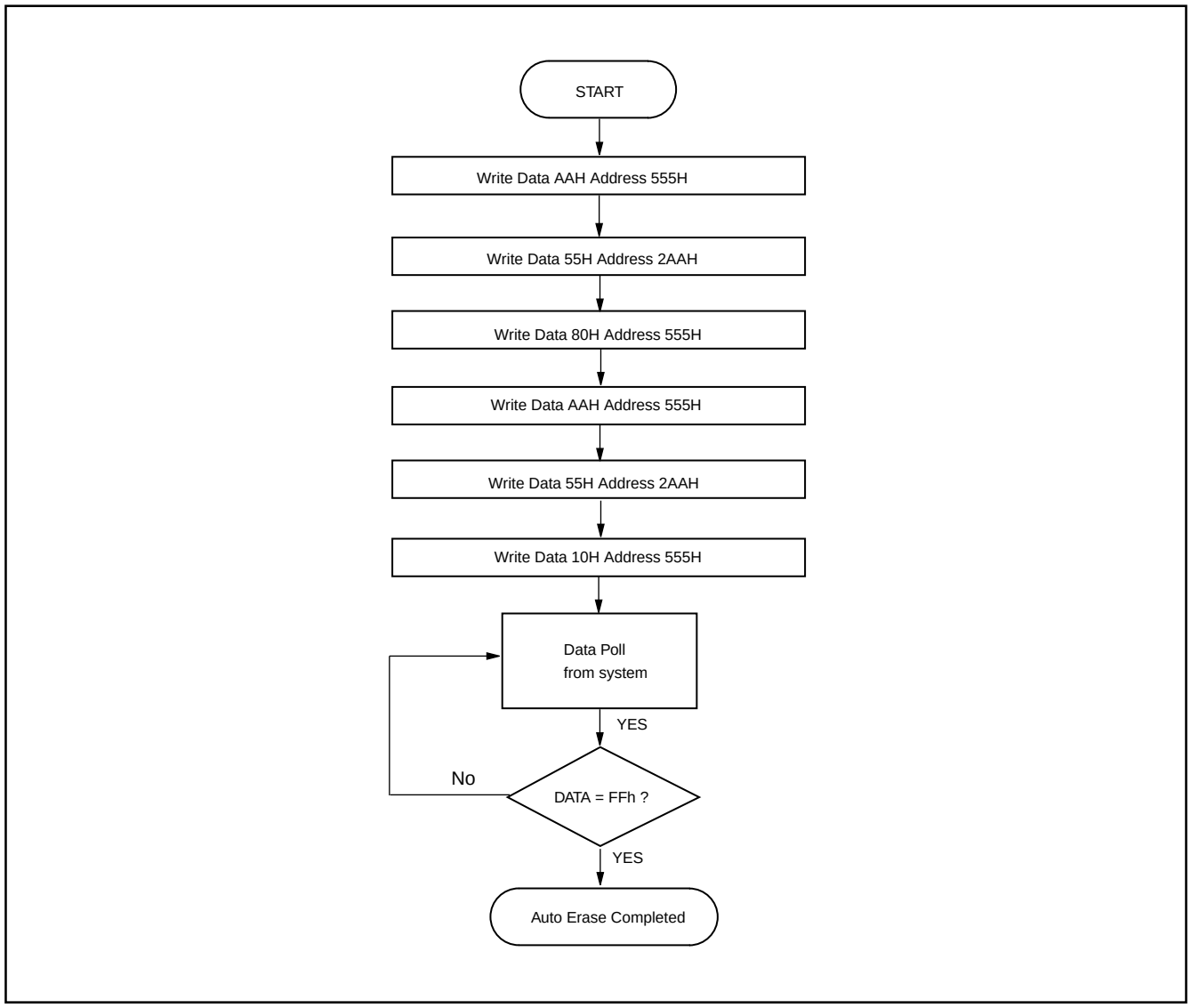


Figure 11. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

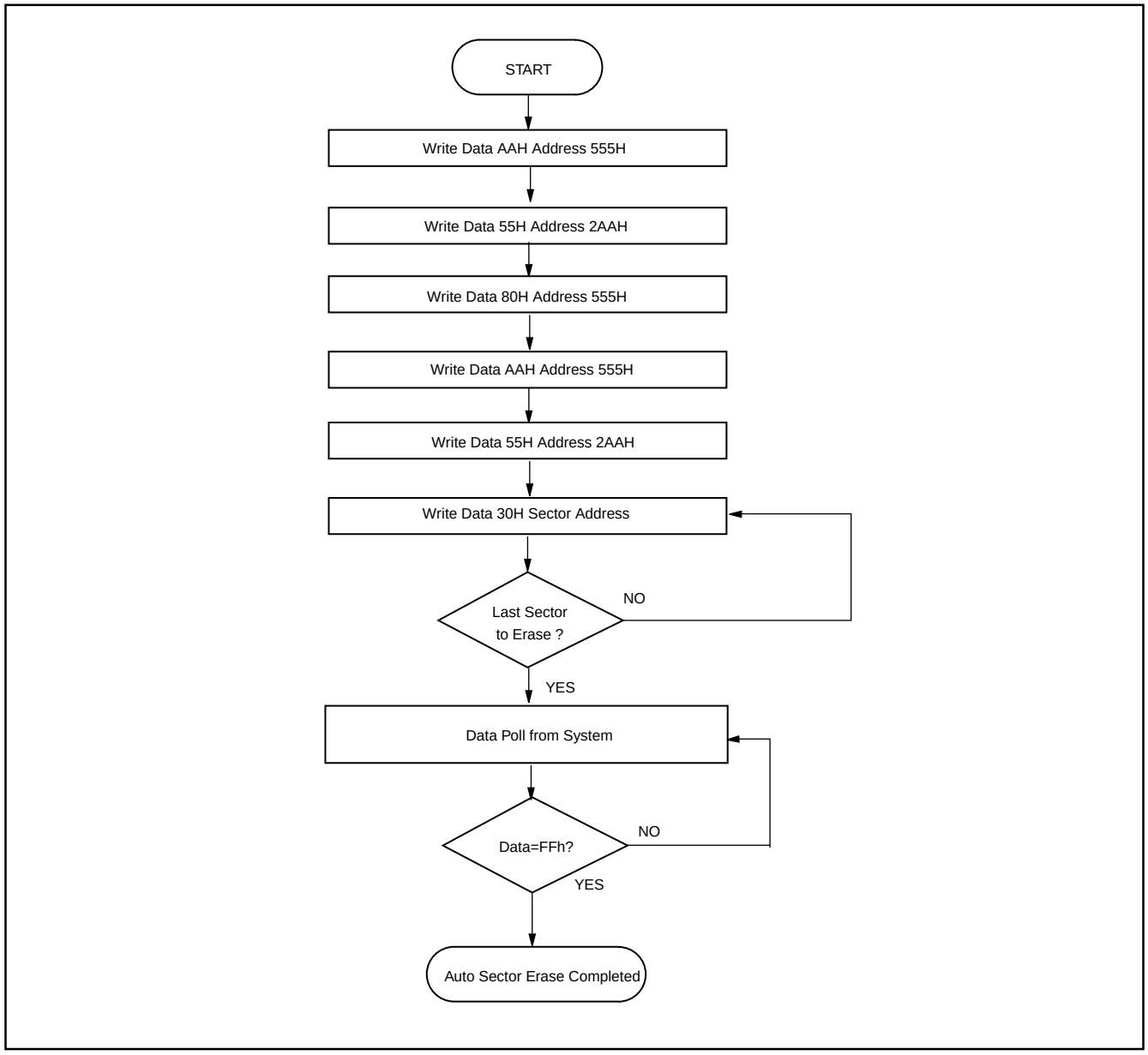
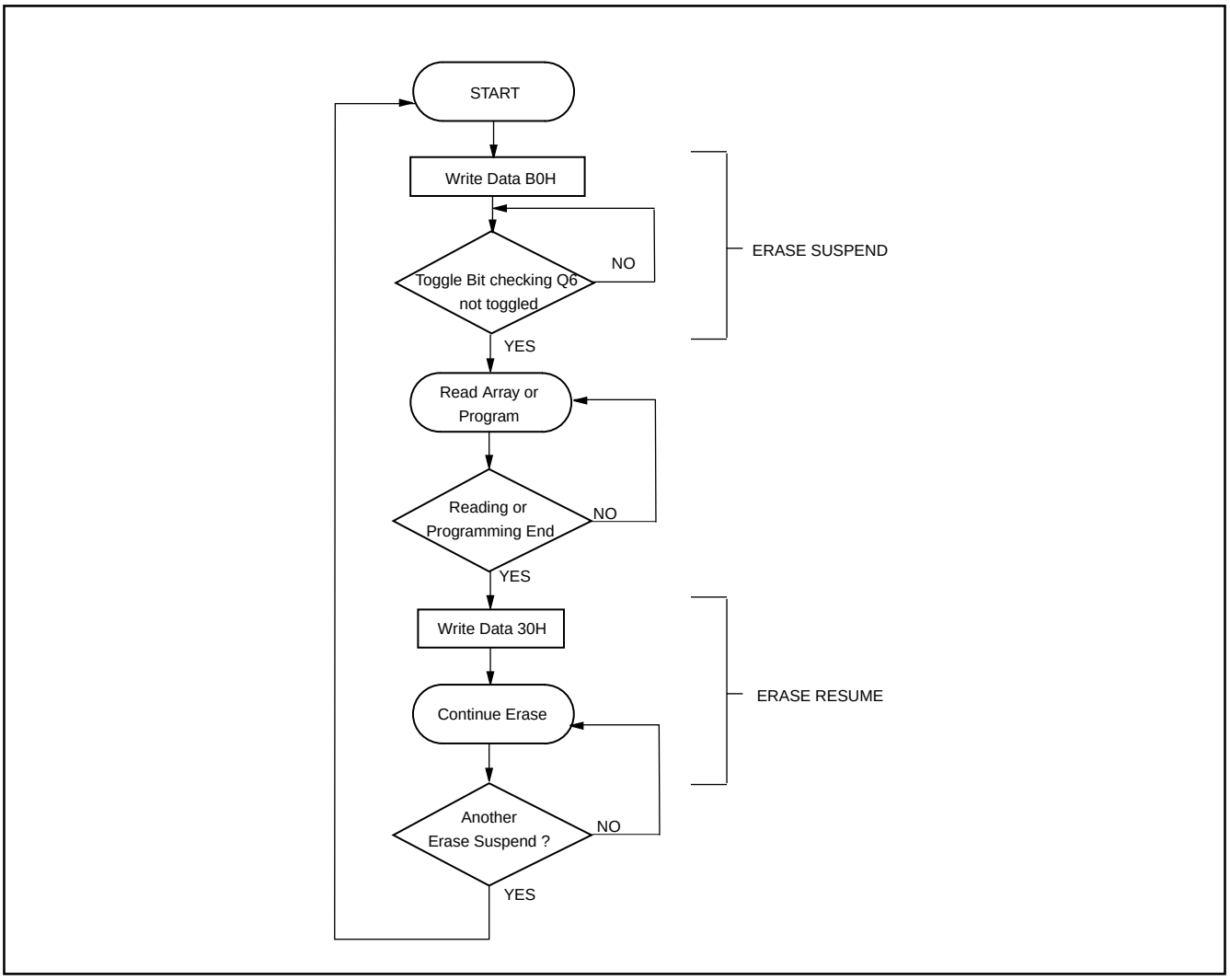


Figure 12. ERASE SUSPEND/RESUME FLOWCHART



AC CHARACTERISTICS

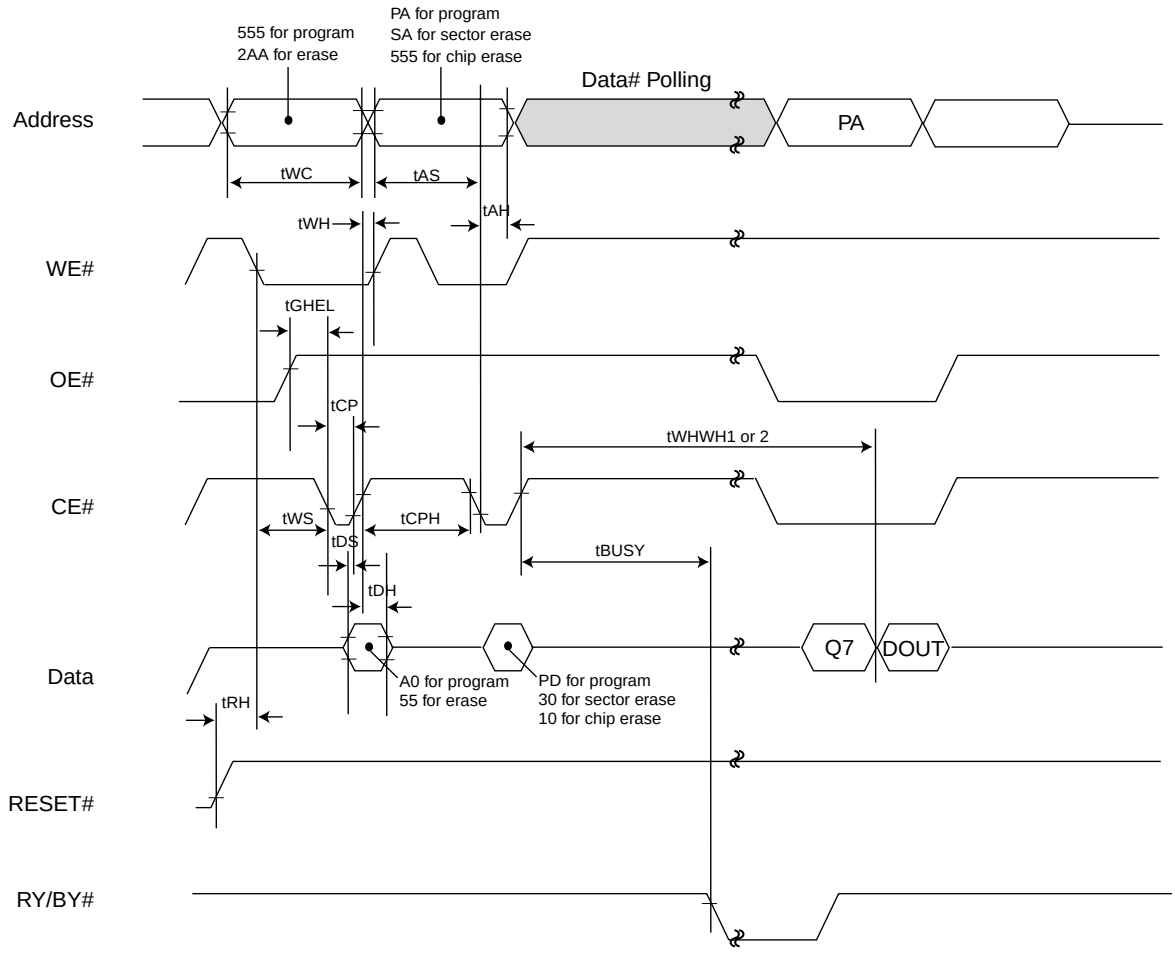
Alternate CE# Controlled Erase and Program Operations

TA=-40° C to 85° C, VCC=2.7V~3.6V (VCC=3.0V~3.6V for 90R)

Parameter Std.	Description			Speed Options 90R	Speed Options 100	Unit
tWC	Write Cycle Time (Note 1)		Min	90	100	ns
tAS	Address Setup Time		Min	0		ns
tAH	Address Hold Time		Min	45		ns
tDS	Data Setup Time		Min	35		ns
tDH	Data Hold Time		Min	0		ns
tGHEL	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
tWS	WE# Setup Time		Min	0		ns
tWH	WE# Hold Time		Min	0		ns
tCP	CE# Pulse Width		Min	35		ns
tCPH	CE# Pulse Width High		Min	25		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)		Typ	240		us
	Single Word/Byte Program Operation (Notes 2,5)	Byte	Typ	60		us
		Word	Typ	60		us
	Accelerated Single Word/Byte Programming Operation (Notes 2,5)	Byte	Typ	54		us
		Word	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	0.5		sec
tRH	RESET HIGH Time Before Write (Note 1)		Min	50		ns
tPOLL	Program Valid Before Status Polling (Note 6)		Max	4		us

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-16 words/1-32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

Figure 13. CE# CONTROLLED PROGRAM TIMING WAVEFORM

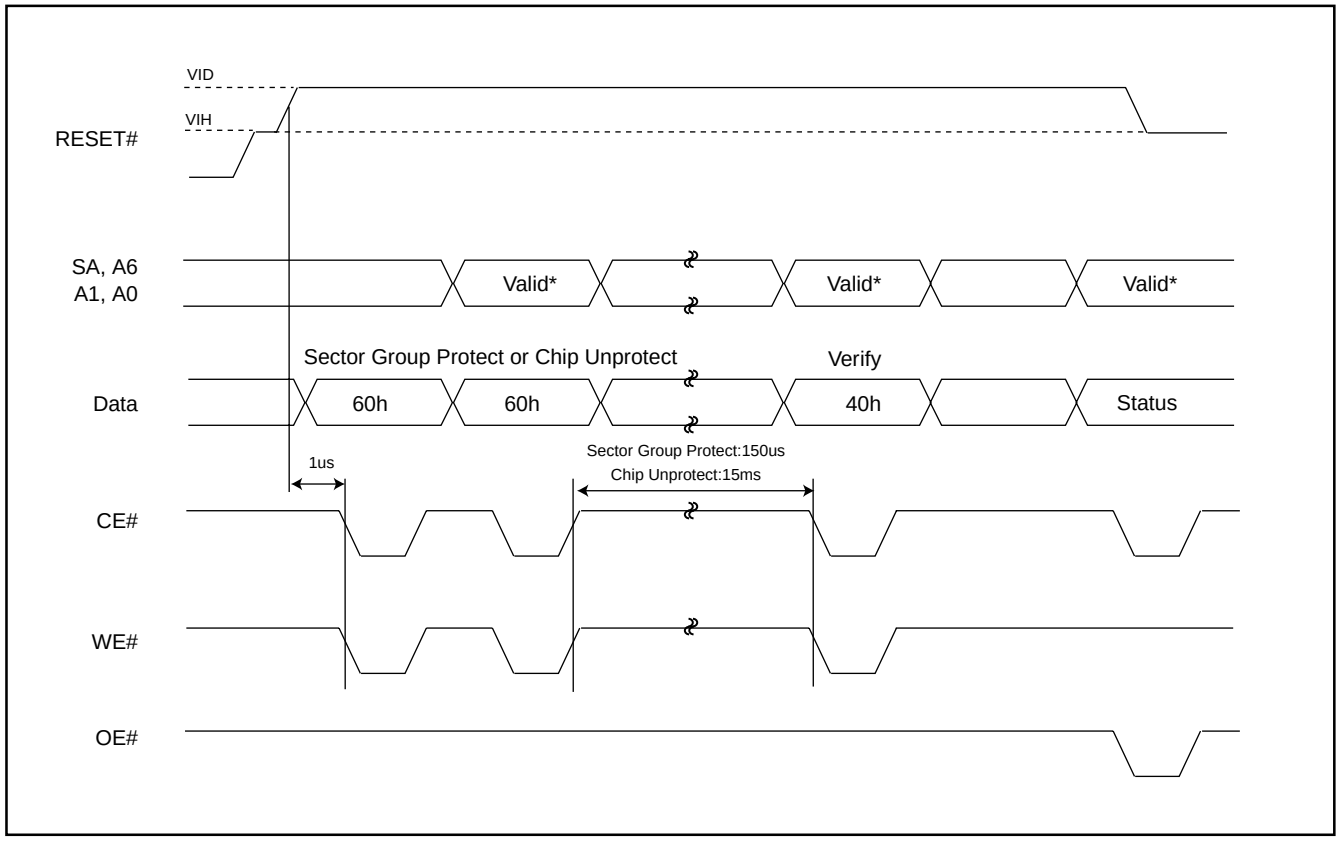


NOTES:

1.PA=Program Address, PD=Program Data, DOUT=Data Out, Q7=complement of data written to device.
2.Figure indicates the last two bus cycles of the command sequence.

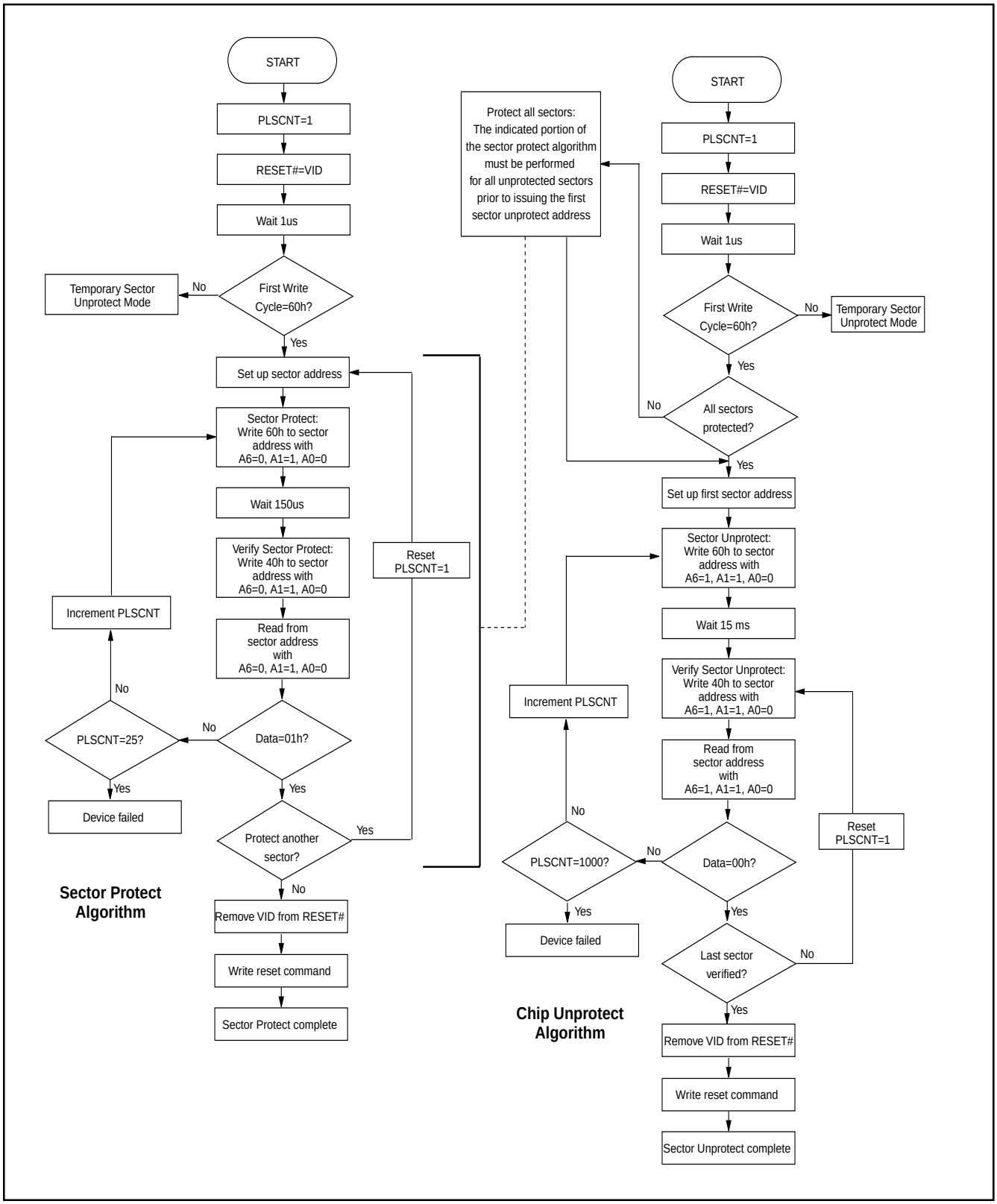
SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 14. Sector Group Protect / Chip Unprotect Waveform (RESET# Control)



Note: For sector group protect A6=0, A1=1, A0=0. For chip unprotect A6=1, A1=1, A0=0

Figure 15. IN-SYSTEM SECTOR GROUP PROTECT/CHIP UNPROTECT ALGORITHMS WITH RESET#=VID



AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVLHT	Voltage transition time	Min.	4	us
tWPP1	Write pulse width for sector group protect	Min.	100	ns
tOESP	OE# setup time to WE# active	Min.	4	us

Figure 16. SECTOR GROUP PROTECT TIMING WAVEFORM (A9, OE# Control)

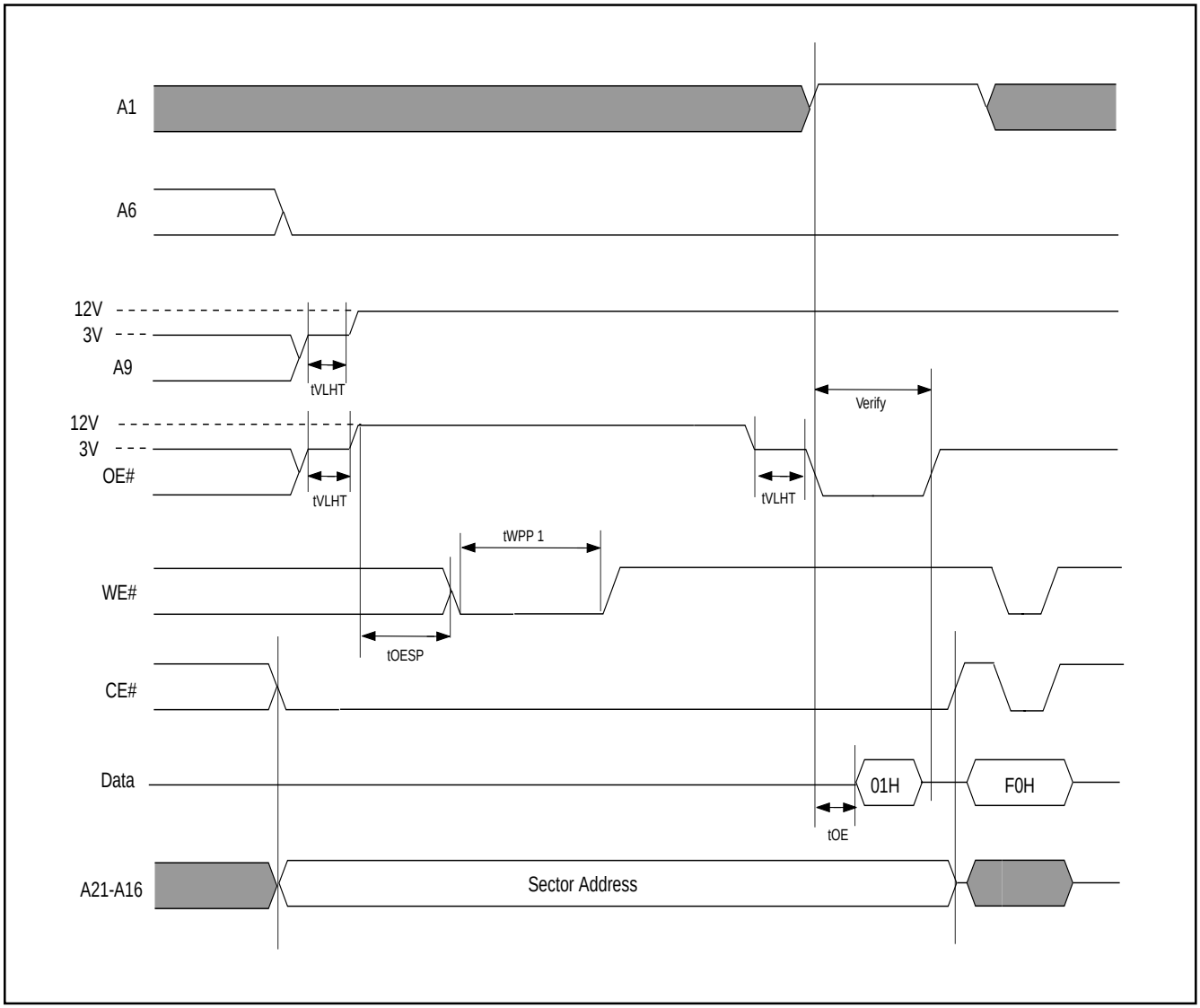


Figure 17. SECTOR GROUP PROTECTION ALGORITHM (A9, OE# Control)

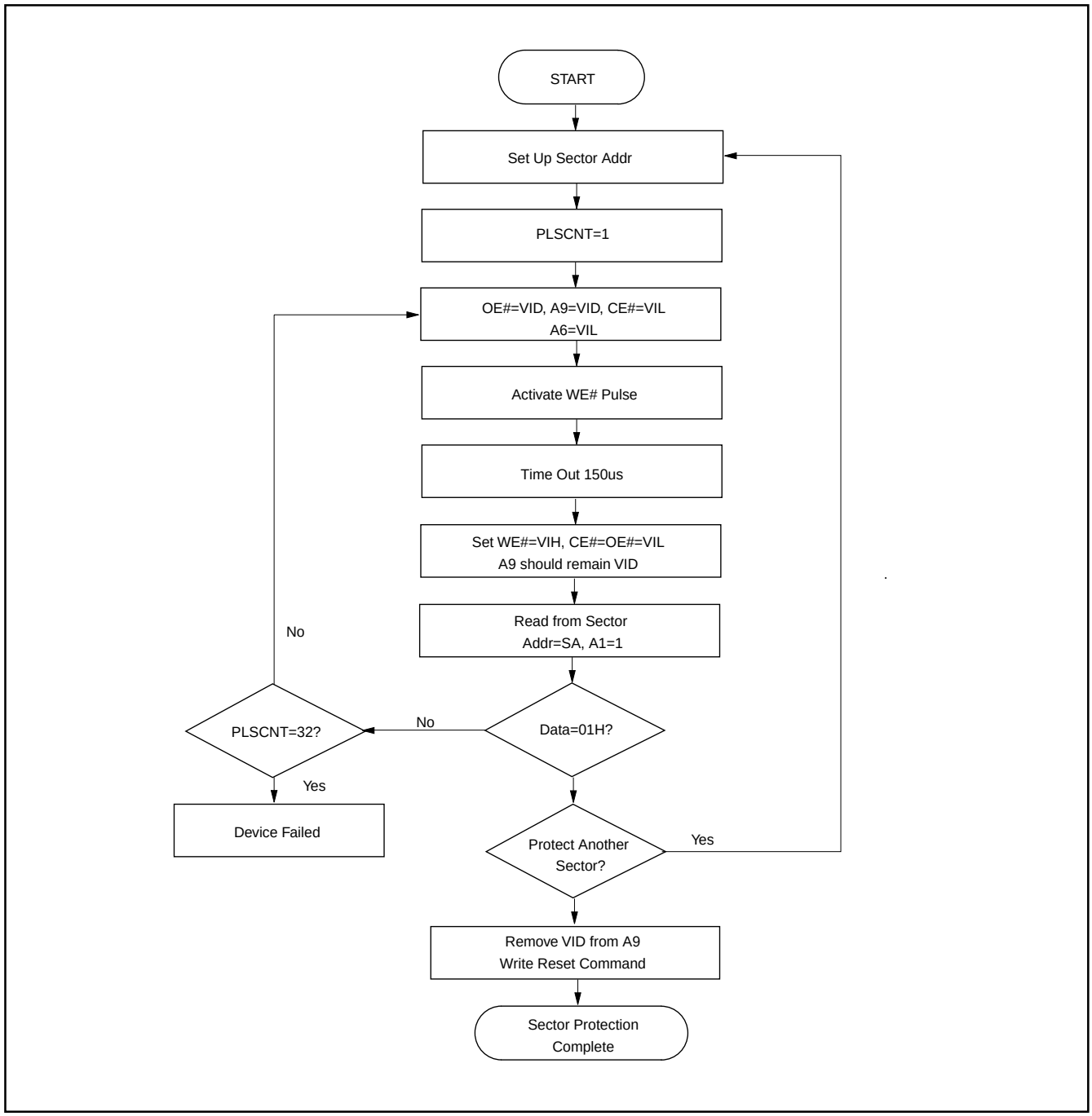


Figure 18. CHIP UNPROTECT TIMING WAVEFORM (A9, OE# Control)

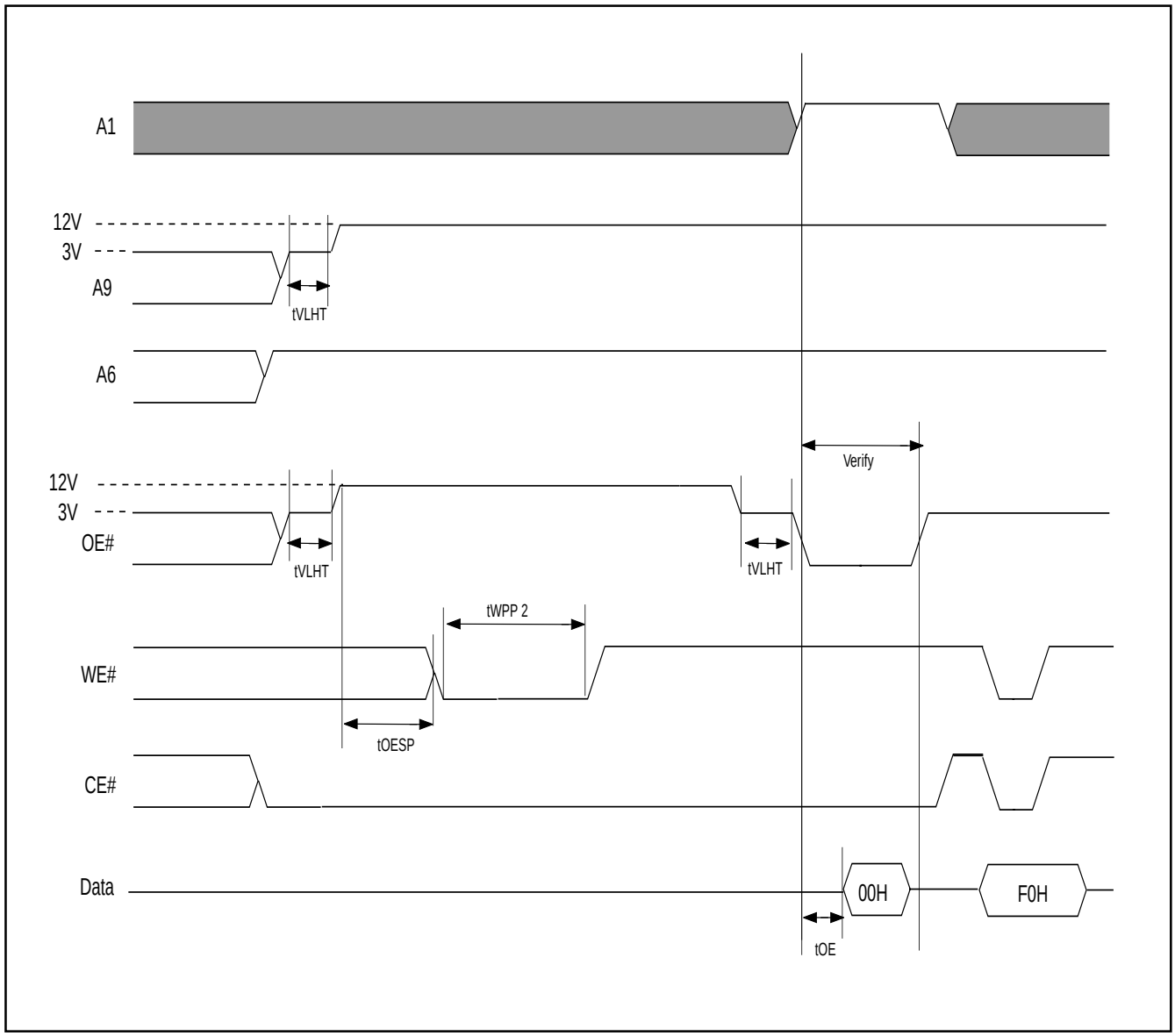
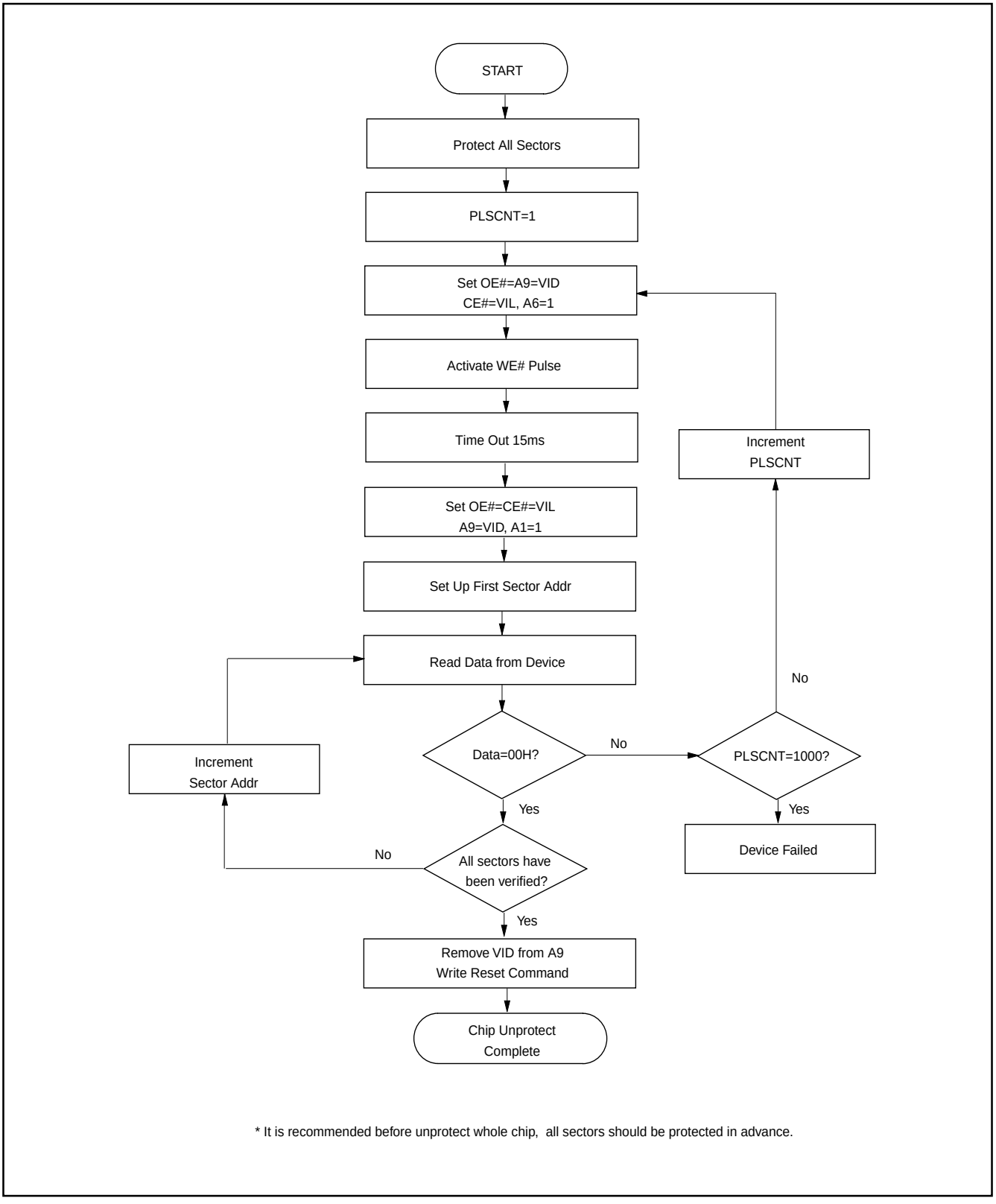


Figure 19. CHIP UNPROTECT FLOWCHART (A9, OE# Control)



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVIDR	VID Rise and Fall Time (see Note)	Min	500	ns
tRSP	RESET# Setup Time for Temporary Sector Unprotect	Min	4	us
tRRB	RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotect	Min	4	us

Figure 20. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

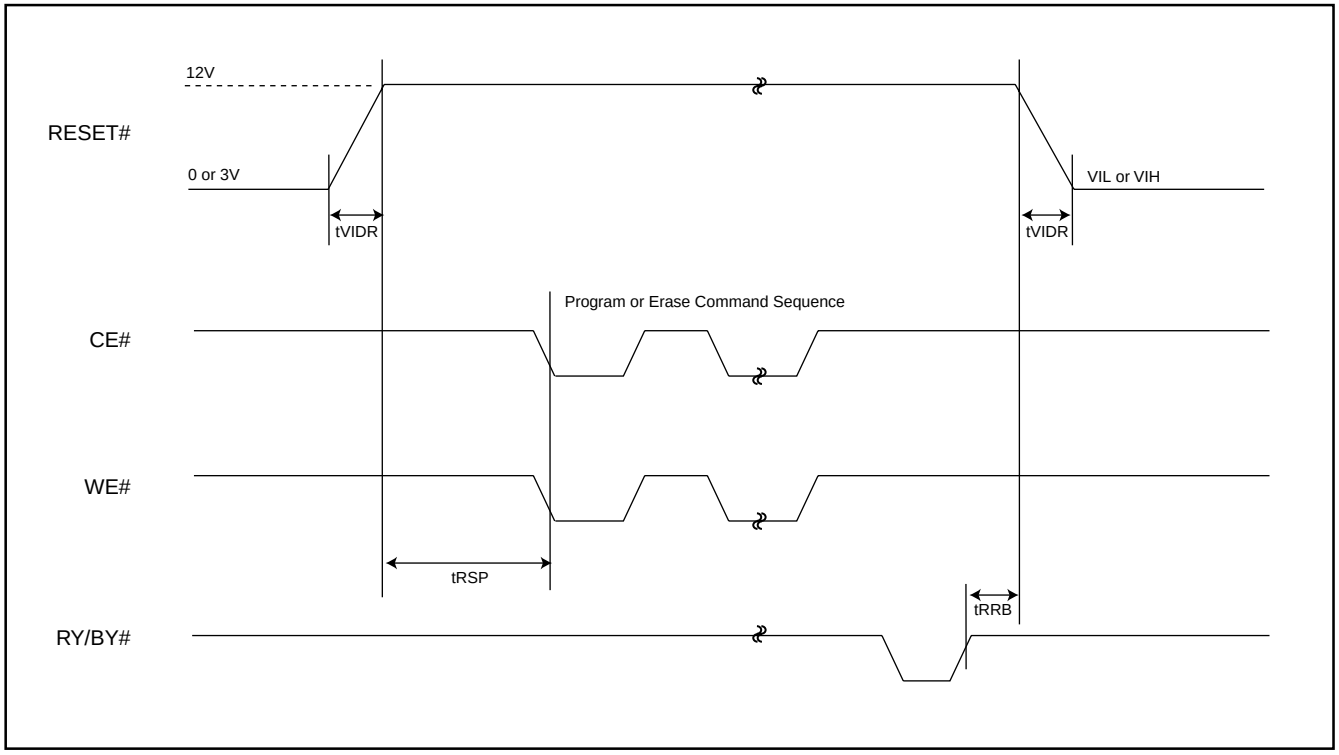
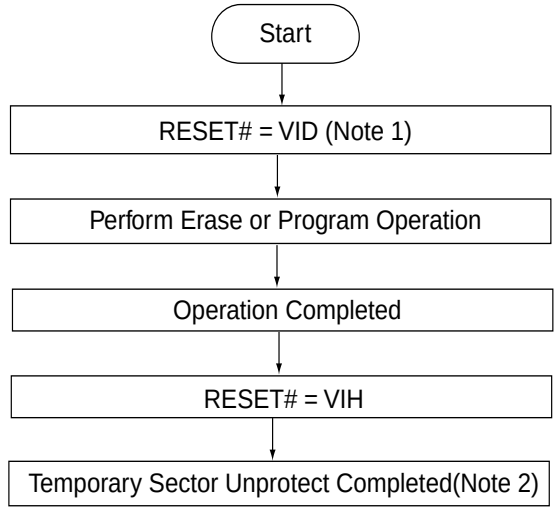


Figure 21. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

2. All previously protected sectors are protected again.

Figure 22. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART

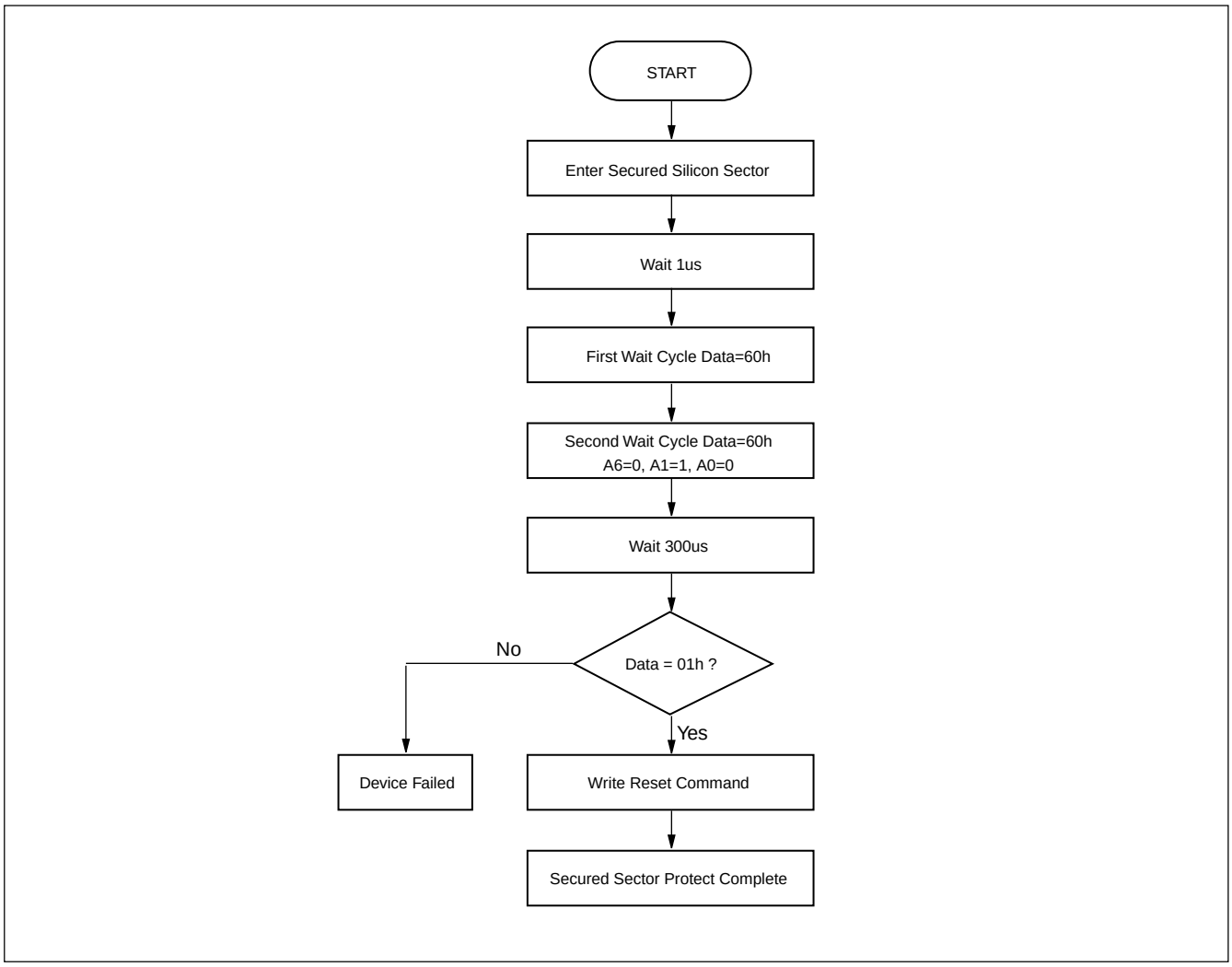
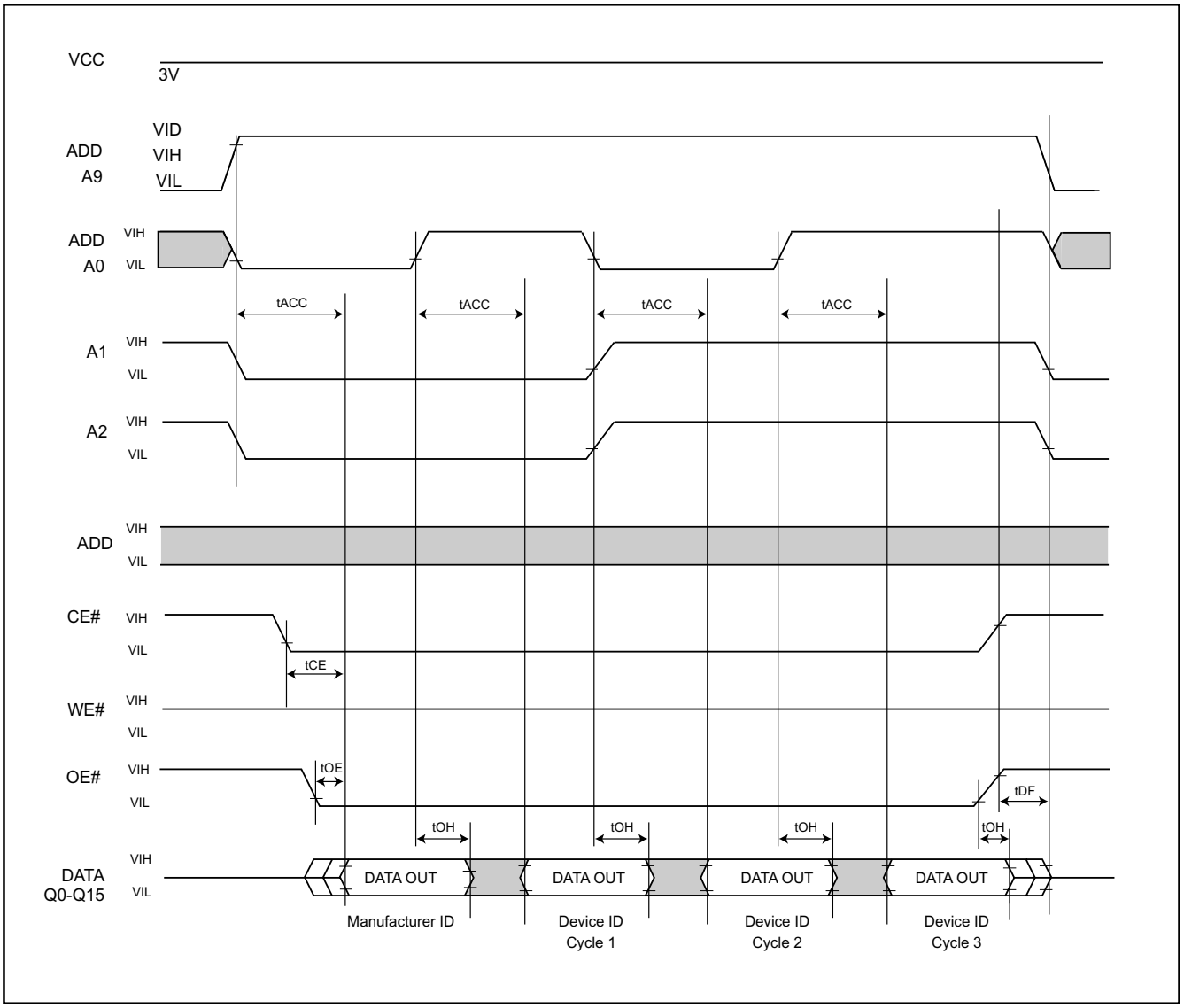
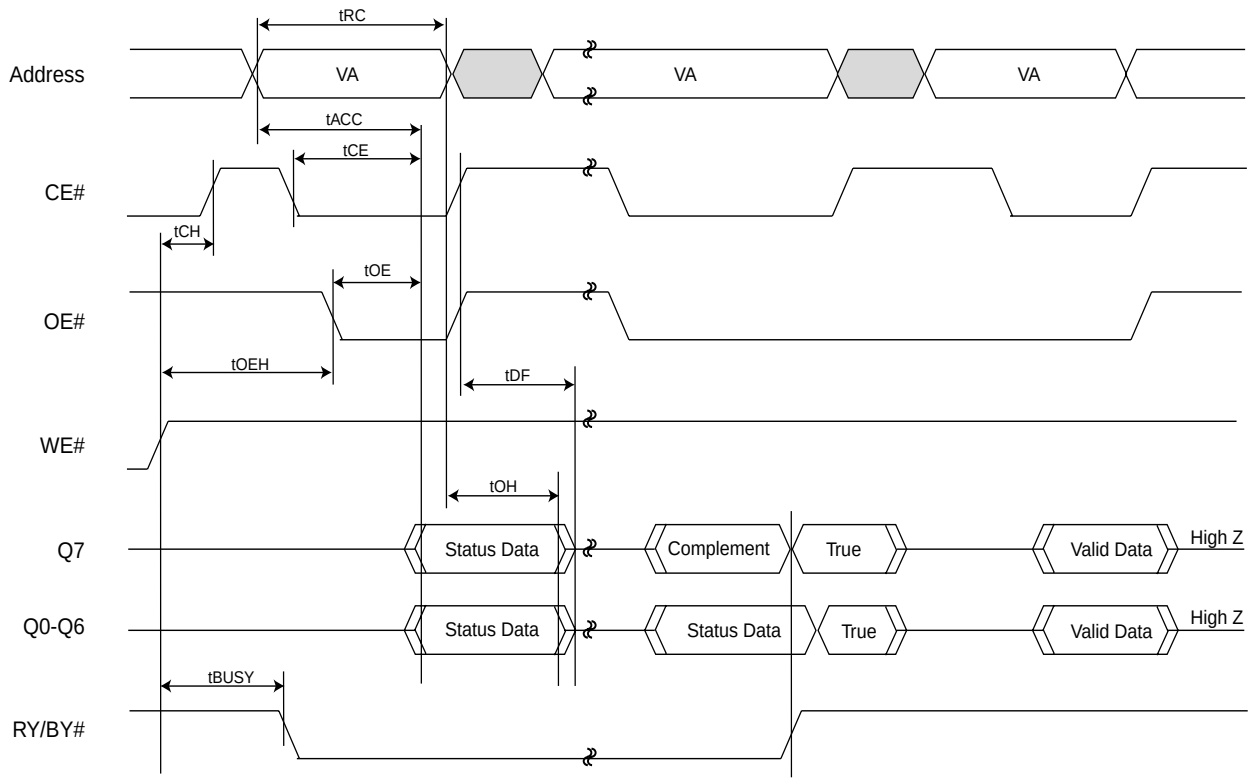


Figure 23. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

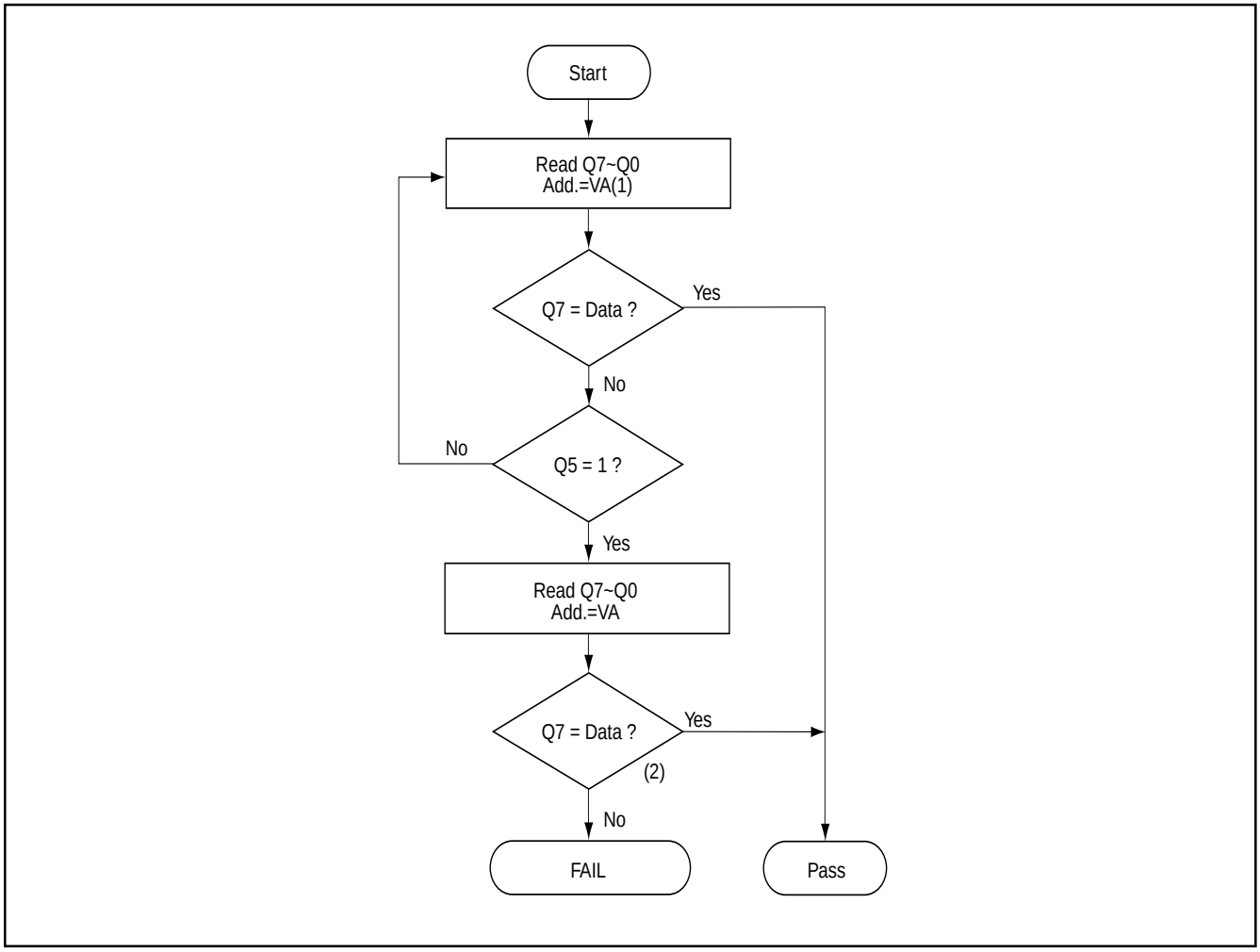
Figure 24. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Note :

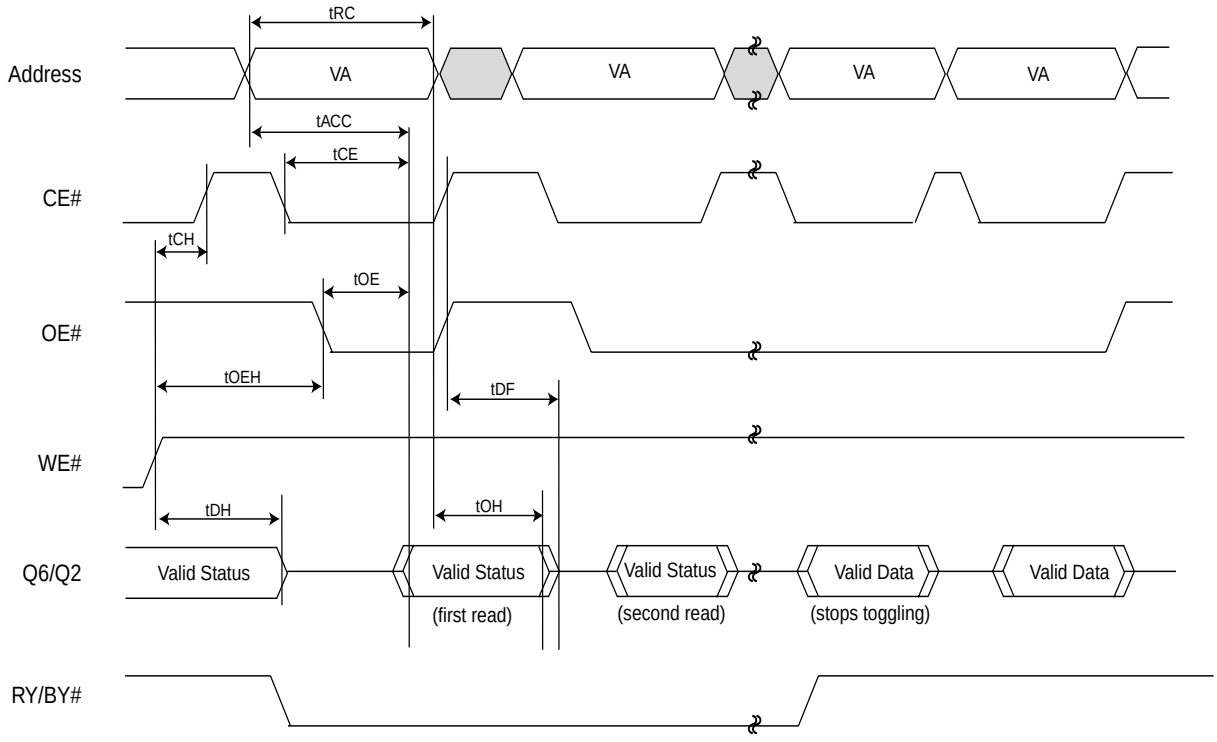
VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

Figure 25. DATA# POLLING ALGORITHM



Notes:
1.VA=valid address for programming.
2.Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

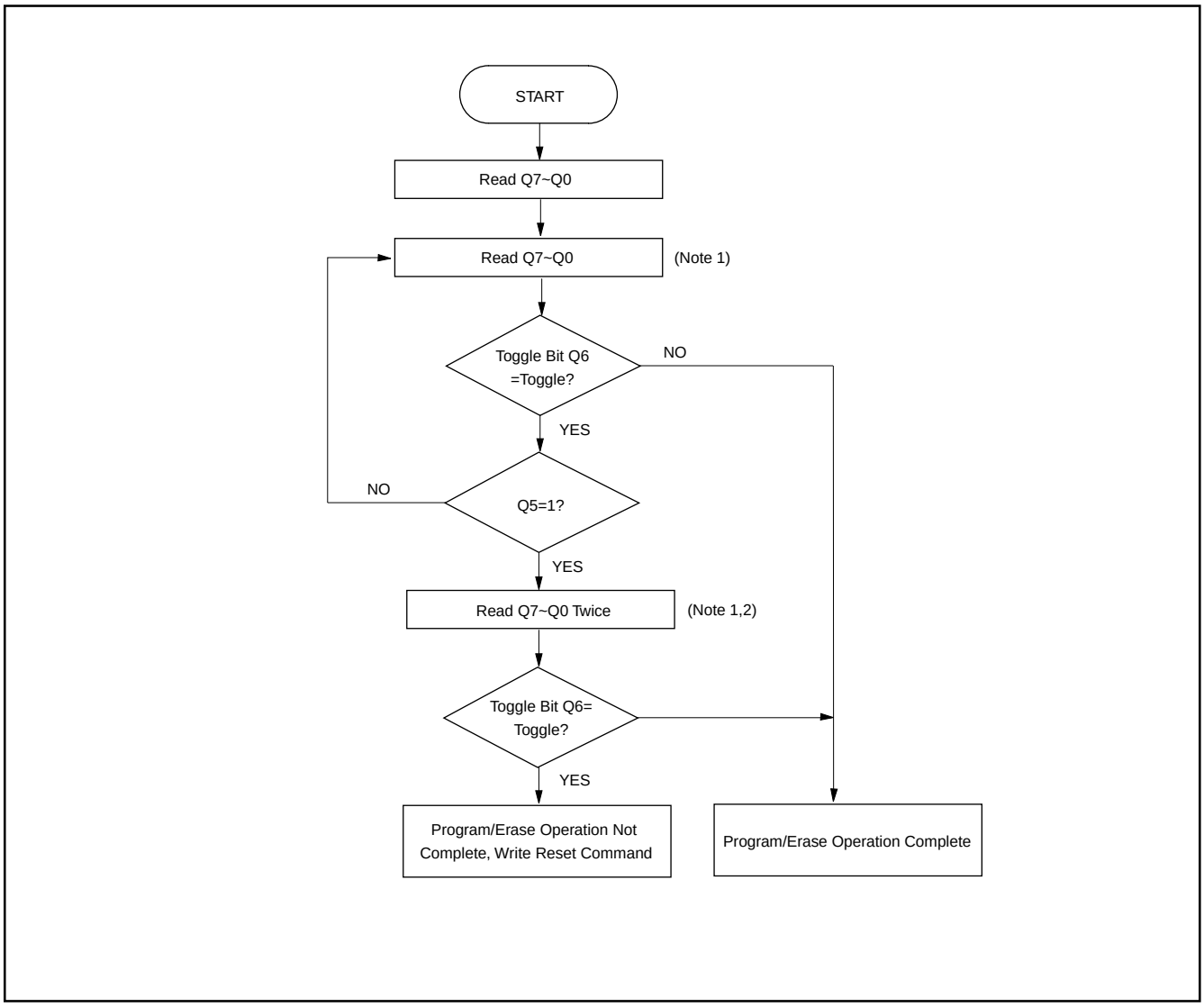
Figure 26. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Note :

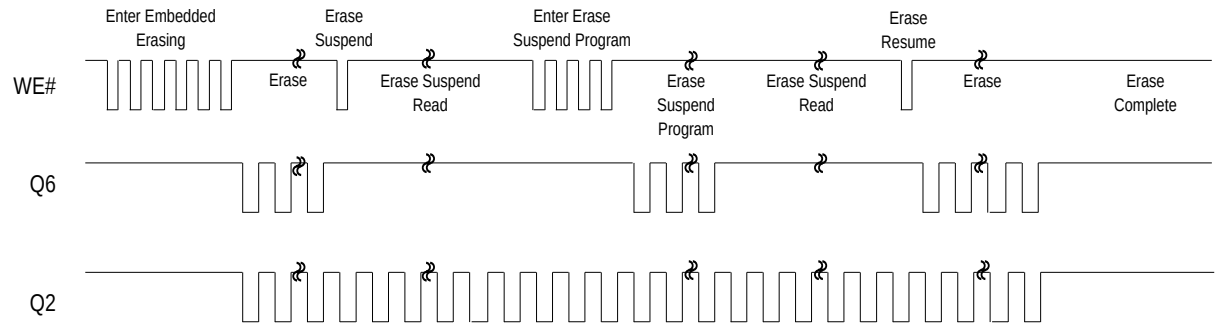
VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 27. TOGGLE BIT ALGORITHM



Notes :
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 28. Q6 versus Q2



Note :

The system can use OE# or CE# to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.5	2	sec	Excludes 00h programming prior to erasure Note 6
Chip Erase Time	128	256	sec	
Total Write Buffer Program Time (Note 4)	240		us	Excludes system level overhead Note 7
Total Accelerated Effective Write Buffer Program Time (Note 4)	200		us	
Chip Program Time	126		sec	

Notes:
1. Typical program and erase times assume the following conditions: 25° C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. For 1-16 words or 1-32 bytes programmed in a single write buffer programming operation.
5. Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.
6. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
7. System-level overhead is the time required to execute the command sequence(s) for the program command. See Tables 3 for further information on command definitions.
8. The device has a minimum erase and program cycle endurance of 100,000 cycles.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

DATA RETENTION

Parameter	Min	Unit
Minimum Pattern Data Retention Time	20	Years

TSOP PACKAGE CAPACITANCE

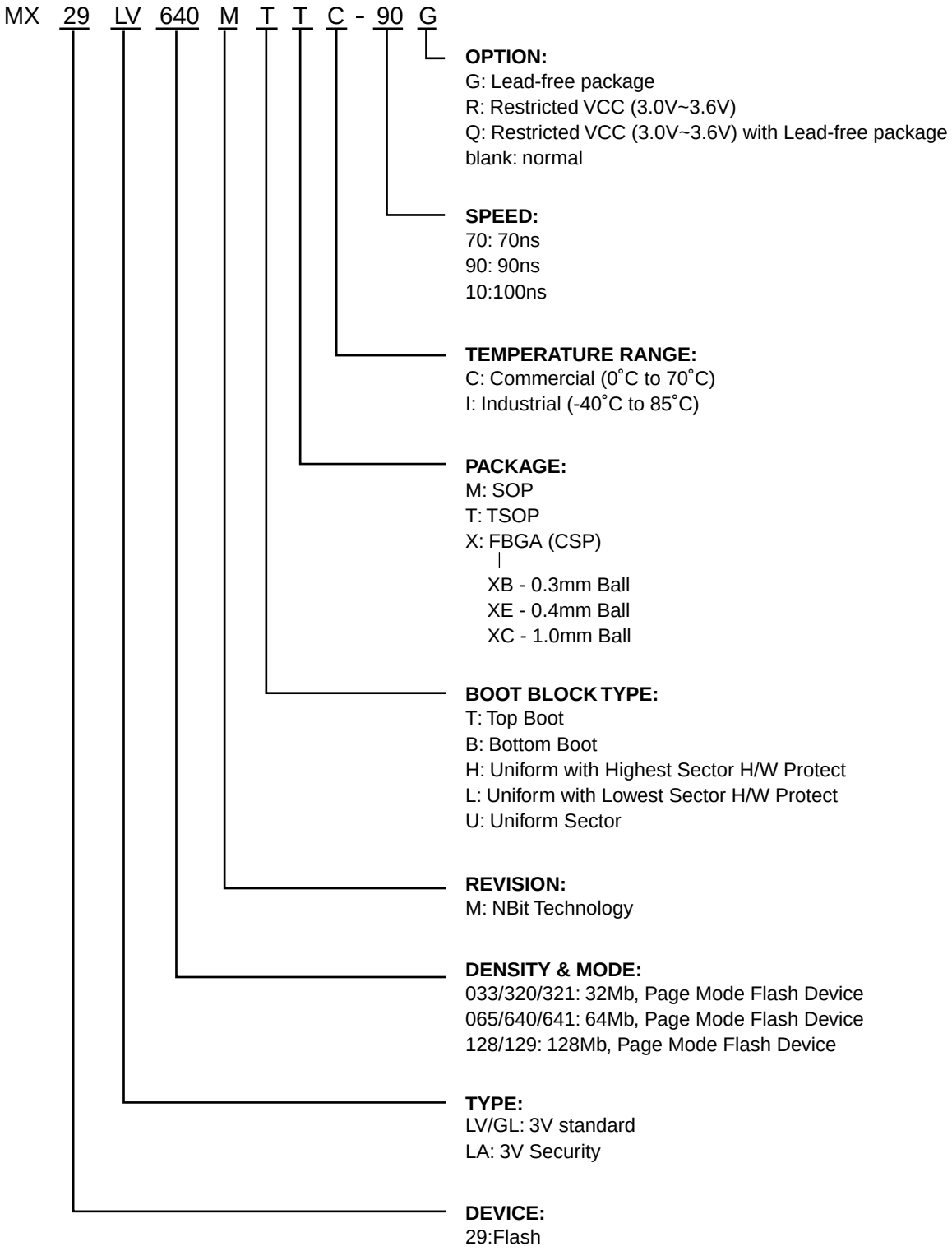
Parameter Symbol	Parameter Description	Test Set		TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	TSOP	6	7.5	pF
COUT	Output Capacitance	VOUT=0	TSOP	8.5	12	pF
CIN2	Control Pin Capacitance	VIN=0	TSOP	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA=25° C, f=1.0MHz

ORDERING INFORMATION

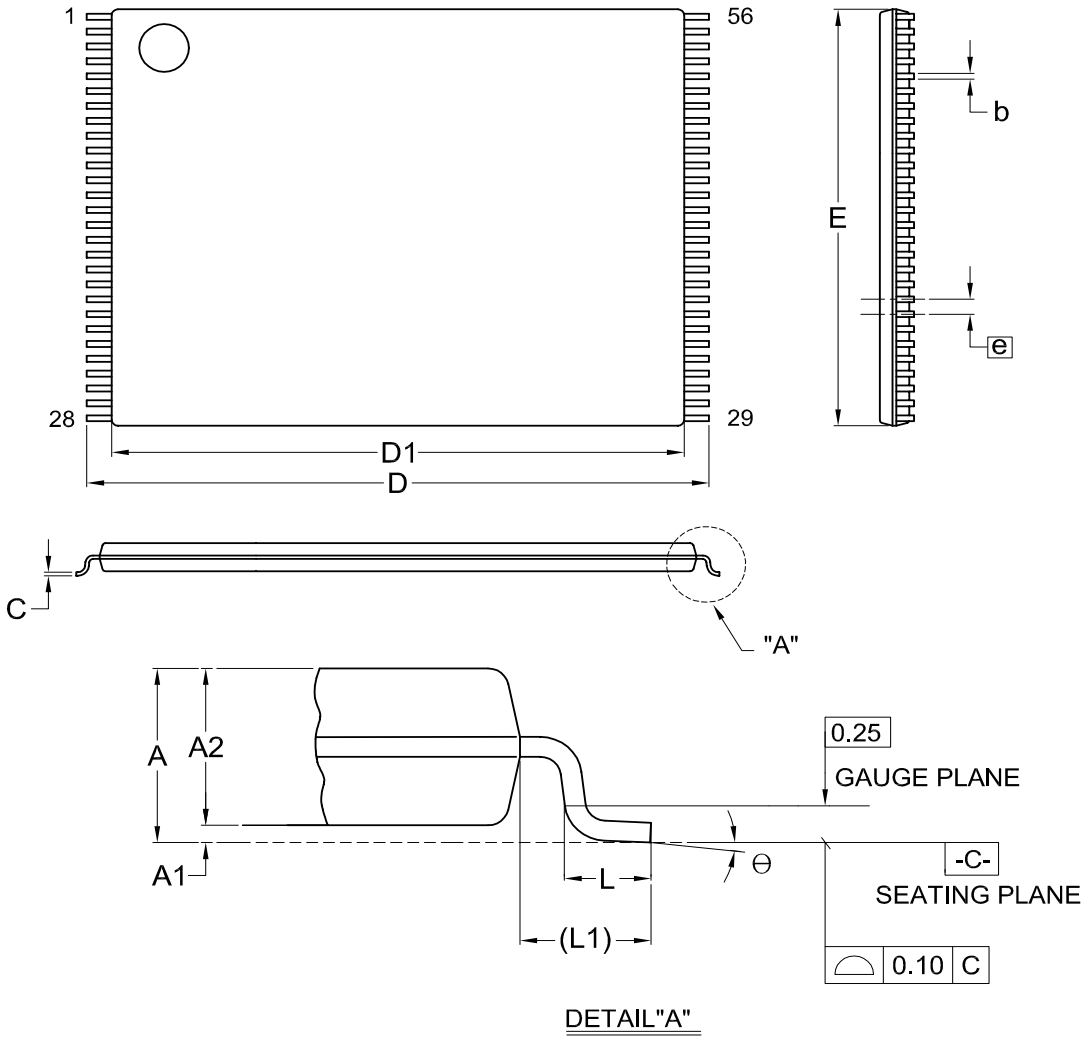
PART NO.	VCC OPERATION (V)	ACCESS TIME (ns)	PACKAGE	Remark
MX29LV128MHTC-90R	3.0~3.6	90	56 Pin TSOP (Normal Type)	
MX29LV128MHTC-10	2.7~3.6	100	56 Pin TSOP (Normal Type)	
MX29LV128MLTC-90R	3.0~3.6	90	56 Pin TSOP (Normal Type)	
MX29LV128MLTC-10	2.7~3.6	100	56 Pin TSOP (Normal Type)	
MX29LV128MHTI-90R	3.0~3.6	90	56 Pin TSOP (Normal Type)	
MX29LV128MHTI-10	2.7~3.6	100	56 Pin TSOP (Normal Type)	
MX29LV128MLTI-90R	3.0~3.6	90	56 Pin TSOP (Normal Type)	
MX29LV128MLTI-10	2.7~3.6	100	56 Pin TSOP (Normal Type)	
MX29LV128MHTC-90Q	3.0~3.6	90	56 Pin TSOP (Normal Type)	Pb-free
MX29LV128MLTC-90Q	3.0~3.6	90	56 Pin TSOP (Normal Type)	Pb-free
MX29LV128MHTI-90Q	3.0~3.6	90	56 Pin TSOP (Normal Type)	Pb-free
MX29LV128MLTI-90Q	3.0~3.6	90	56 Pin TSOP (Normal Type)	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 56L (14X20mm)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	13.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	14.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	14.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.547		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.551	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.555		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1608	4	MO-142			12-01-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary" wording	P1	AUG/11/2005
	2. Added description about Pb-free device is RoHS compliant	P1	
	2. Added note 7 for ILIT parameter in DC Characteristics table	P34	
	3. Added comments into performance table	P65	
	4. Added Part Name Description	P68	
1.1	1. Correct "Package Capacitance" table	P66	FEB/08/2006

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